ASP-DAC 2024

wearMeter: an Accurate Wear Metric for NAND Flash Memory

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Direct Measurement and Indirect Measurement.

How smart?

Wear degree & wearMeter

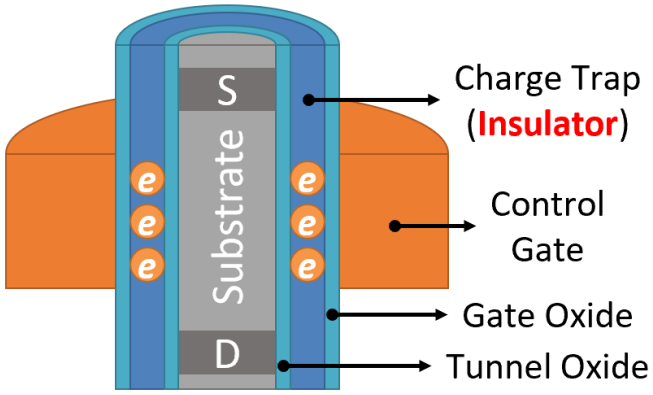
- Wear degree of NAND flash memory can not be directly measured.
- So far, there is no effective method to accurately measure the wear degree.
- We propose an accurate wear degree metric called wearMeter, accompanied by an offline measurement method to accurately measure the wear degree of NAND flash memory.

3D NAND Flash memory

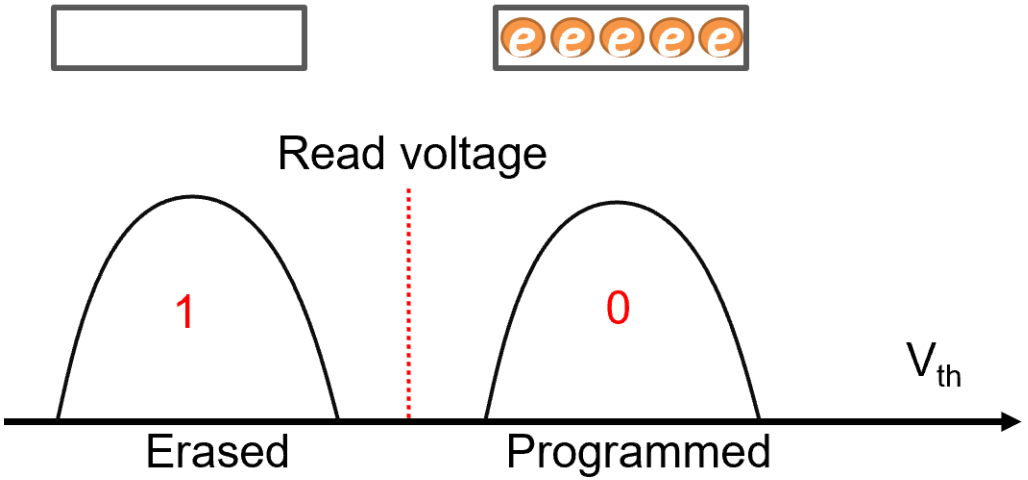
- Everywhere today: from mobile to data centers
- By 2025, 3D NAND will consume over 95% of all NAND flash memory
- The most widely used non-volatile memory in the world

Program & Erase Operations

- Program operation:
  - Injecting electrons into the memory cell to represent bit 0
- Erase operation:
  - dragging electrons out of the memory cell to represent bit 1.

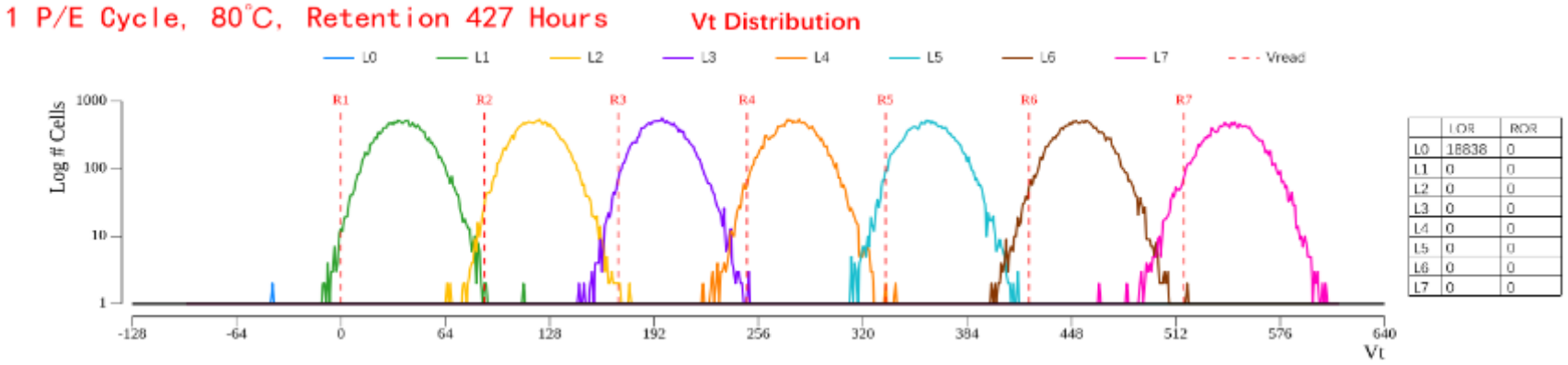


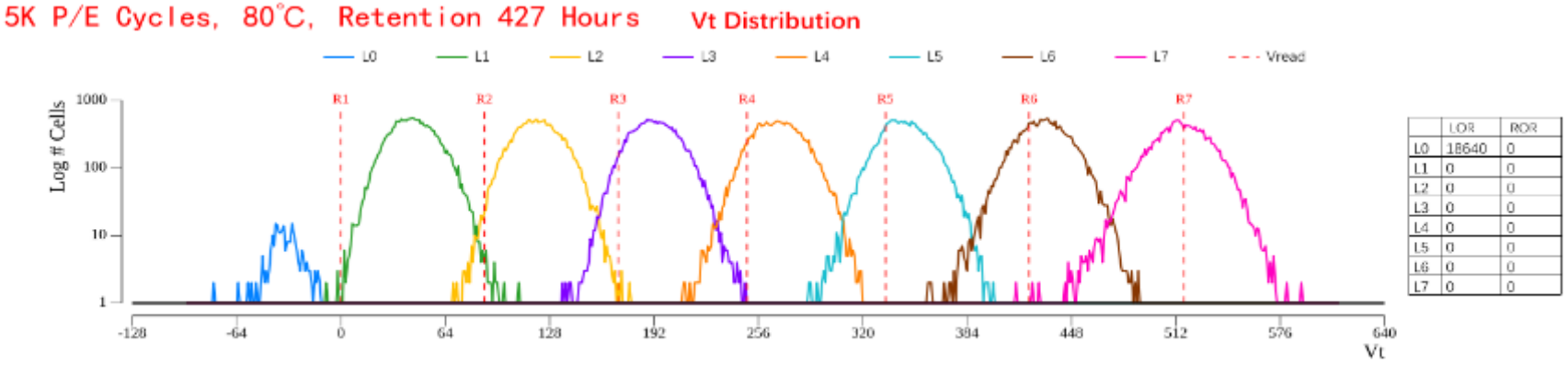
3D Charge-Trap Cell



Program /Erase (P/E) cycles

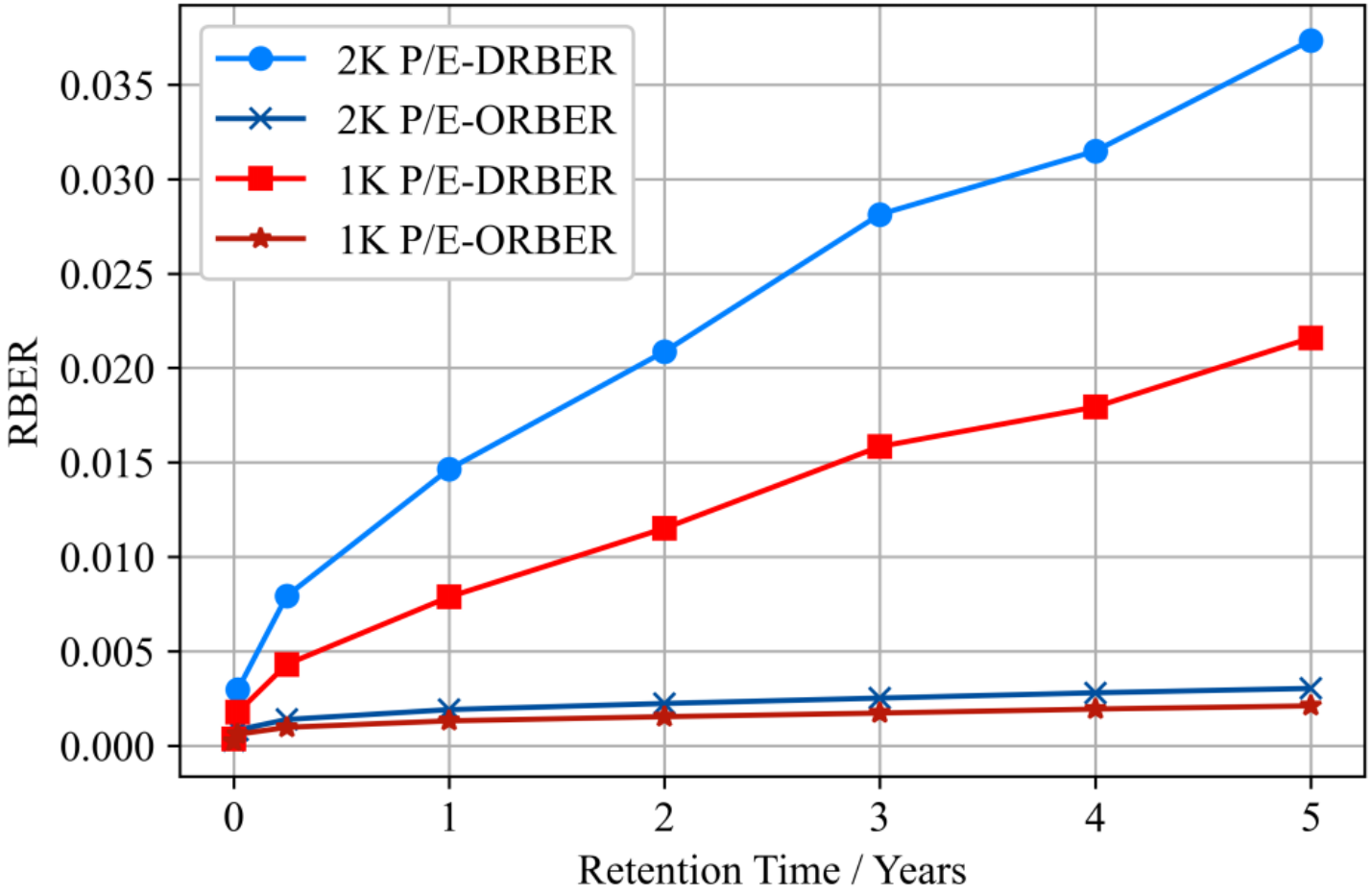
- P/E cycles are the primary cause of increased wear degree.
- The higher the wear degree, the greater the retention loss.
- Traditionally, P/E cycles are used as a metric to measure wear degree.



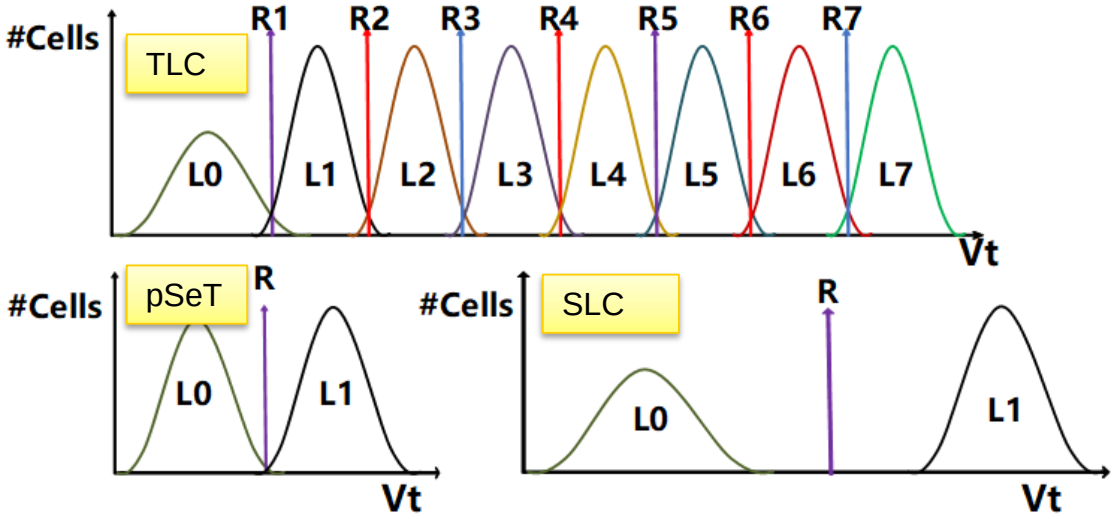


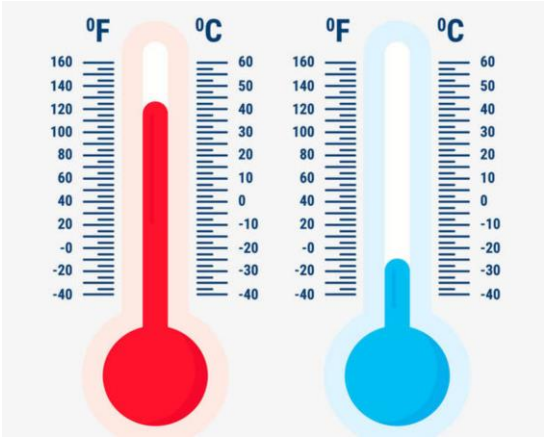
The impact of P/E cycles & retention

- RBER: Raw Bit Error Rate;
- DRBER: Default RBER, read by default read voltage;
- ORBER: Optimal RBER, read by optimal read voltage;



P/E cycles = Wear degree?





- xLC modes: consistent wear in P/E cycles?
- Temperature impact on P/E cycle wear?
- Dwell time effect on P/E cycle wear?

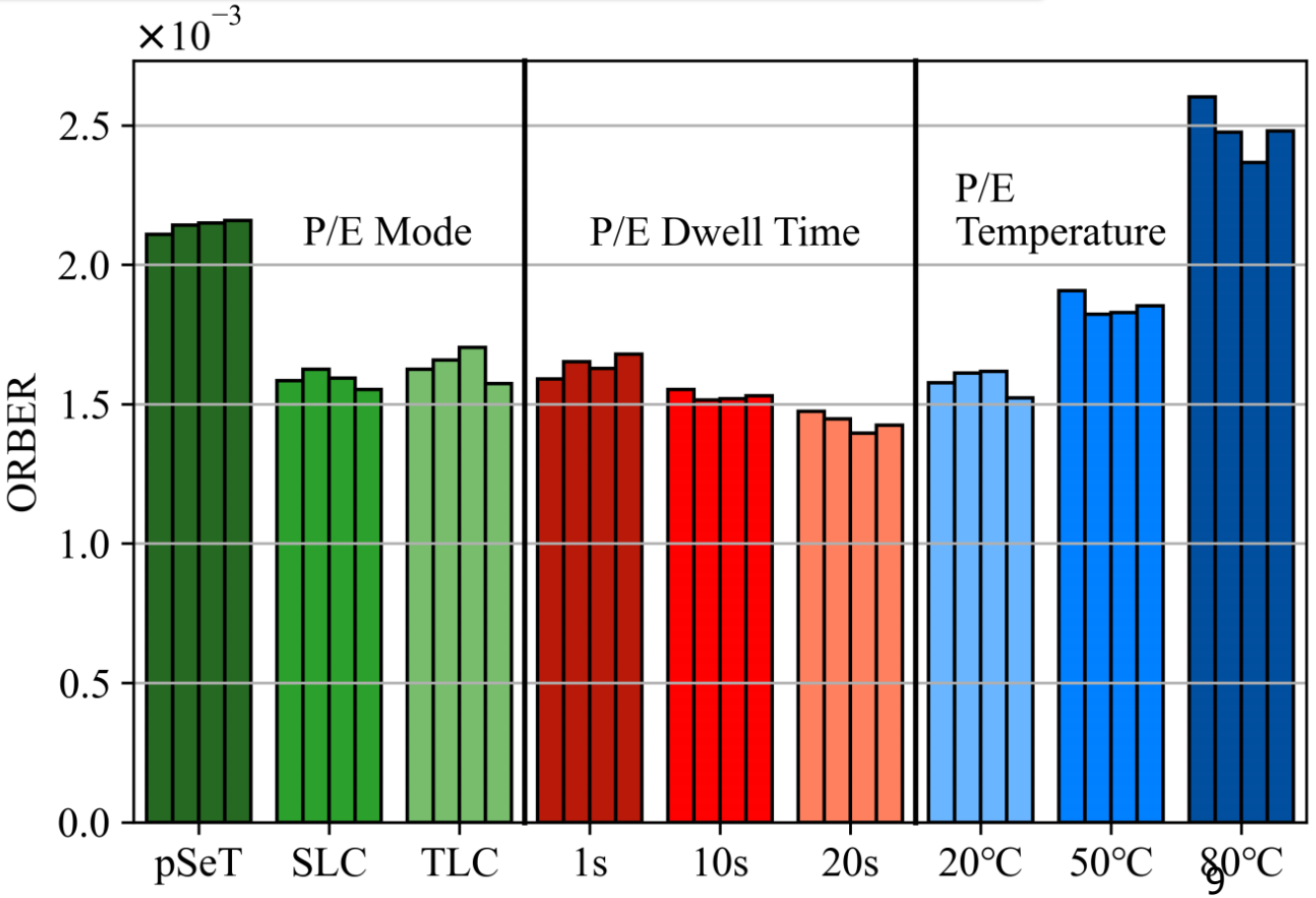
P/E cycles ≠ Wear degree

For equal block wear degree, similar ORBER is expected under the same conditions (same data, same retention time at the same temperature).

- Different program/erase settings can lead to different degrees of wear;

- The longer the dwell time, the lower the wear caused by program/erase operations;

- The higher the temperature, the higher the wear caused by program/erase operations.



wearMeter

$$w = 100(\mu + 9\sigma)$$

- μ: the average ORBER of a block
- σ: standard deviation across all the codewords in the block.
- μ + 9σ is the estimation of the maximum ORBER of the block
- The reliability in data storage of a flash block can indicate the wear degree of the block.

Measure Steps

Step 1: Neutralization

- Perform two P/E operations to the block in the default TLC mode, with each programming different random data into the block.

Step 2: Data Retention

- Introduce retention time on the block, baking at 125℃ for a duration equivalent to one year at 30℃.

Step 3: ORBER Acquisition

- Collect the ORBER for each individual codeword in the block after the retention time.

Step 4: ORBER Statistics

- Compute the average ORBER (μ) and standard deviation (σ) across all the codewords in the block

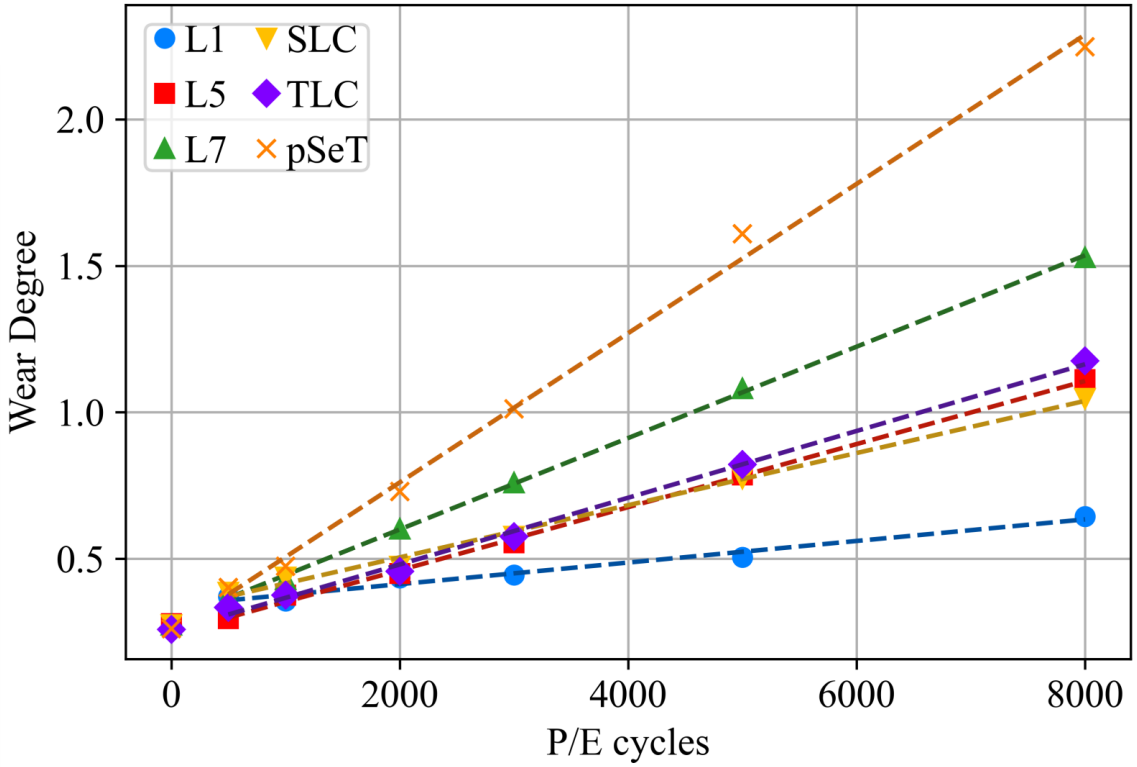
Two Primary Benefits of wearMeter

- Independent of the Wear Sources
  - Independent of the specific P/E pattern, temperature, P/E dwell time, and other wear sources, making it possible to accurately measure the wear degree.
  - Allows for comparison among different sources of wear, among different blocks, and even among different samples.
- Straightforward Assessment of Block Reliability:
  - comparing the wear degree with the error-correcting capability of the ECC engine, denoted as c, we can determine how much reliability margin this block has.
  - The margin of reliability (r) of the block can be expressed as:

$$r = 100c - w$$

Verification on Real Devices

- Perform P/E cycles (0 to 8000) on different blocks.
- Assess wear degree for each P/E level using our measurement method.
- Model wear degree vs. P/E cycles, estimate P/E for wear degrees 0.5, 0.8, 1.1, 1.4.
- Conduct estimated P/E operations on new blocks.
- Verify wear degree accuracy with our technique; closeness to 0.5, 0.8, 1.1, 1.4 confirms our metric's validity.



The wear degree obtained from actual tests and the corresponding models for six P/E modes across P/E cycles.

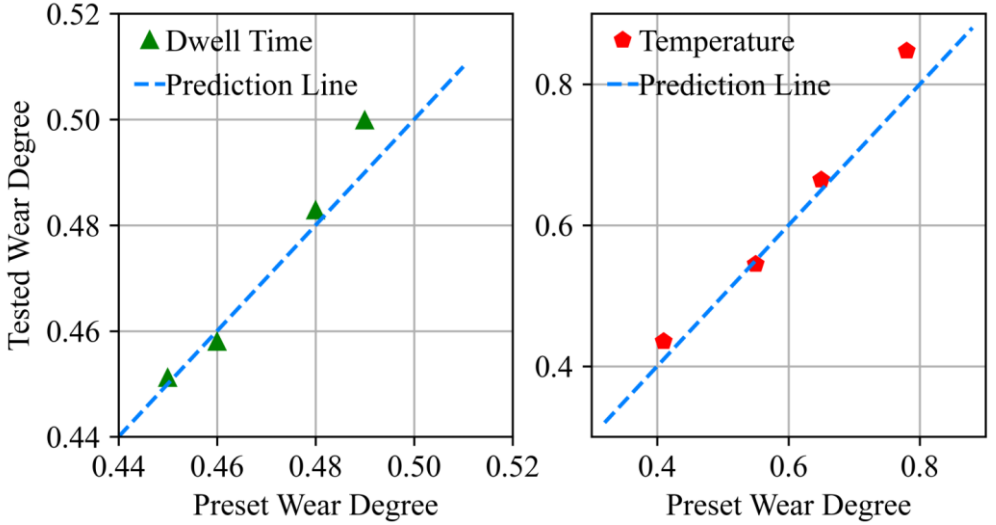
1) SLC: the default SLC mode;
2) TLC: the default SLC mode;
3) pSeT: the SLC program/TLC erase mode;
4) L1: program all cells to Level 1 and erase in TLC mode.
5) L5: program all cells to Level 5 and erase in TLC mode.
6) L7: program all cells to Level 7 and erase in TLC mode.

Verification on Real Devices

The estimated number of P/E cycles at a certain wear degree.

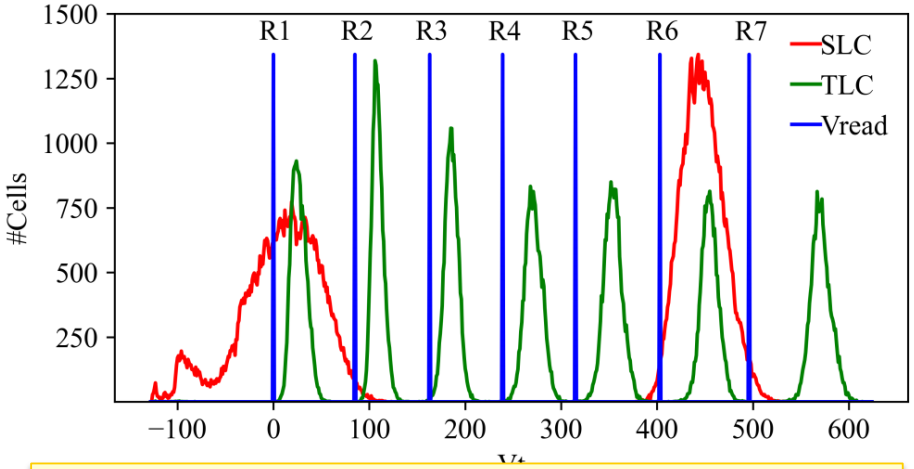
P/E Mode / Wear Degree	L1	L5	L7	SLC	TLC	pSeT
0.5	4344	2627	1406	1784	2523	1068
0.8	9137	5468	3326	4427	5152	2359
1.1	13930	8309	5246	7071	7781	3650
1.4	18723	11149	7166	9714	10410	4941

Despite the natural variability among blocks, the precision of the wearMeter's results is notably high, establishing its reliability and efficacy.

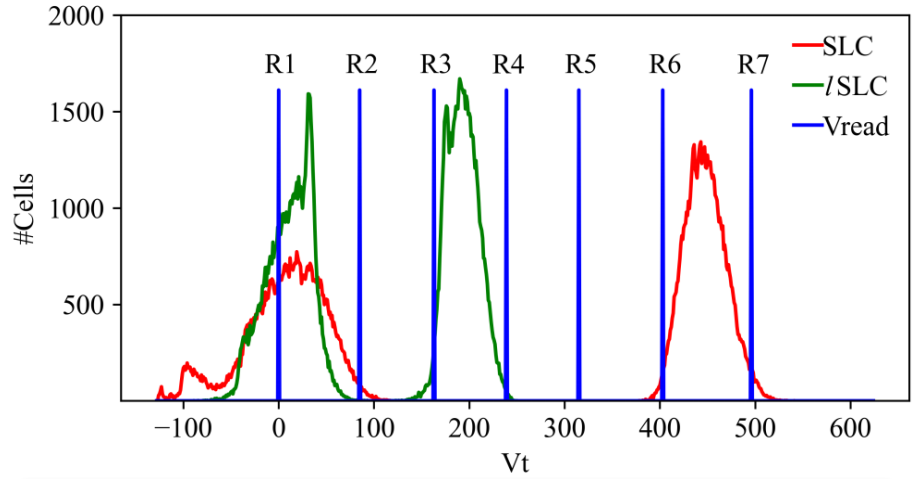


The comparison between the tested wear degrees and the estimated wear degrees, under different dwell times and different temperatures.

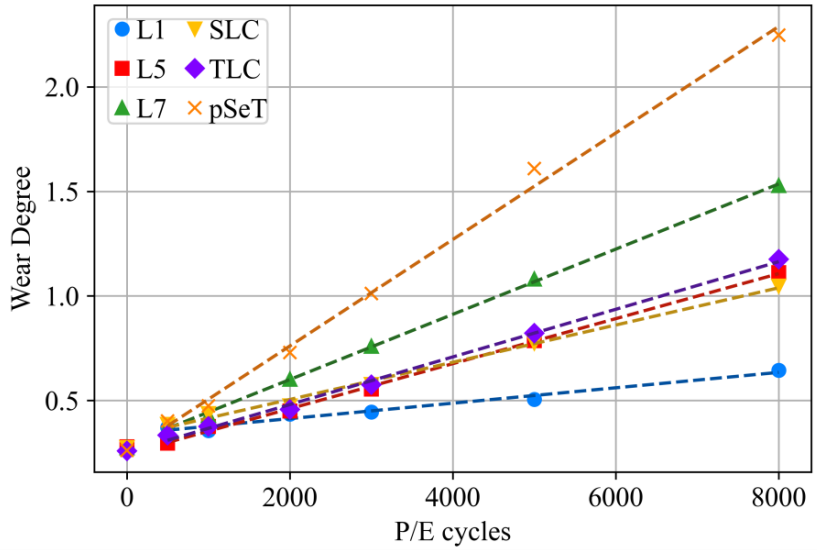
A USE CASE: *l*SLC



The default SLC mode and the default TLC mode.



The default SLC mode and the low-wear SLC (*l*SLC) mode.

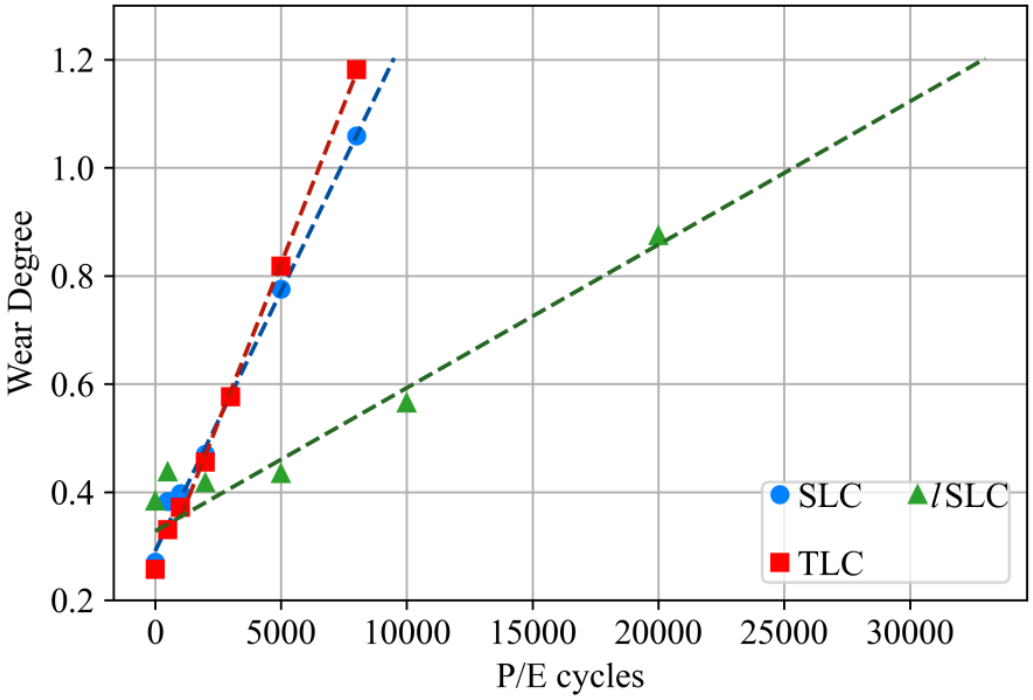


The wear degree of different xLC mode.

- The wear degree of an SLC P/E is much lower than that of a TLC P/E?
- SLC mode blocks are often used for data buffers or storing hot data. The reliability requirement for these blocks is even lower than that of TLC mode.
- we propose a low-level SLC mode to reduce the wear degree of SLC blocks.

A USE CASE: *l*SLC

- Under the same number of P/E cycles, the wear degree is reduced by more than 50%.
- For the same wear degree, the *l*SLC mode can endure more than three times the P/E cycles of the SLC mode.
- The programming time for *l*SLC is roughly 178 microseconds, significantly less than the 427 microseconds for the default SLC mode.



The comparison of wear degree among default TLC mode, default SLC mode, and lSLC mode.

Conclusion

- Show that the current wear metric, P/E cycle, cannot accurately and consistently reflect the wear degree of flash memory;
- Proposed an accurate wear metric called **wearMeter**, accompanied by an offline measurement method for NAND flash memory. Experiments on real flash chips are conducted to verify the effectiveness of the proposed wear metric;
- Leveraging this metric, proposed a low-wear SLC (*l*SLC) mode to enhance SLC mode's lifespan. Real flash sample tests revealed that *l*SLC can endure over 3X the P/E cycles compared to the default SLC when all other conditions remain the same, without performance loss.

Thank You!