The presenter!

- Sina Bakhtavari Mamaghani
- Ph.D. candidate at Karlsruhe Institute of Technology – In collaboration with Siemens (Since 2022)
- M.Sc. in Computer Engineering (2018-2021)
  - Thesis: Design of magnetic-based memory capable of performing basic logic operations
- B.Sc. in Electrical Engineering (2014-2018)
- Research interest:
  - Design and test of emerging memory technologies, including MRAM and ReRAM

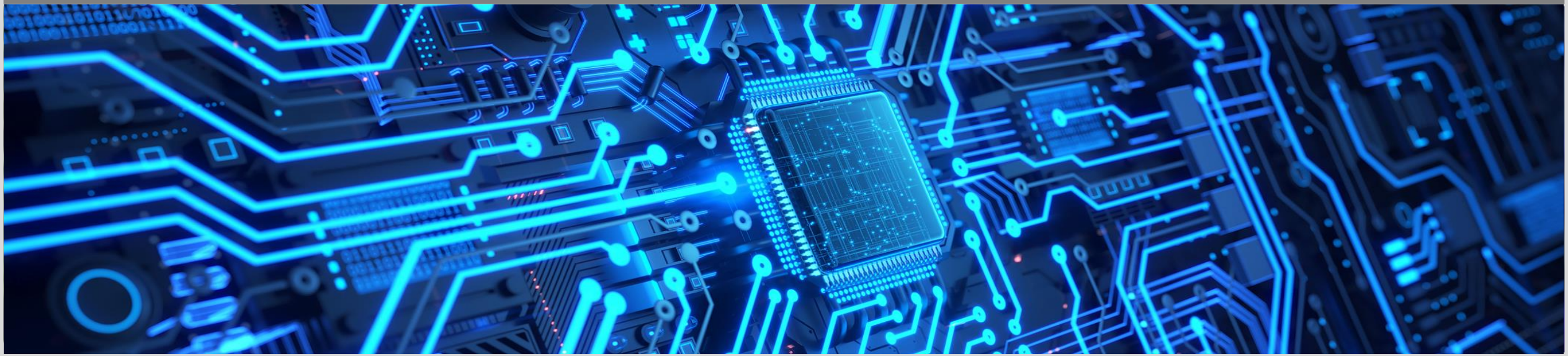
Karlsruhe Institute of Technology

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

A Dynamic Testing Scheme for Resistive-Based Computation-In-Memory Architectures

Presenter: Sina Bakhtavari Mamaghani

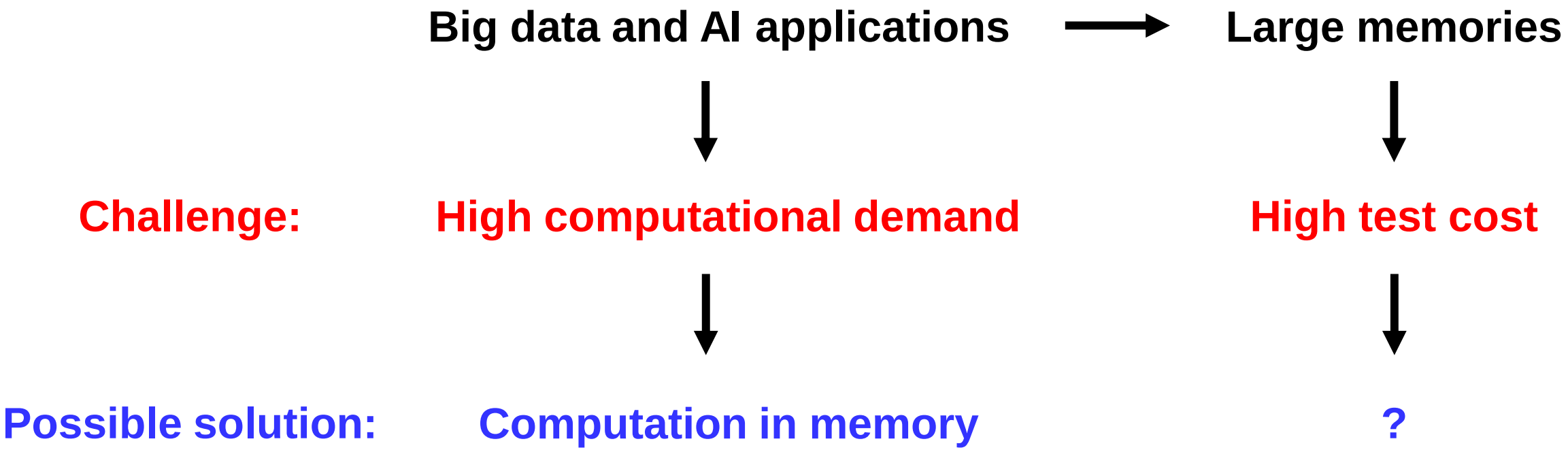
CDNC - Chair of Dependable Nano Computing, Department of Computer Science



Outline of my talk

1. Challenges of big data and AI applications and their associated memory units.
2. Computation-In-Memory (CIM) to the rescue.
3. Using CIM for cost-effective testing.
4. The remaining steps for test improvement.

Challenges of big data and AI applications

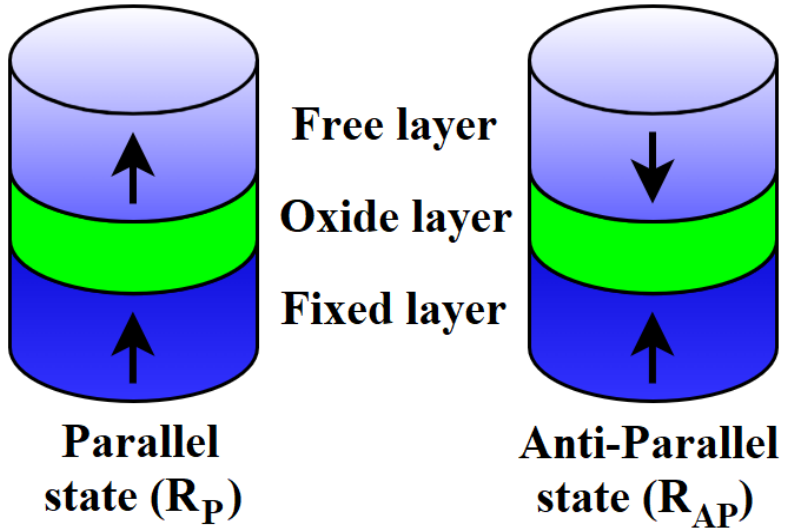


Our goal: use existing on-chip components to solve the high test cost issue

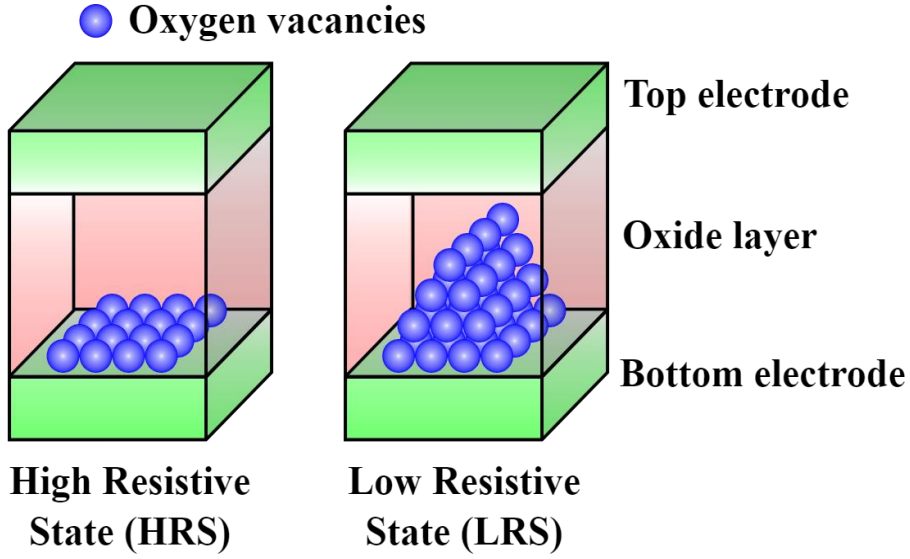
Companies working on emerging memory technologies

Storage elements

- Magnetic tunnel junction (MTJ)
  - Storing data through bi-stable magnetic polarities
  - Parallel state (R_P) → Low resistance
  - Anti-Parallel state (R_{AP}) → high resistance



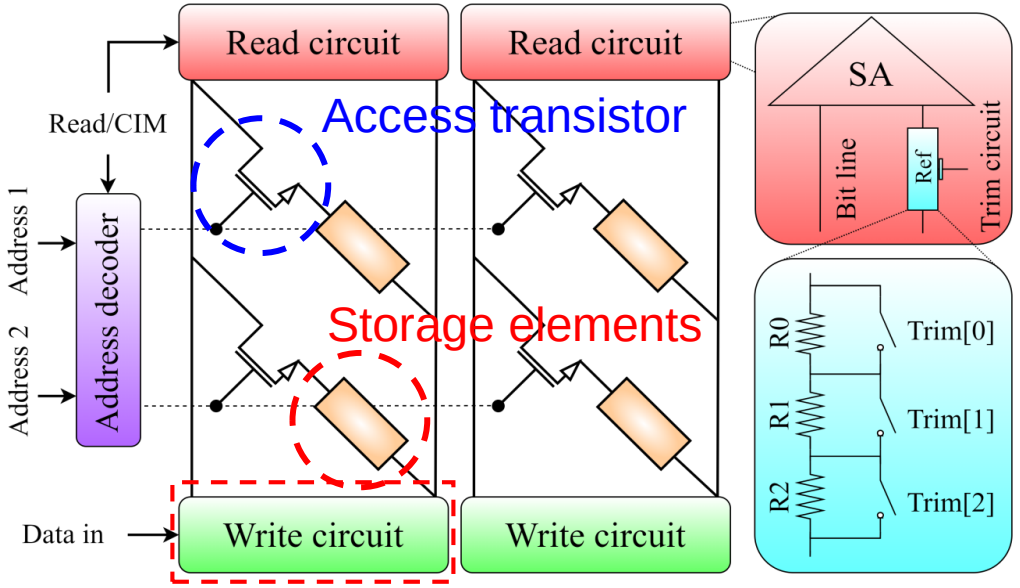
- Valence change memories (VCM)
  - Storing data by conductive filaments
  - Formed conductive filaments (LRS) → Low resistance
  - Destroyed conductive filaments (HRS) → high resistance

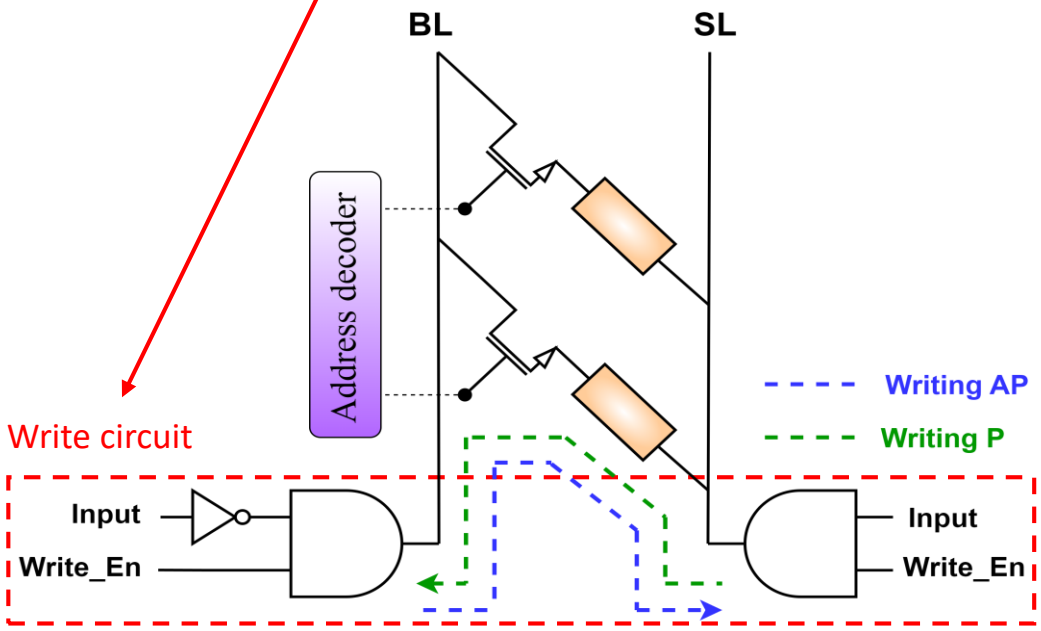


Write circuit

- Write process:
  - Passing a write current through elements
  - Write current (I_{Write} >> $I_{Critical}$)

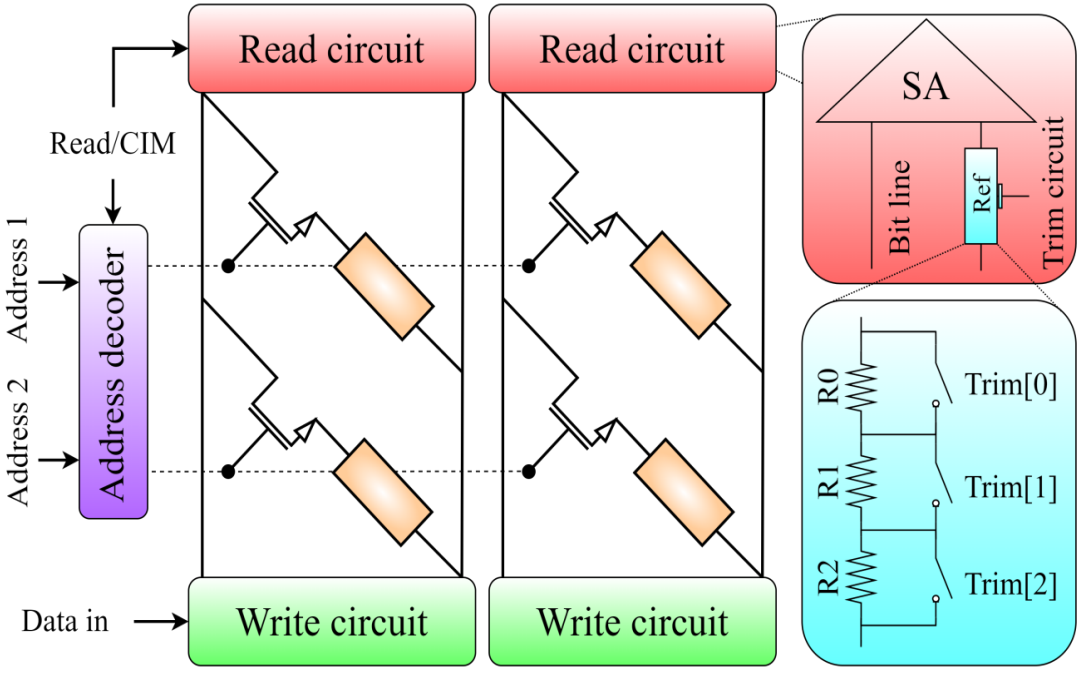
Write_En	Input	Result
0	X	No change
1	0	P → AP
1	1	AP → P

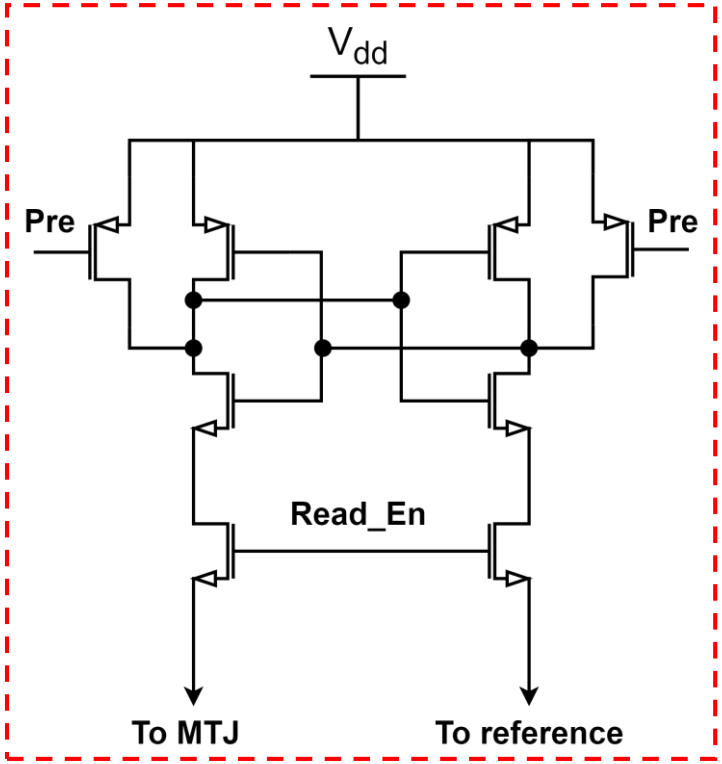




Read circuit

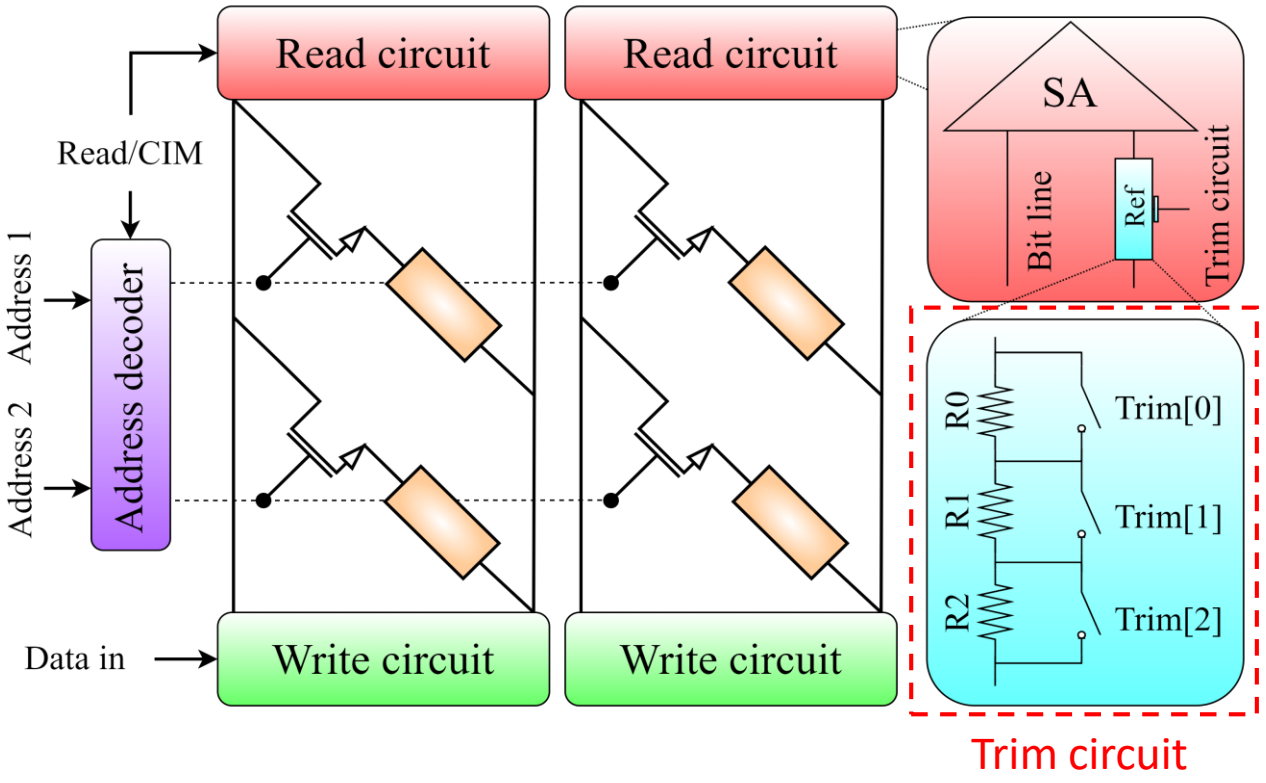
- Work based on different concepts:
  - Current comparison: comparing the read current from storage elements with a reference current
  - Voltage comparison: using voltage division and threshold circuit to read out the value
- Reference source
  - Current source
  - Resistance
- Reference value
  - Fixed
  - Configurable

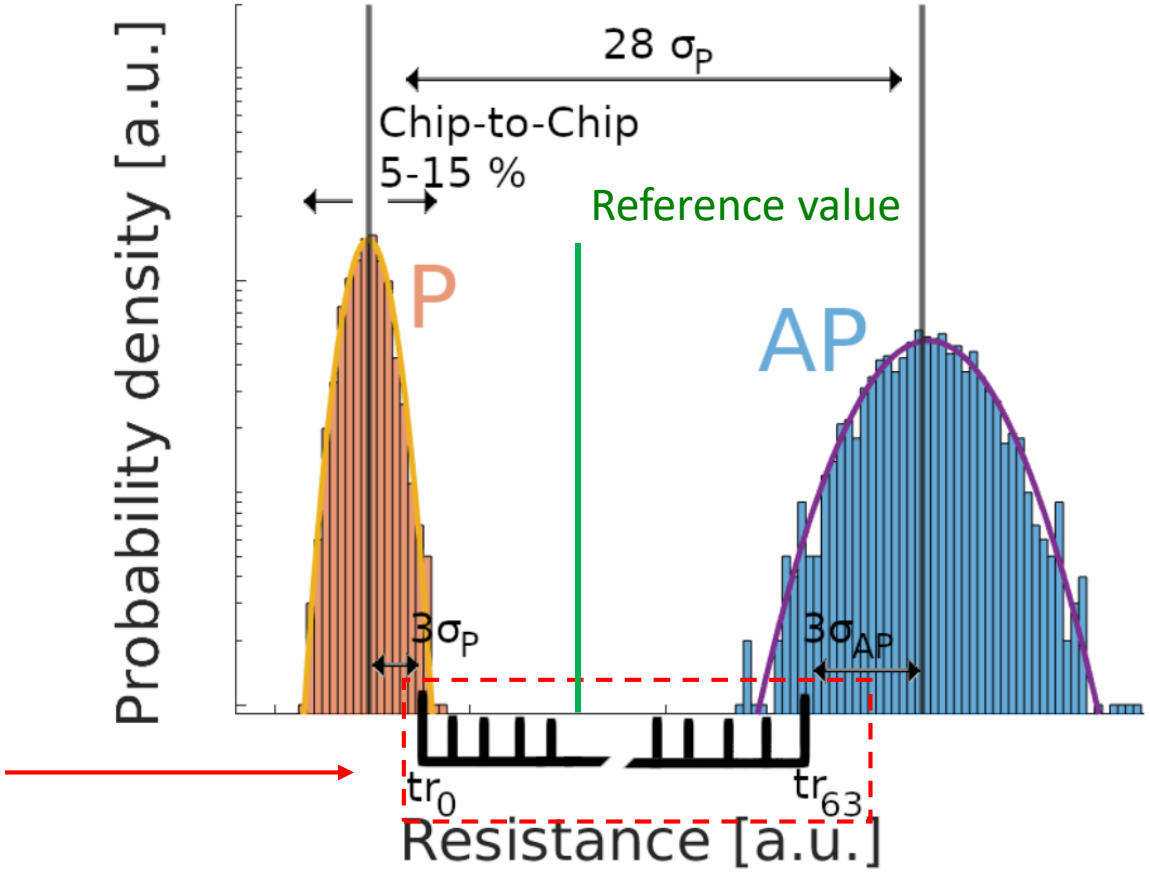




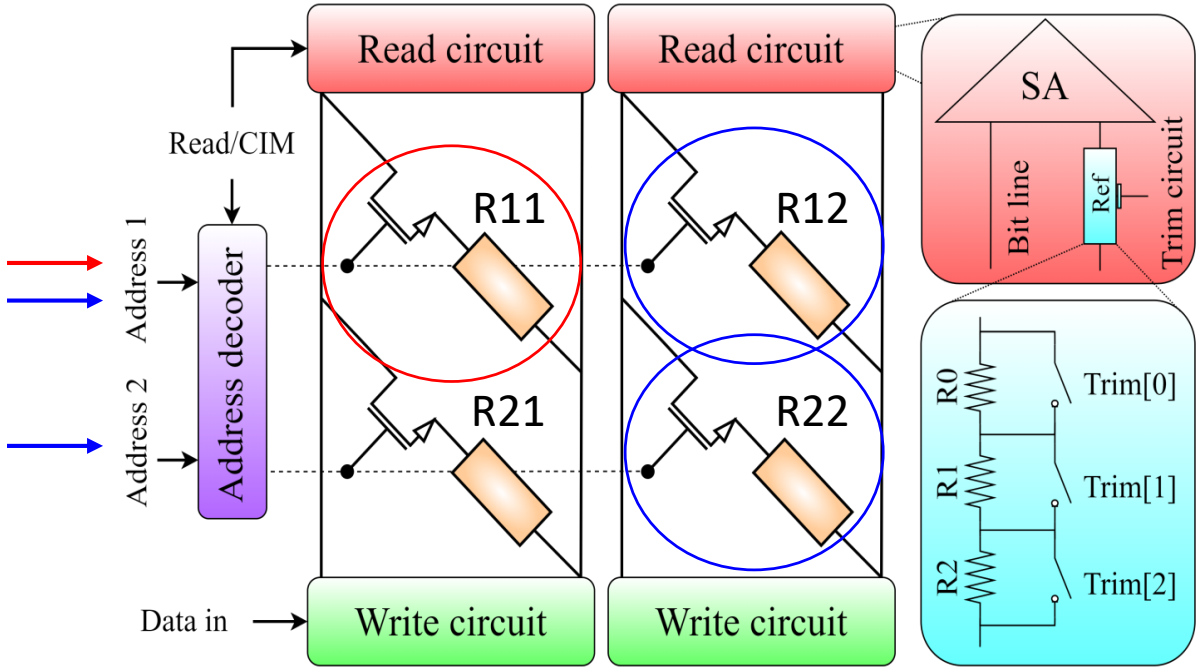
Trim circuit and its importance

- Chip-to-chip variation (5%-15%) → Using trim → Increasing yield

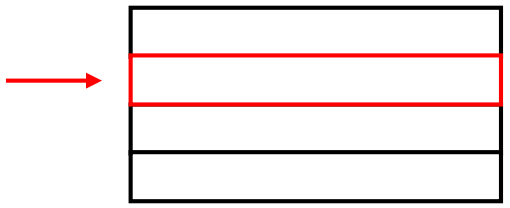




CIM operation



Memory read operation:

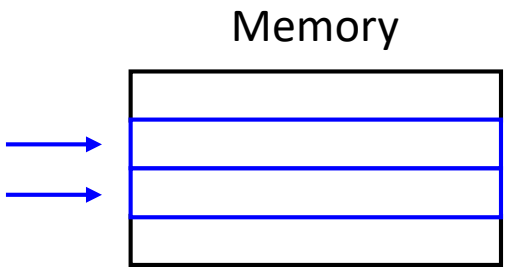


Data_out = 0

R11 > Memory_read_ref ?

Data_out = 1

CIM operation:



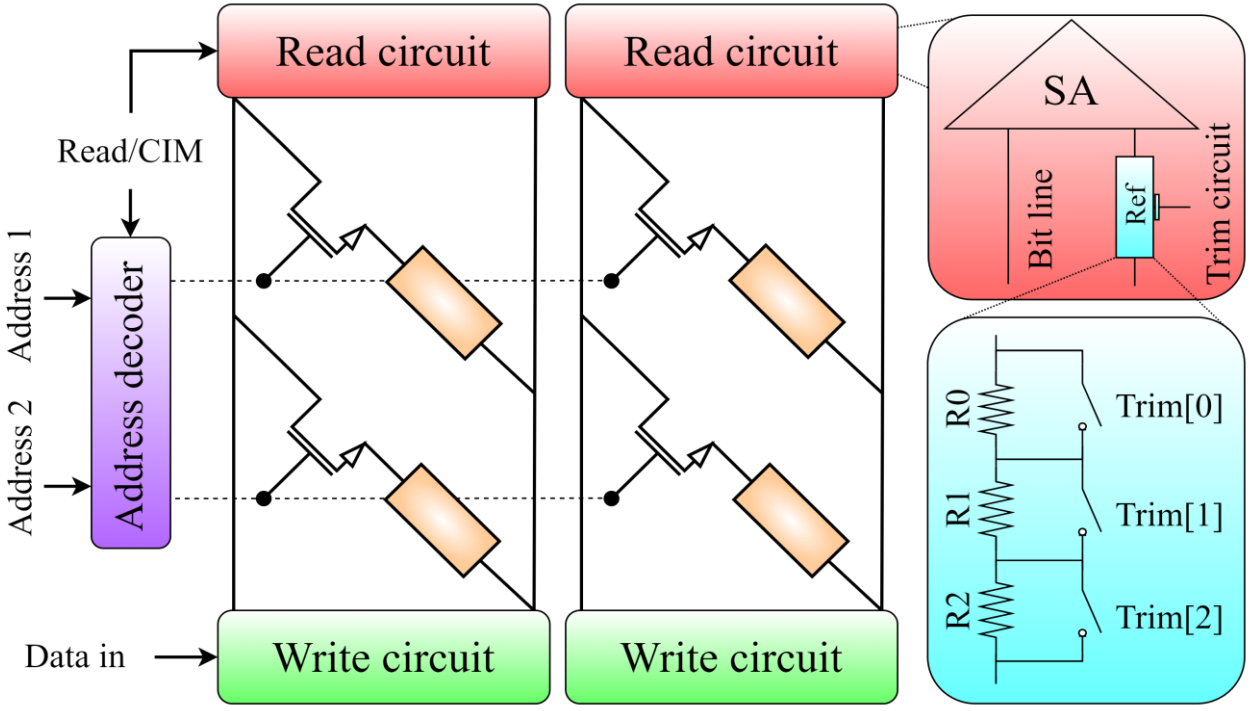
Data_out = 0

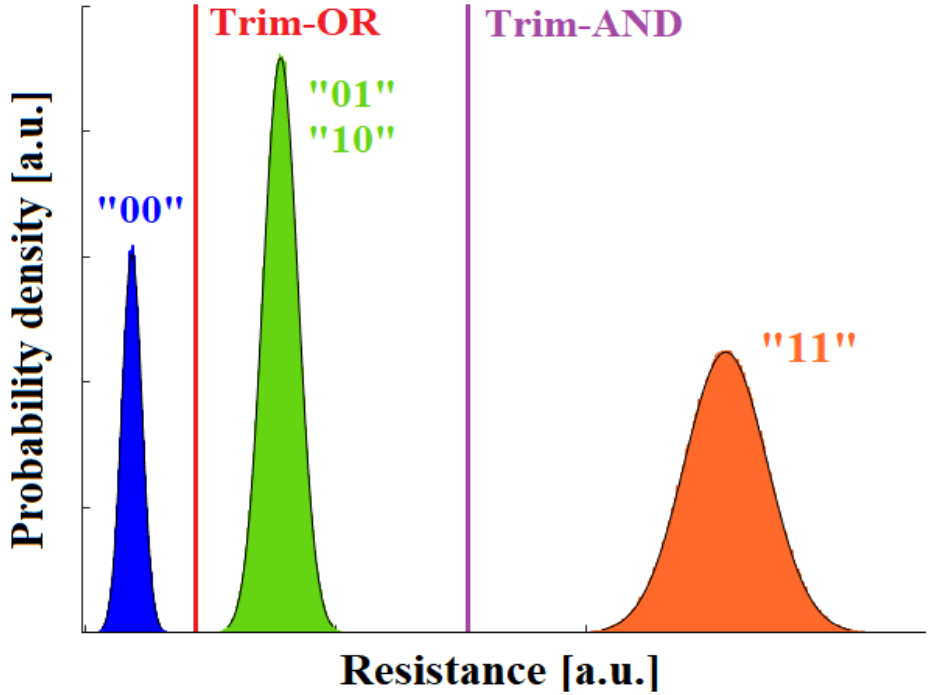
R12 || R22 > CIM_OR_ref ?

Data_out = 1

Trim circuit and its importance

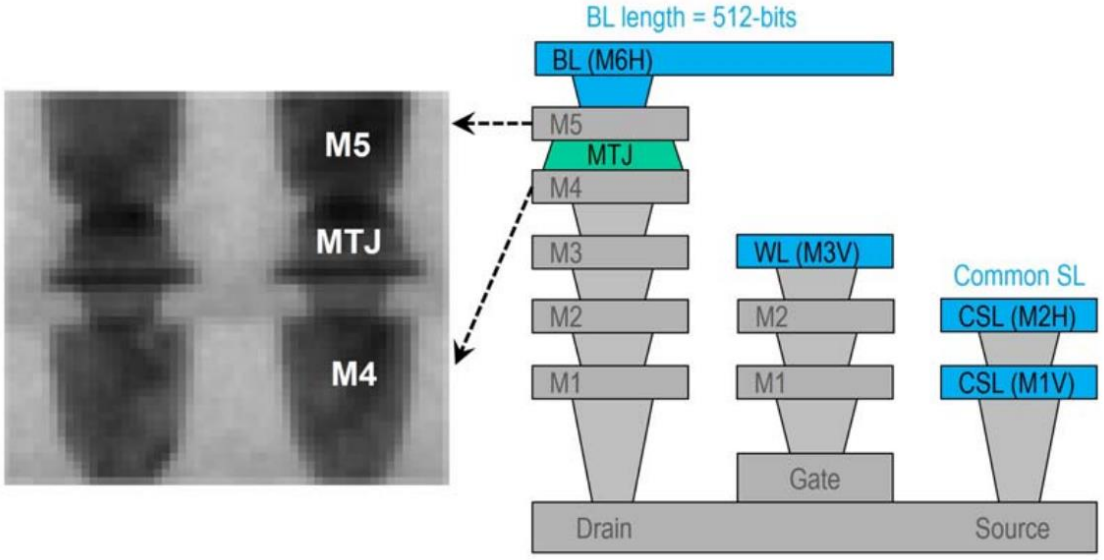
- Providing multi-reference capability for CIM operation.





MTJ defects - Pinhole defect

- A small discontinuity or hole in the insulating layer of the MTJ
  - Diffusion of Boron or other metallic impurities into the MgO layer during the deposition process
  - Diffusion of Oxygen atoms out of the MgO layer due to over-annealing
  - Filling of pinholes in the MgO layer with CoFeB material



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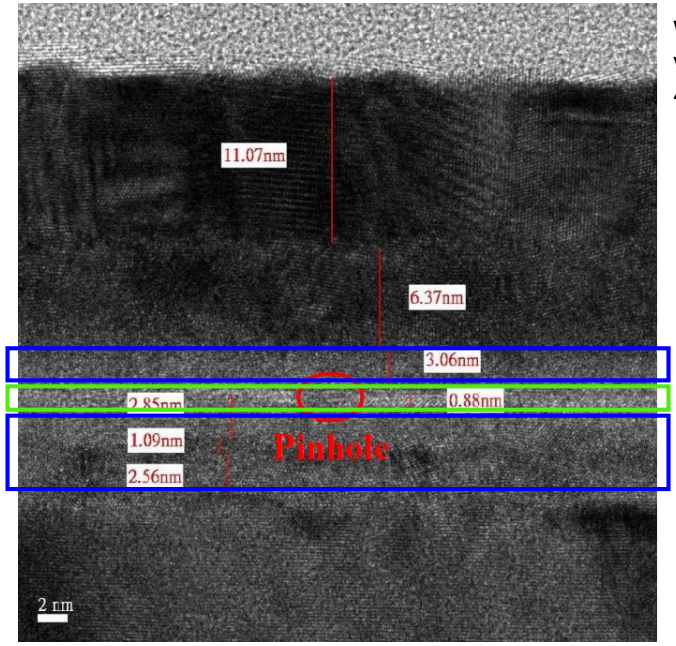
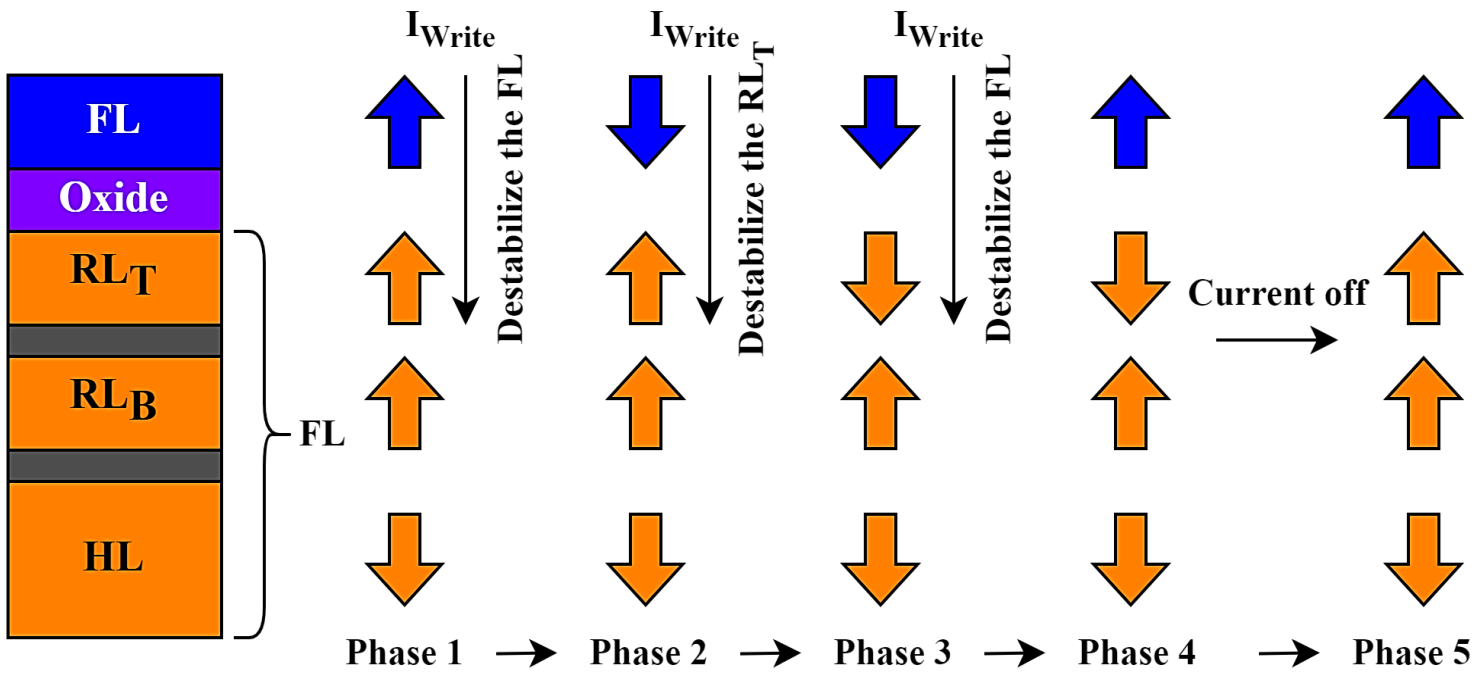


W. Zhao et al., Materials, vol. 9, no. 1. MDPI AG, p. 41, Jan. 12, 2016.

Free layer
Oxide layer
Fixed layer

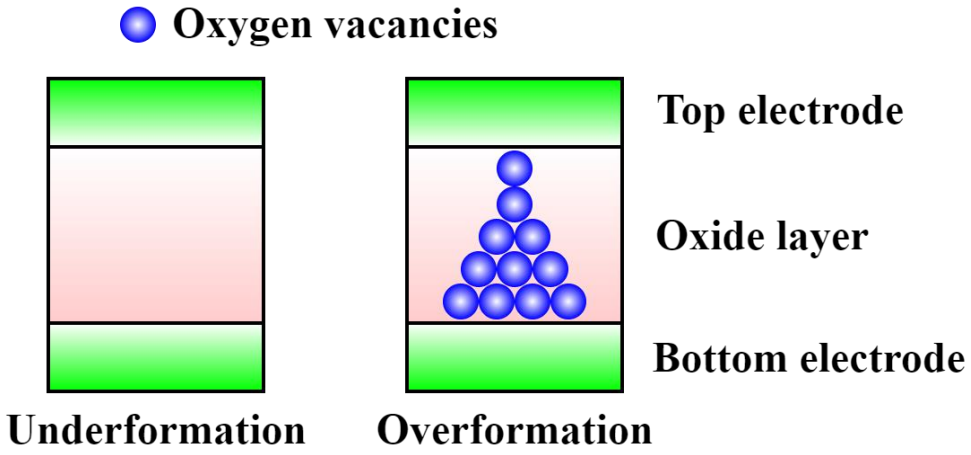
MTJ defects - Back-hopping failures

- Unstable reference layer.
- Data is flipped after the write voltage is removed.



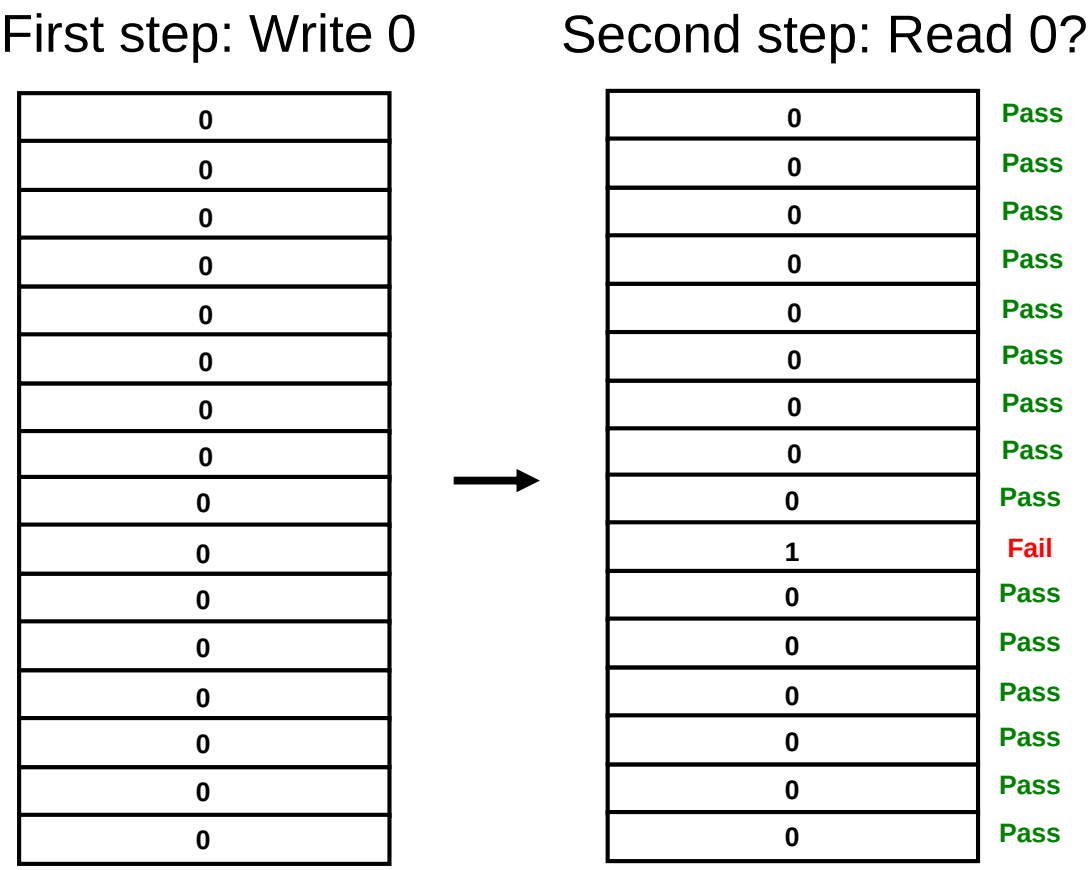
VCM defects – under/over formation

- Formation process
  - Using high voltage to initially form the filament
- Underformation
  - The filament is not formed → open circuit fault
- Overformation
  - The filament physically connects two electrodes → short circuit fault



Current test solutions

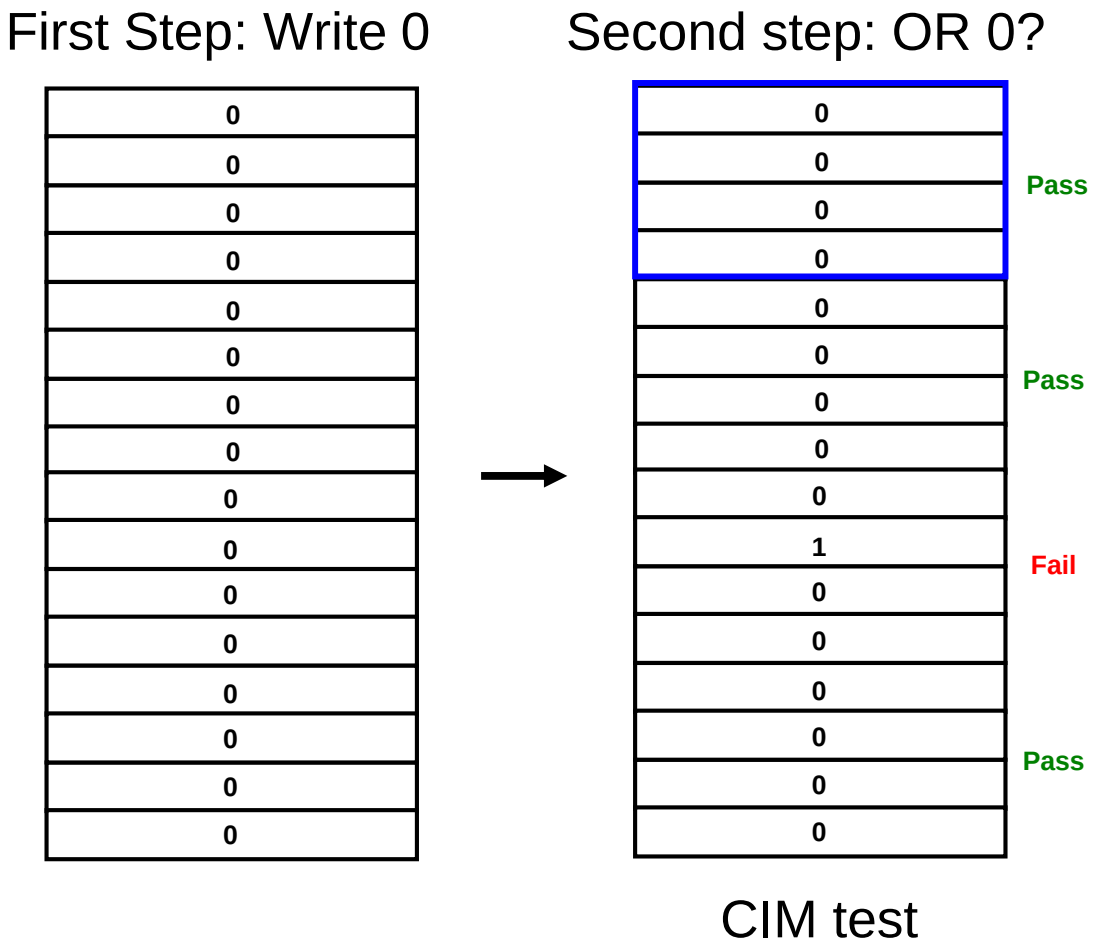
- March C



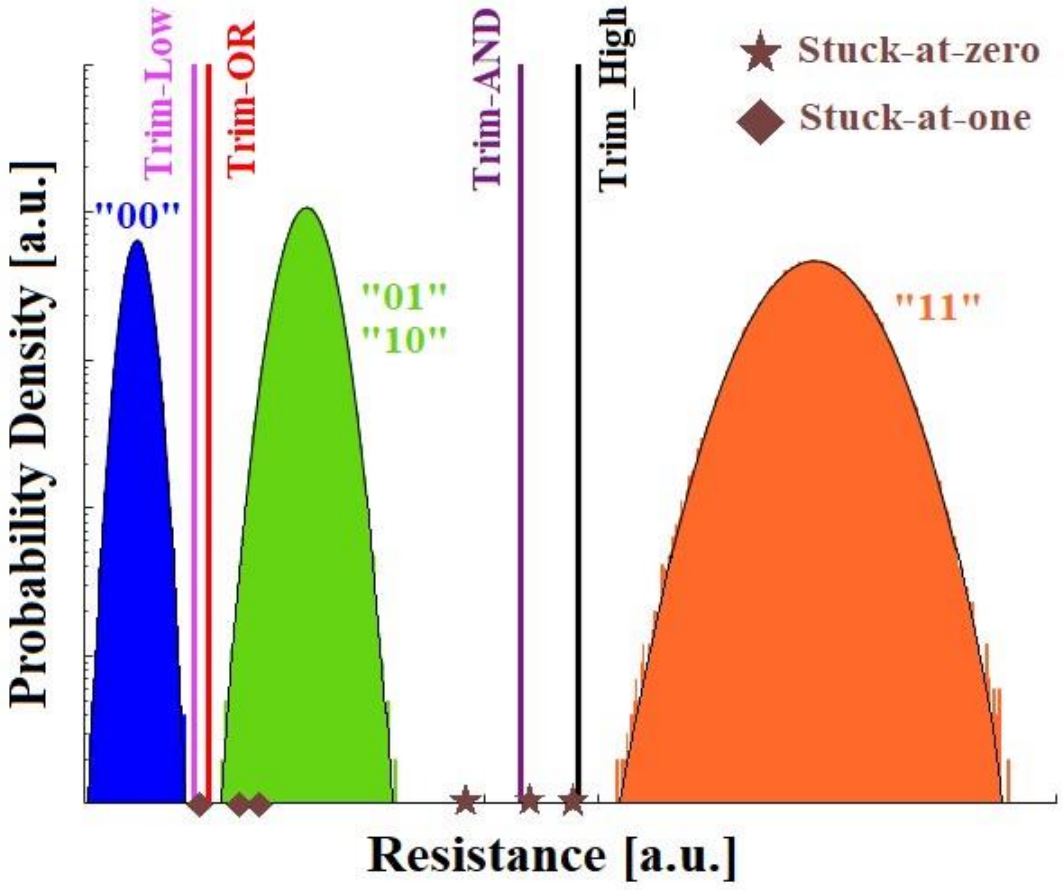
Same step if performed for stuck at 0 defects

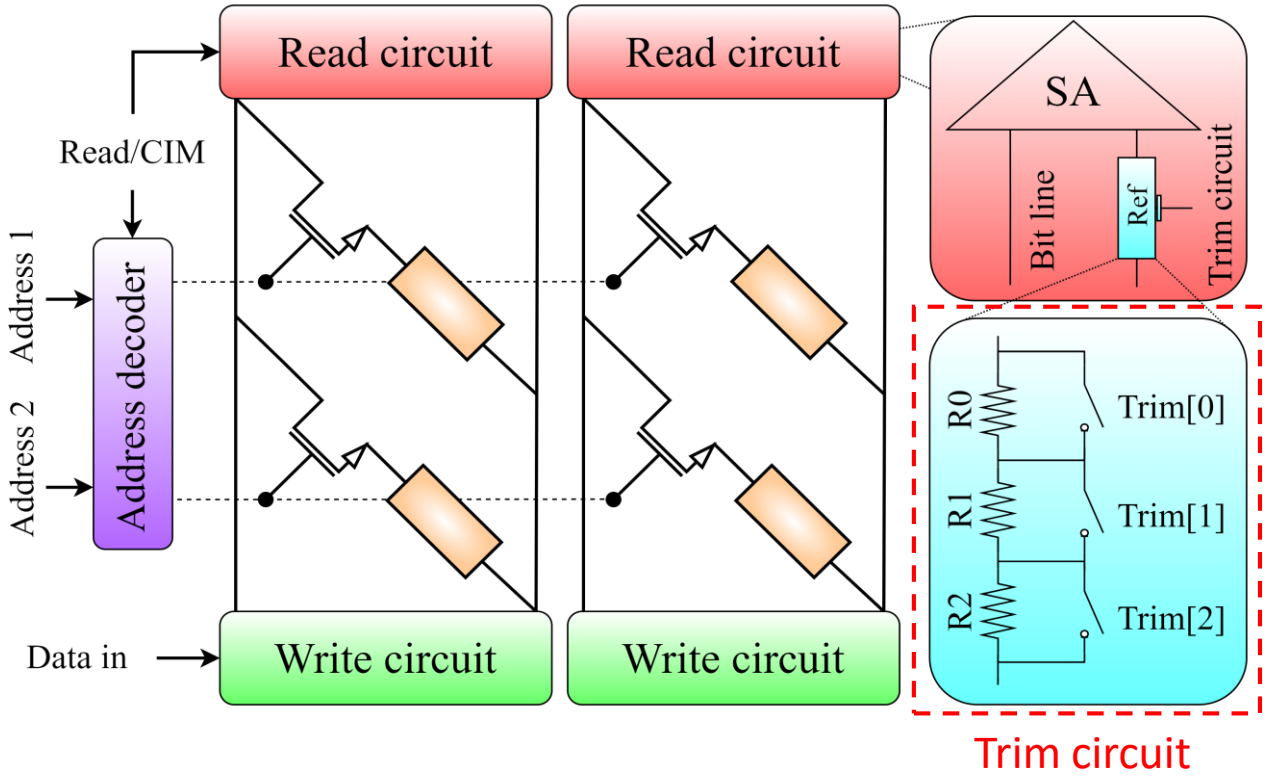
Proposed solutions

- 4-bit CIM



Reference setting





Study cases

TABLE I. CASE STUDIES

Technology	Case I (MRAM)	Case II (ReRAM)
Memory size	1Mb	1Mb
CIM type/inputs	CIM-P (2-input)	CIM-P/4-input (2-input)
Defect type/rate	Back-hopping (2ppm)	Under-formation (1ppm) & Over-formation (1ppm)
Chip-to-chip variation	5%	NA

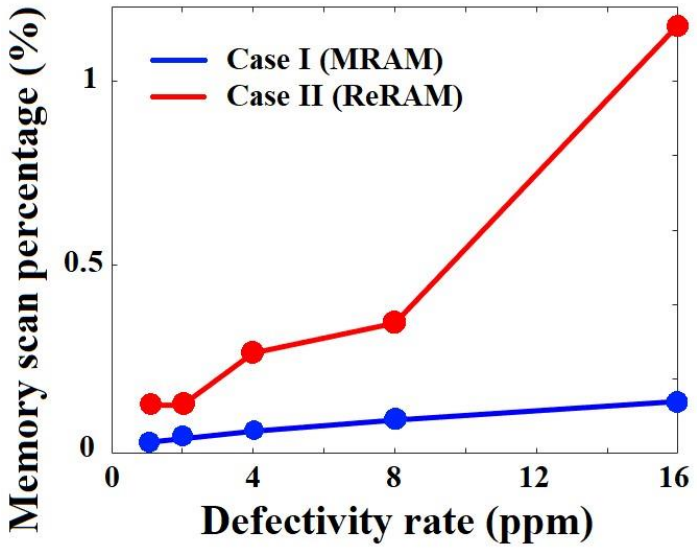
Comparative analysis

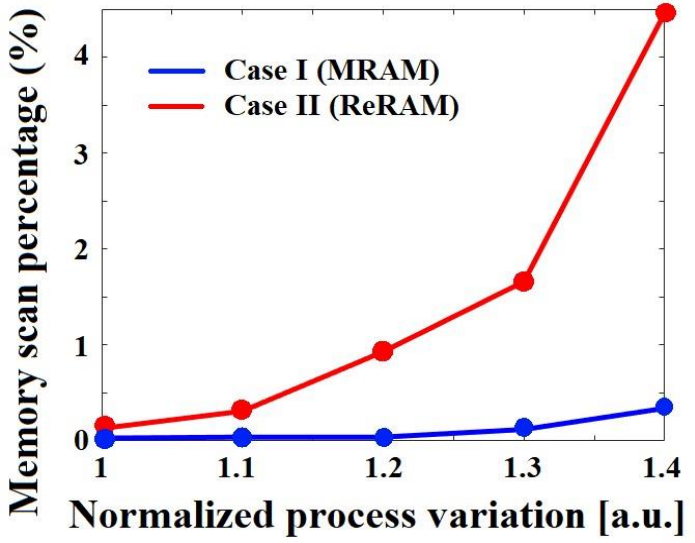
TABLE I. COMPARATIVE ANALYSIS OF TIME OVERHEAD AND REQUIRED SCAN PERCENTAGE OF DIFFERENT TEST SCHEMES

Parameter	Proposed	Münch (DATE 2021)	Nair (ETS 2021)	Tsai (DFT 2019)	Bernardi (IOLTS 2022)	March C
Test time order	$2\left(N+\frac{N}{m}\right)+(d\times m)$	$10N$+$4N$	$10N$ +$5.5N$	$12N$	$10N$+$3kN$	$10N$
Memory scan percentage for Case I	4.0×10^{-2}%	100%	100%	100%	100%	100%
Time overhead for Case I	~3.15×10^{6} cycles (m=2 & d=210)	~14.7×10^{7} cycles	~16.2×10^{7} cycles	12.6×10^{7} cycles	13.6×10^{7} cycles (k=1)	~1×10^{7} cycles
Memory scan percentage for Case II	0.13×10^{-2}%	100%	100%	100%	100%	100%
Time overhead for Case II	~2.62×10^{6} cycles (m=4 & d=348)	~14.7×10^{7} cycles	~16.2×10^{7} cycles	12.6×10^{7} cycles	13.6×10^{7} cycles (k=1)	~1×10^{7} cycles
CIM test capability	Yes	Yes	Yes	Yes	No	No

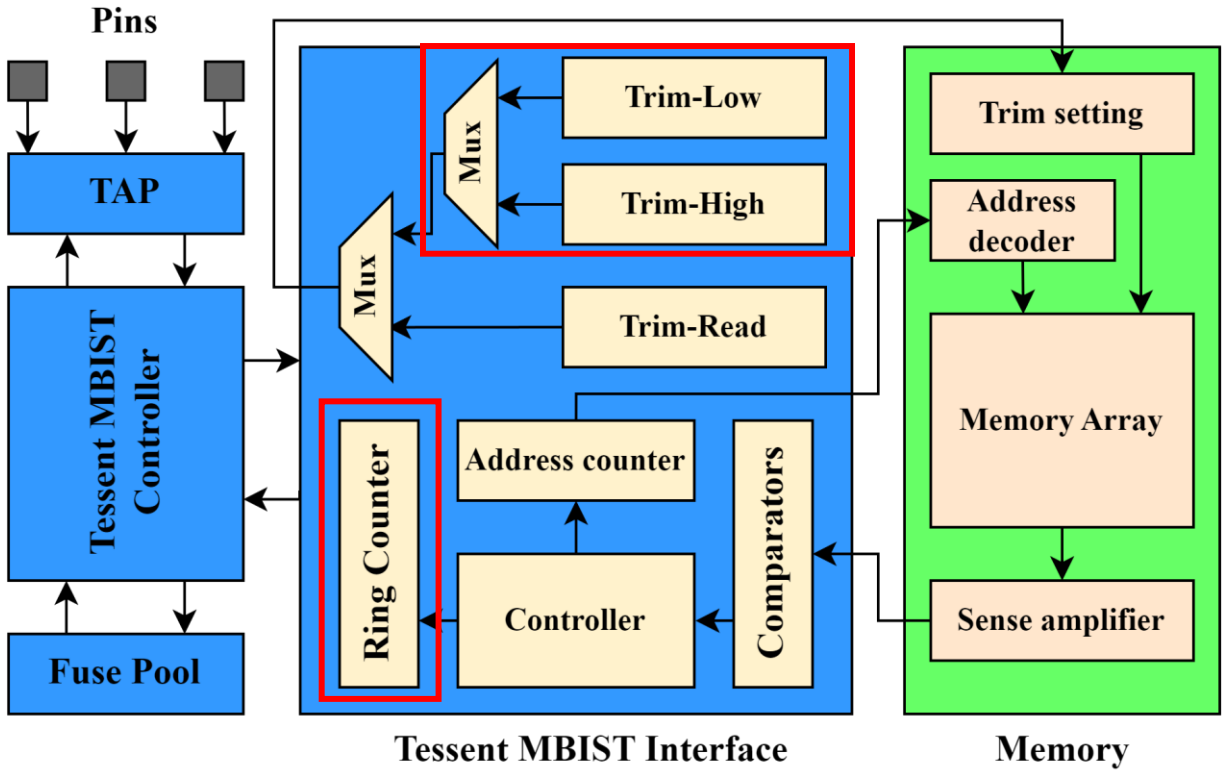
* N: # memory cells, m: # inputs for CIM operation, d: # batches that fail with Trim-Low and Trim-high settings, k: # repetitions for a subset of the test.

Defectivity rate and process variation





Integration into Siemens Tessent MBIST



Conclusion

- We proposed a dynamic test method based on the existing MBIST solution
- The proposed method uses different test resolutions based on requirements
- We achieved full test coverage while considerably lowering the cost

Thank you for your attention

Any questions?

Contact me!