Towards Automated Testing of Multiplexers in Fully Programmable Valve Array Biochips

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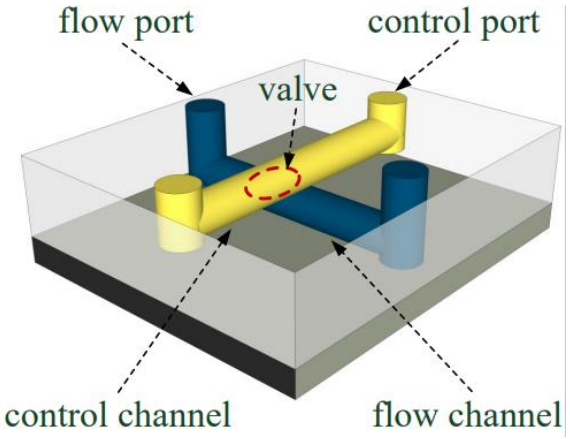
Overview

- **Background and Motivation**
- Preliminary and Problem Formulation
  - Structure of Multiplexer
  - Manufacturing Defects in FPVA Biochips
  - Fault Model
  - Single-Fault-Type Assumption
  - Problem Model
- Details of the Proposed Automated Fault Test Method
  - ILP-based ATPG Algorithm
  - Test Strategy
- Simulation Results
- Conclusion

Continuous-Flow Microfluidic Biochips

- Fundamental component: valves.
- Increasing integration level of valves.



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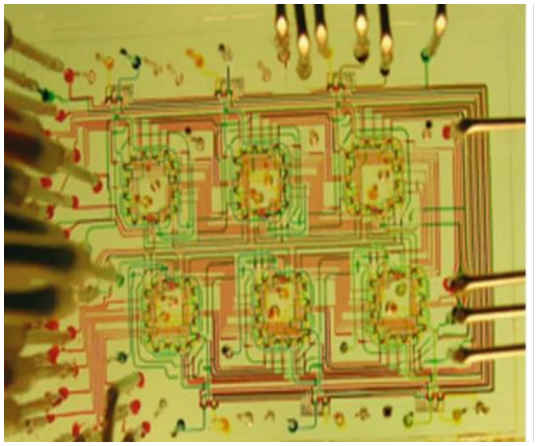

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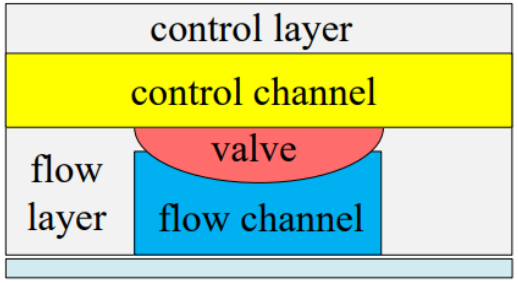

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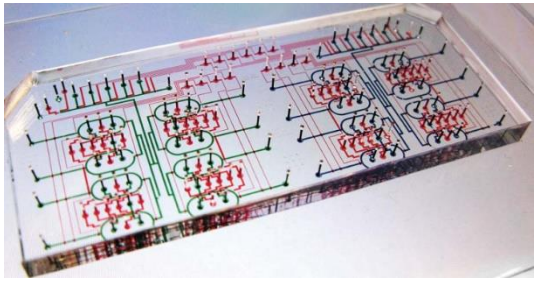

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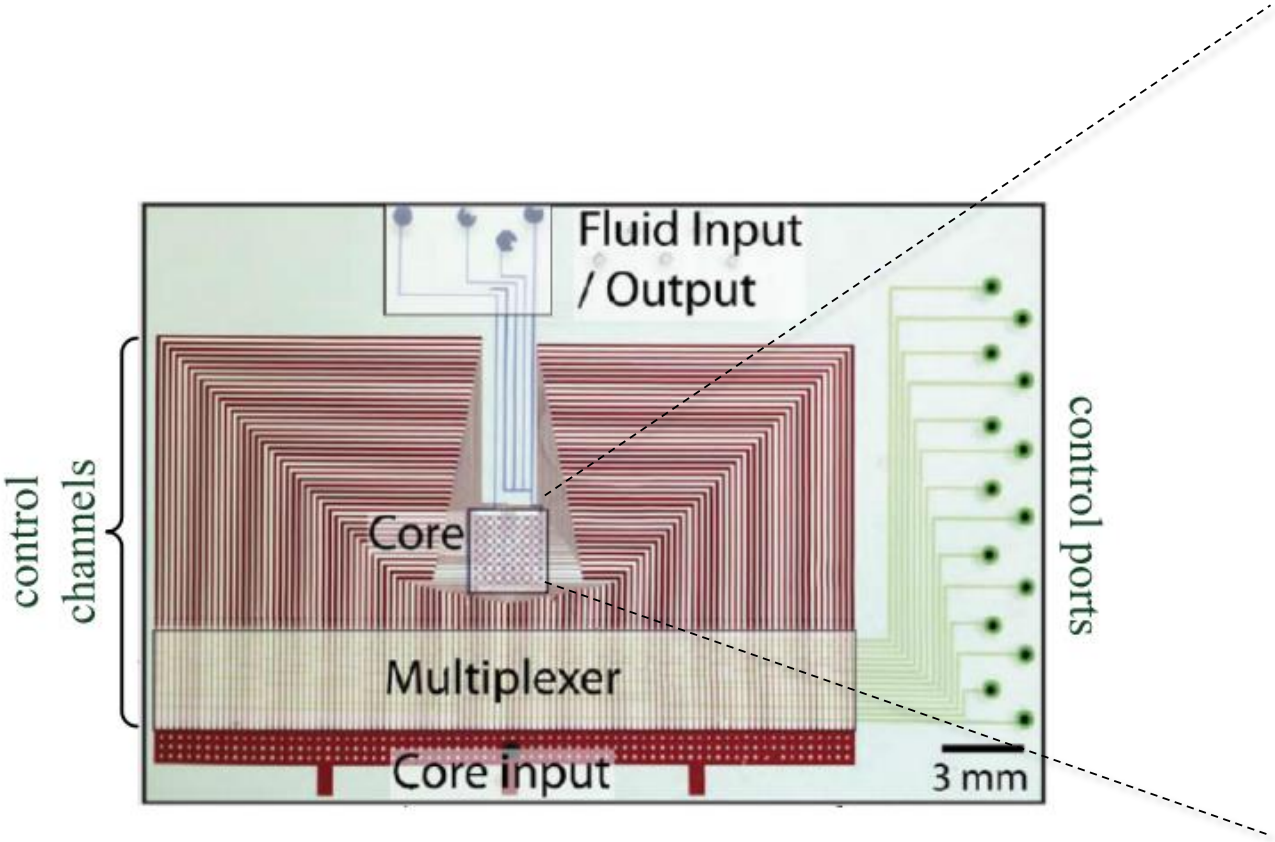
Fully Programmable Valve Array(FPVA) Biochips

The utilization of multiplexers has bolstered valve integration within FPVA Biochips.



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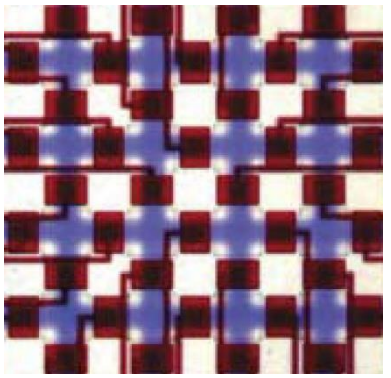

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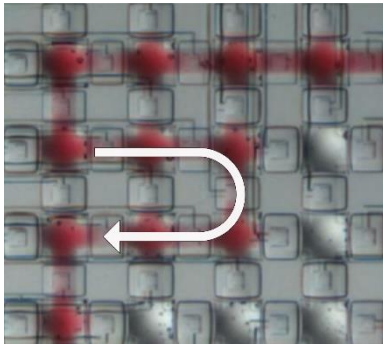

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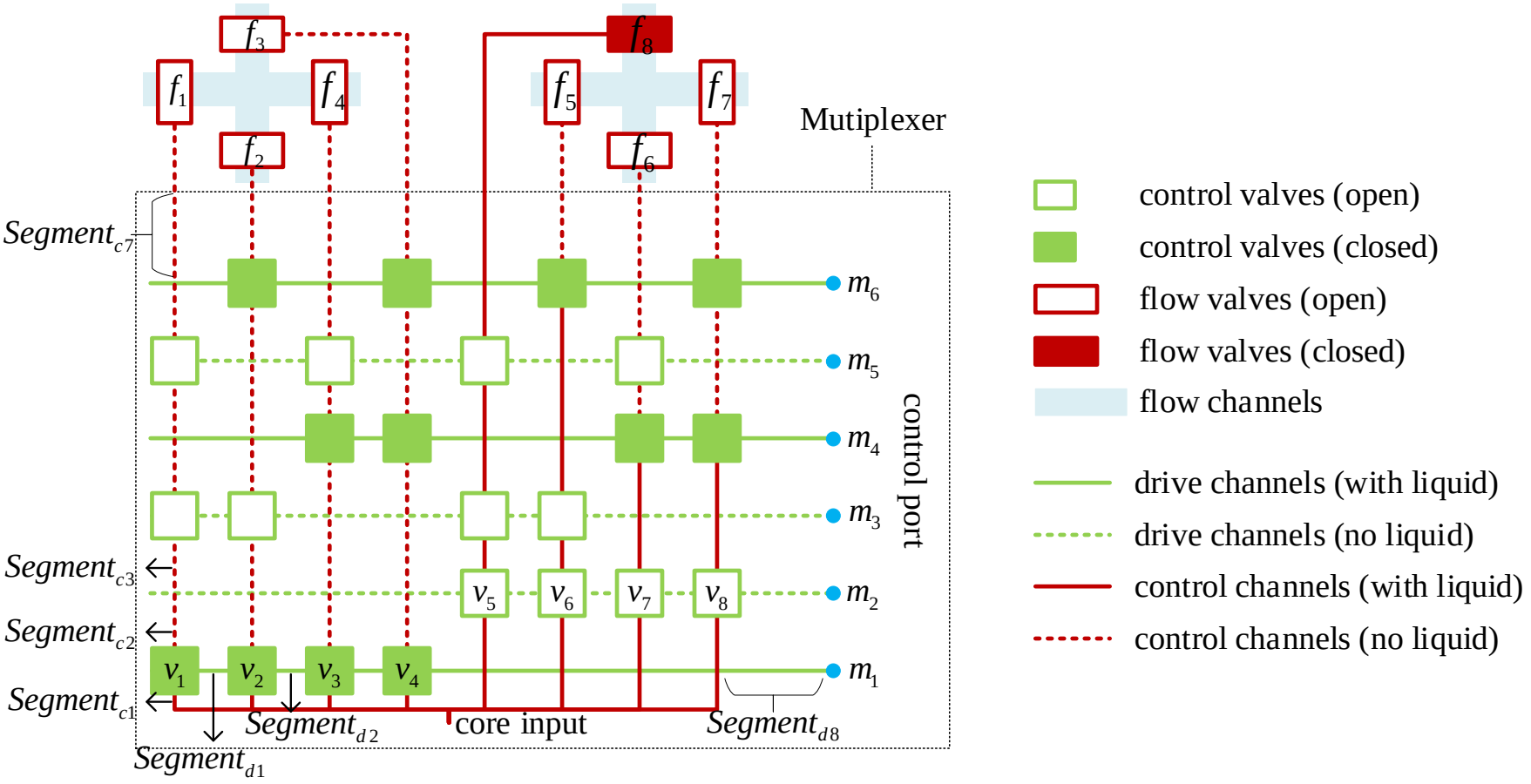
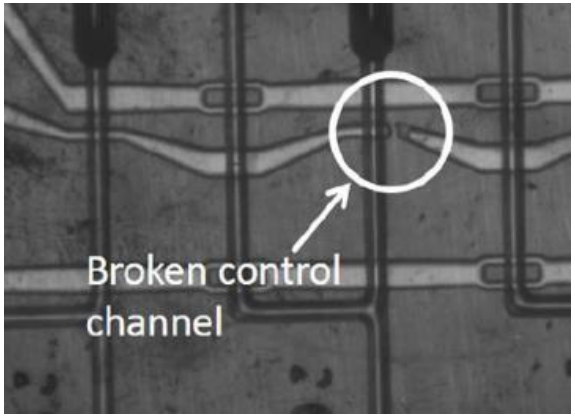
Structure of Multiplexer



- The Multiplexer's Two-Layer Structure.
- Upper Layer: The Driving Layer (Green).
- Lower Layer: The Control Layer (Red).

Manufacturing Defects in FPVA Biochips



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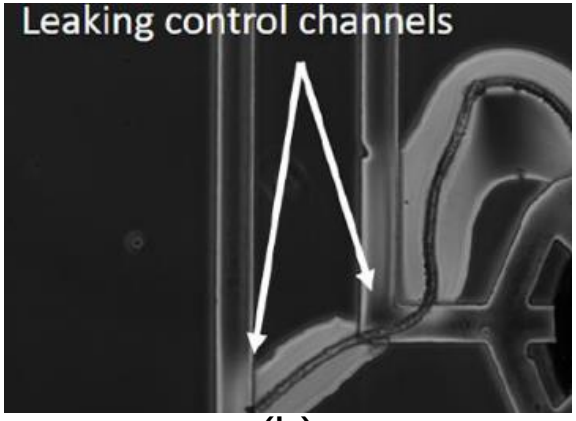

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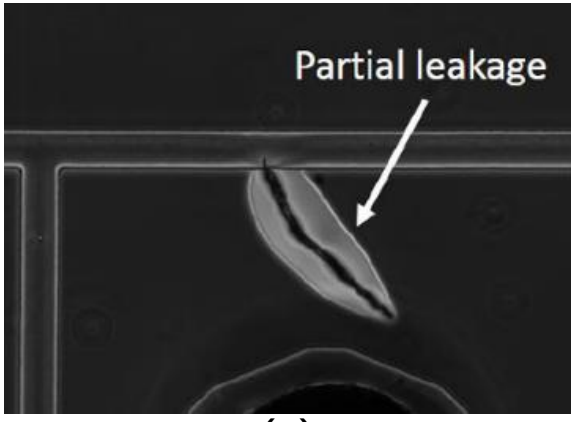

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(d)

Throughout the manufacturing and operational phases, FPVA biochips may experience physical defects. [*K. Hu et al., 2014*]

Fault Model

Five categories：

- Control channel blockage
- Control channel leakage
- Drive channel blockage
- Drive channel leakage
- Valve elastic degradation

Fault Model

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- **Control channel blockage**
- Control channel leakage
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- Drive channel leakage
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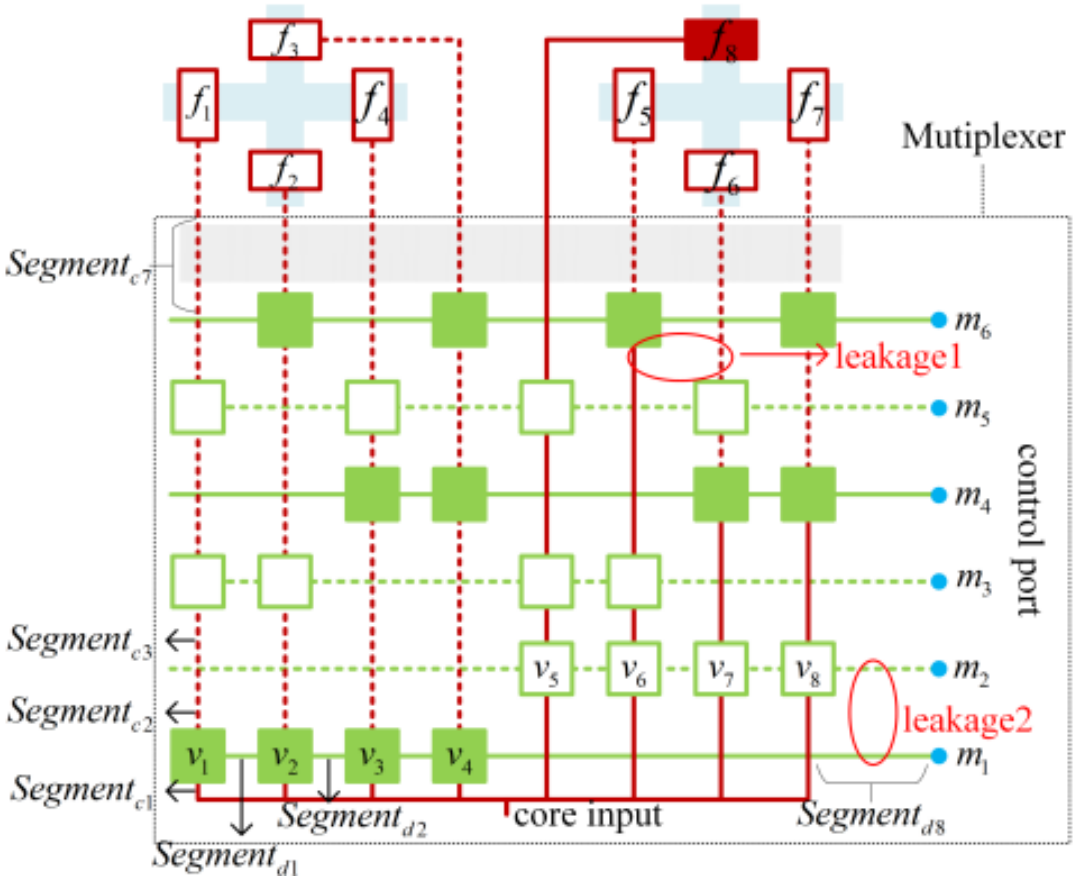

Single-Fault-Type Assumption

- **Assumption:**

  A chip will rarely contain multiple fault types, but the same type of fault may occur multiple times in a layer.

- **Because:**

  - The root cause of a fault typically leads to the occurrence of the same type of fault.
  - Since the layers of a multiplexer are manufactured independently, there will be no interlayer faults.

  [*K. Hu et al., 2015*]

Problem Model

- Based on the time division concept, we divide the execution process of a test pattern into four parts: “drive delay”, “filling delay”, “leakage delay” and “refresh delay”.

- **Given:** The structure of a multiplexer.
- **Output:** A set of test patterns.
- **Objective:** Minimizing the number of test patterns.
- **Subject to:** The generated test pattern combinations can cover all the possible positions of the above five types of faults in the multiplexer, i.e., achieving 100% fault coverage.

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ILP-based ATPG Algorithm

- Formulate **Integer Linear Programming(ILP)** models for the five types of faults mentioned above.
- To achieve 100% fault coverage, we must ensure that n_p test patterns can cover each potential fault location at least once.

$$\sum_{m=1}^{n_p} bd_j^m \geq 1, j \in C_d \qquad \sum_{m=1}^{n_p} lc_{i,j}^m \geq 1, (i,j) \in G_c$$

$$\sum_{m=1}^{n_p} ld_j^m \geq 1, j \in G_d \qquad \sum_{m=1}^{n_p} ec_{i,j}^m \geq 1, (i,j) \in V$$

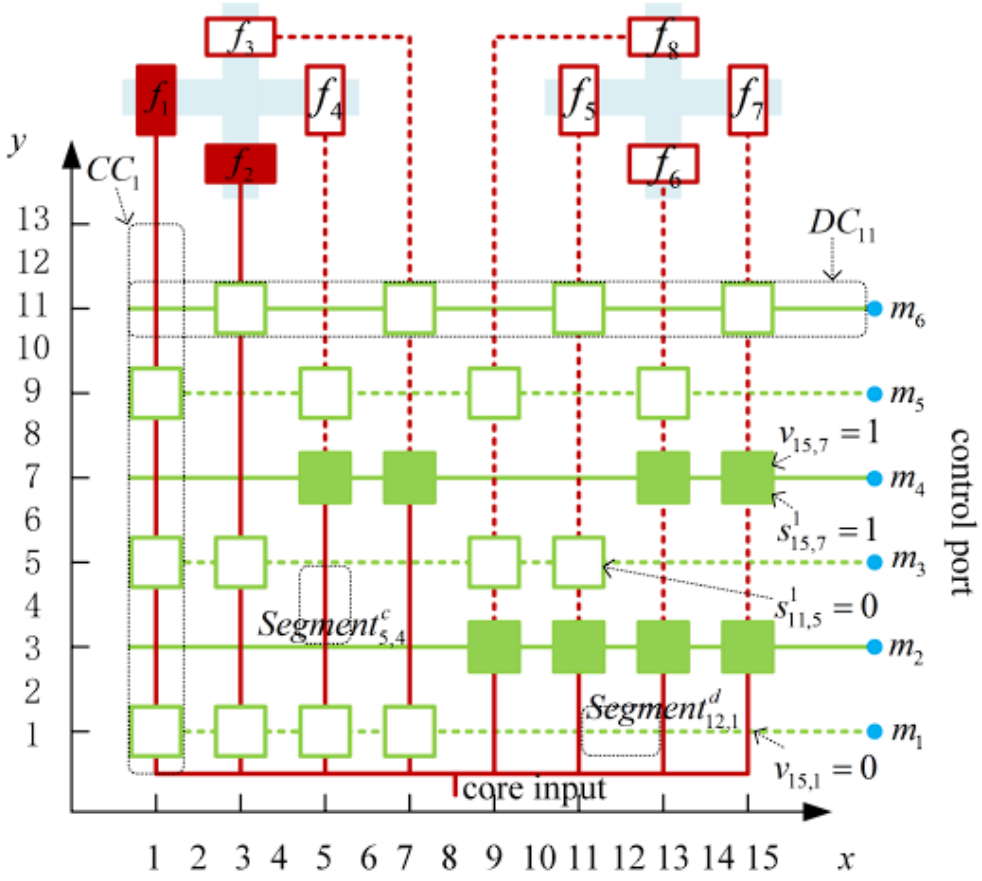
$$\sum_{m=1}^{n_p} bc_i^m \geq 1, i \in C_c$$

- The proposed ILP model aims to identify a test pattern combination with the minimal quantity.

$$minimize \sum_{m=1}^{n_p} p_m$$

ILP-based ATPG Algorithm

- For example:
  - Test patterns generation.



$$s'''_{i,k} = s'''_{j,k}, \quad \forall s_{i,k}, s_{j,k} \in S, m = 1, 2, \ldots, n_p$$

Test Strategy

We divide the execution process of a test pattern into four steps during the test process of the multiplexer.

- **Step1:** Inject colorless gas and close corresponding control valves.

- **Step2:** Inject ample colored gas into control channels and close the core input to contain the gas within those channels.

- **Step3:** Maintain closed control ports and core input to enable complete gas leakage to the external environment over time.

- **Step4:** Open control ports and core input to release channel gas. Replace colored gas with colorless in control channels to avoid impacting next test execution.

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Simulation Results

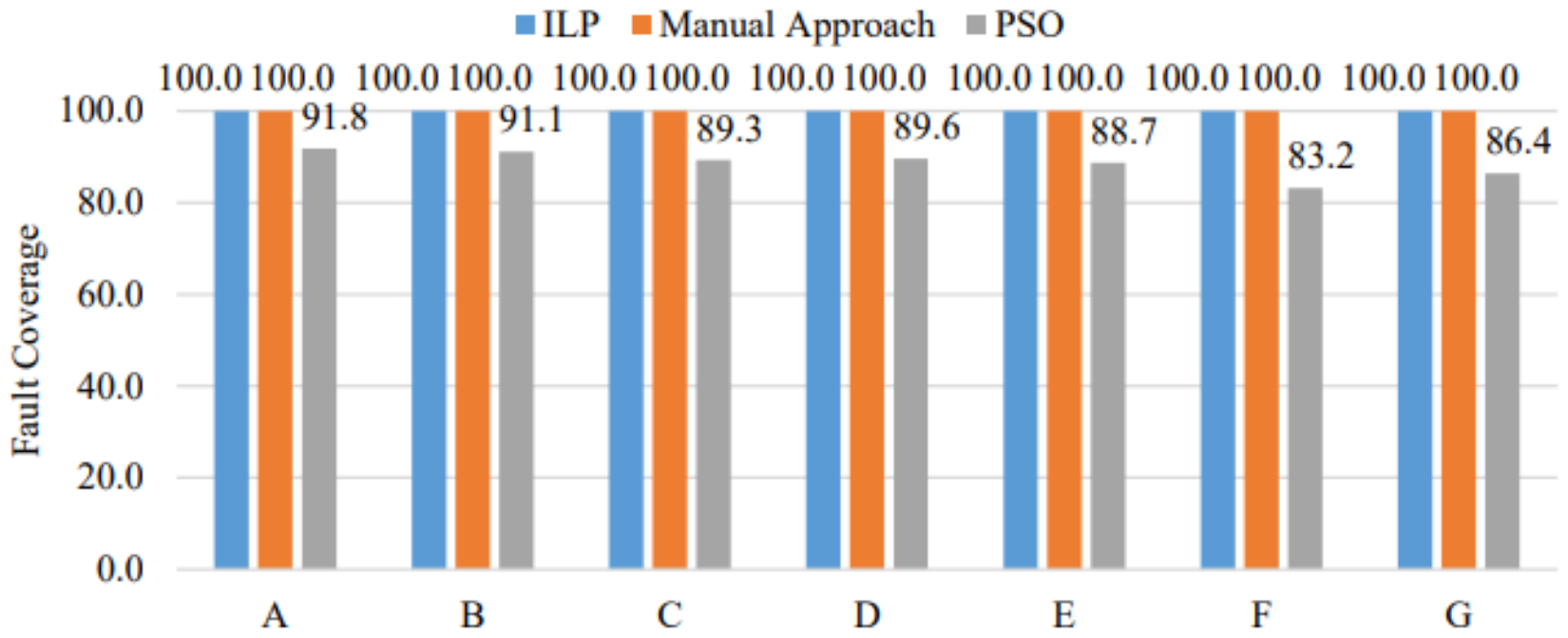
Comparison results of execution time and number of test patterns.

Multiplexer				ILP			Manual Method		Imp(%)		PSO		Imp(%)	
Bench	n^v	n^d	n^c	n^p	n^t	$t(s)$	n^t	$t(s)$	n^t	t	n^t	$t(s)$	n^t	t
A	24	6	8	6	5	2.1	8	-	37.5	-	5	19.2	0.0	89.2
B	36	8	9	8	7	7.7	9	-	22.2	-	8	40.6	12.5	81.0
C	64	8	9	8	7	17.3	16	-	56.3	-	10	63.8	30.0	72.9
D	105	10	21	10	8	142.6	21	-	61.9	-	17	93.1	52.9	-53.3
E	160	10	32	16	9	1800.0	32	-	71.9	-	19	128.4	52.6	-1301.5
F	246	12	41	20	12	1800.0	41	-	70.7	-	21	178.7	42.9	-907.0
G	384	12	64	32	20	1800.0	64	-	68.8	-	41	181.6	51.2	-891.2

- n^v: The number of control valves;
- n^d: The number of drive channels;
- n^c: The number of control channels;
- n^c: The number of control channels;
- n^p: A constant, used to limit the maximum number of test patterns;
- n^t: The number of test patterns generated by the algorithm;
- t : The time used to generate test patterns;
- - : Time is difficult to estimate.

Simulation Results

Comparison results of fault coverage.



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Conclusion

- We propose an ILP-based automated test pattern generation(ATPG) algorithm.
- We propose an automatic testing strategy for multiplexers.
- The proposed ILP-based algorithm can generate fewer test patterns in a reasonable time and achieve 100% fault coverage.

Thank you for your attention!