Reinforcing the Connection between Analog Design and EDA

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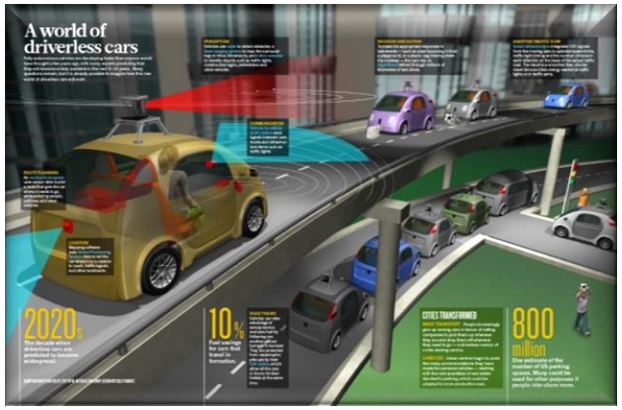
Driven to Discover®

The need for analog design automation

Demand

- The real world is analog, but processing is (largely) digital
- At the very least, need A2D conversion
  - Maybe a lot more – in-sensor computing, RF, …



[Waldrop, Nature]

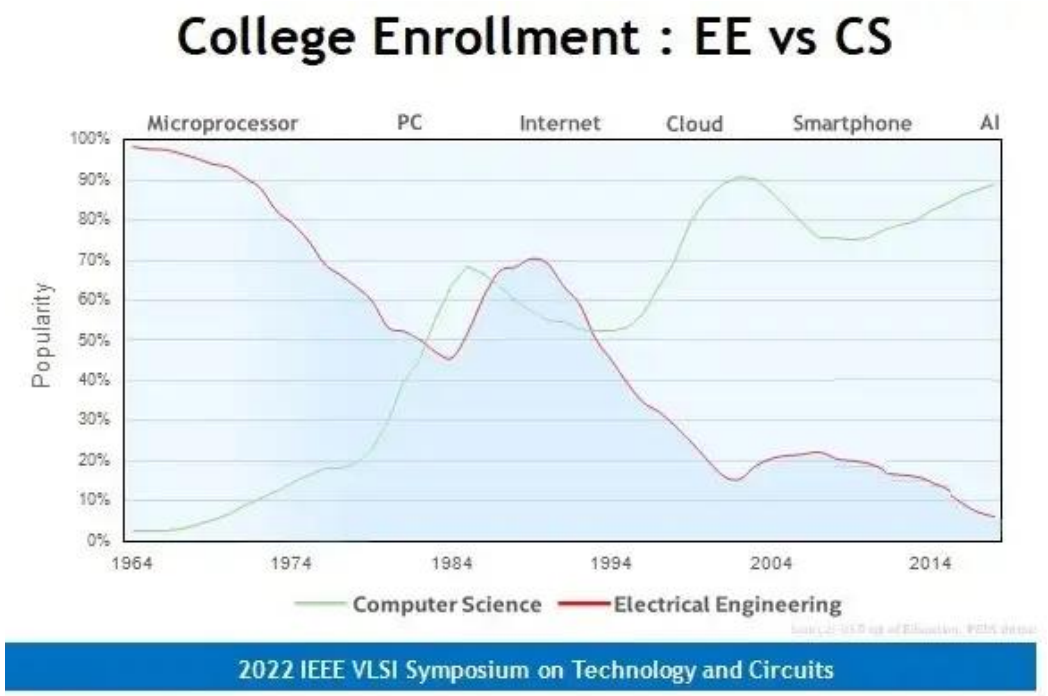
[http://adtellintegration.com]

EDA360 Insider

70% of re-spin issues are AMS in nature: How mixed-signal design can mess up a perfectly good SoC

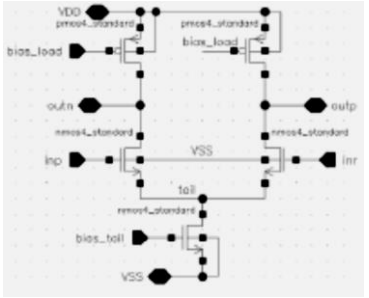
Supply

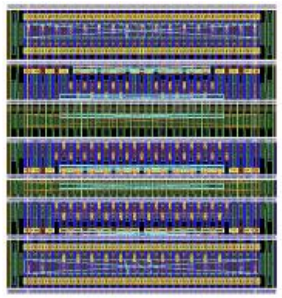
- Finding designers is hard
- Finding analog designers is harder



Analog layout automation: A quick history

- Procedure-based
  - Generate layouts based on pre-designed templates in a procedural approach
    - Tends to be circuit specific, extensive designer input/setup
  - Examples
    - Switched-capacitor circuit capacitors [Yaghutiel 1988]
    - Voltage reference / opamps [Rijmenants JSSC 1989]
    - SAR ADCs [Wulff JSSC 2017]
    - BAG2: able to traverse multiple hierarchies





```
class DiffAmp(SerdesRXBase):
    def __init__(self, temp_db, lib_name, params, used_names, **kwargs):...
    def draw_layout(self):
        # ...
        self.draw_base(lch, fg_tot, ptap_w, ntap_w, nw_list, nth_list,
                       pw_list, pth_list, ng_tracks=ng_tracks,
                       nds_tracks=nds_tracks, pg_tracks=pg_tracks,
                       pds_tracks=pds_tracks, n_orientations=n_orient,
                       p_orientations=p_orient, **kwargs)

        mp_wires = self.draw_mos_conn('nch', 1, col_inp, n_in, sdir, ddir)
        mn_wires = self.draw_mos_conn('nch', 1, col_inn, n_in, sdir, ddir)
        # ...
        inp_wires = self.connect_to_tracks(mp_wires['g'], wire_layer, inp_tidx)
        inn_wires = self.connect_to_tracks(mn_wires['g'], wire_layer, inp_tidx)
        self.add_pin('INP', inp_wires)
        self.add_pin('INN', inn_wires)
        # ...
```

(c) Layout Generator (XBase).

- Optimization-based [Cohn, JSSC 1991; Gielen, Proc. IEEE 2000]
  - Formulate the layout problem as constrained optimization program
  - Often stochastic based algorithms
  - Challenging to guarantee “tapeout” quality

- Various research groups active in this area
  - TU Munich (Helmut Graeb)
  - UT Austin/MAGICAL (David Pan)
  - NTU (Mark Lin)
  - KU Leuven (Georges Gielen)
  - IST Sevilla
  - Boğaziçi University (Günhan Dündar)
  - etc.

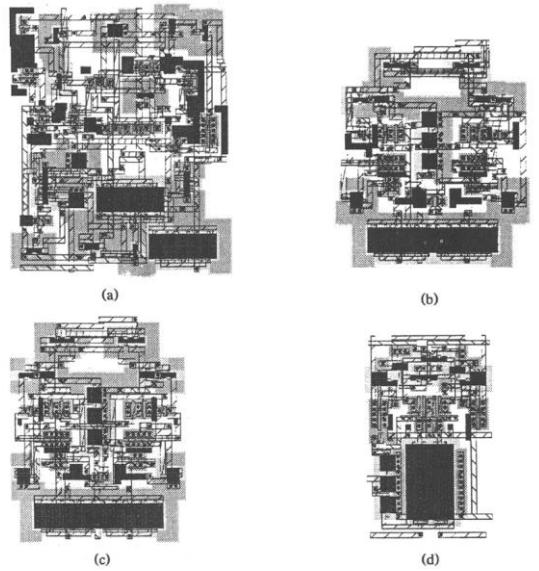


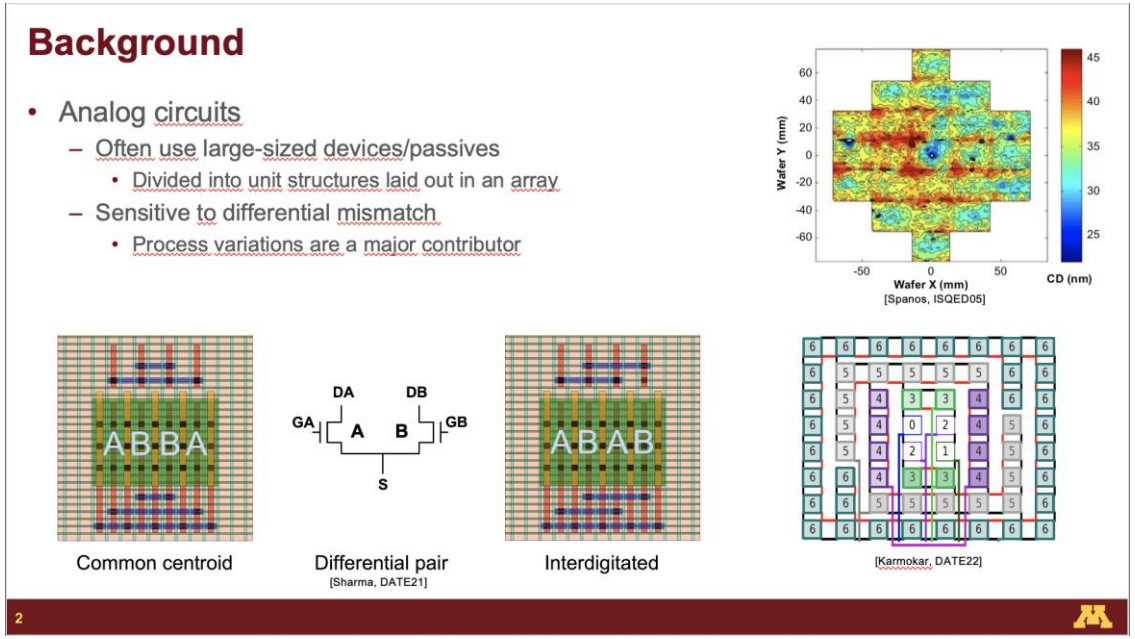
Fig. 8. CMOS comparator layouts. (a) Automatic layout with no placement or routing optimization. (b) Automatic layout with placement optimization only. (c) Automatic layout with both placement and routing optimization. (d) Manual layout.

3

Limitations of prior efforts

Link to process?

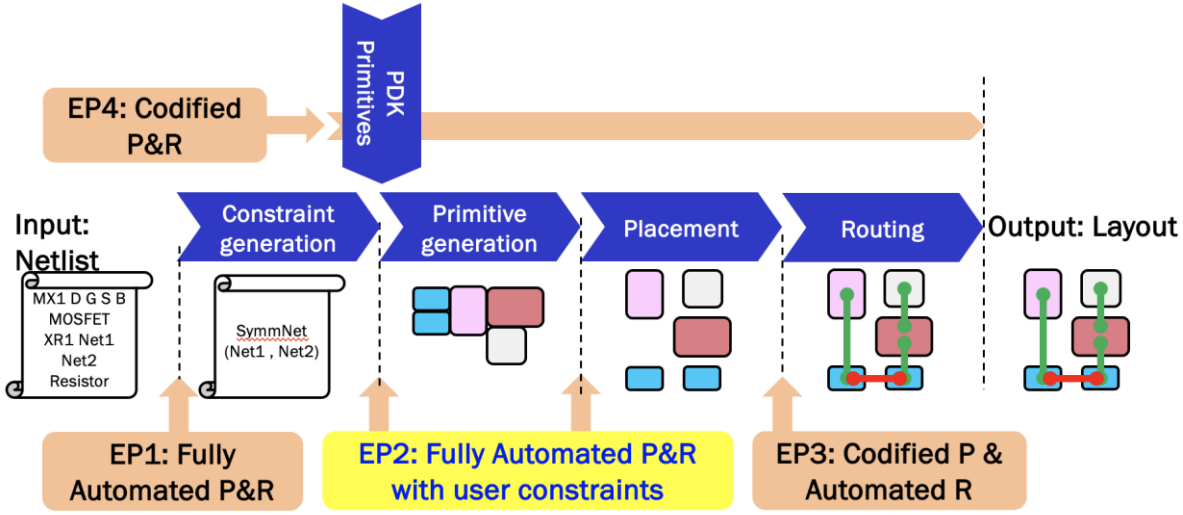
- Many conventional assumptions, which are unquestioned
- Lack of support from publicly-available measured data



[From our ASPDAC22 talk]

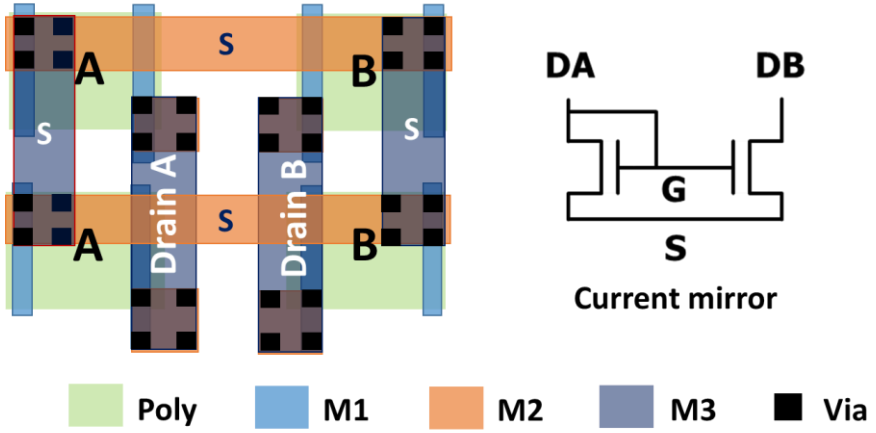
Link to the designer?

- Incorporating designer input critical
- EDA tools try to “automate it all”: this will not win over designers
- Need to support
  - Designer input
  - Designer-driven design-space exploration

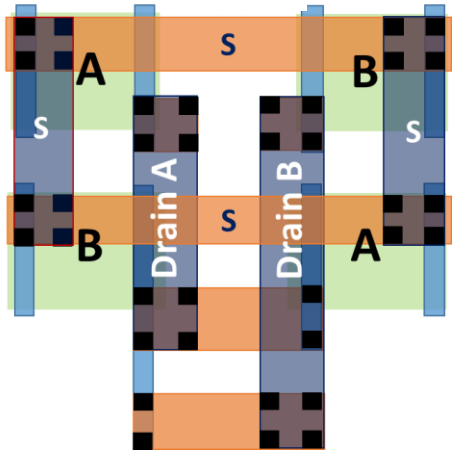


Motivation: Layout Design

Clustered (NonCC)



Common-centroid (CC)



CC requires ~20% more area even for an array with only 2 devices

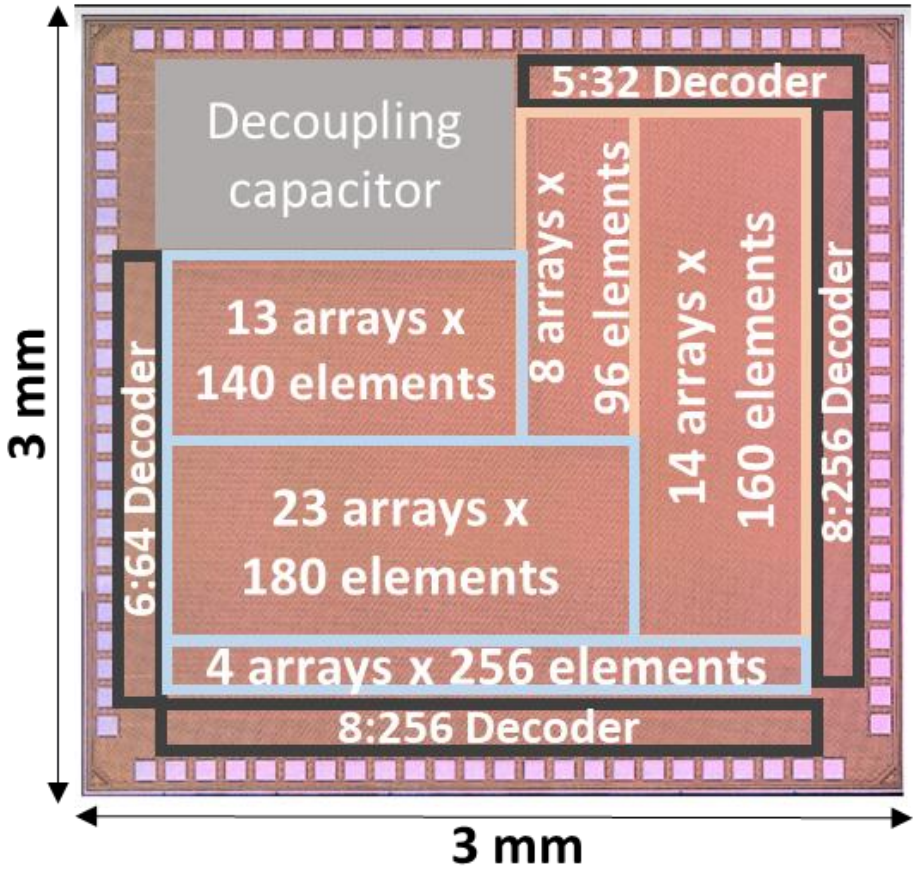
	NonCC	CC
Routing parasitics	✓	✗
Layout area	✓	✗
Layout time	✓	✗
Differential mismatch	✗ (?)	✓ (?)

- Designers often resort to CC to reduce distance-dependent variations
- CC (especially in FinFET technologies) has larger routing parasitics and area
- Distance-dependent variation models can convey whether or not CC is needed

[Madhusudan, ESSDERC23]

5

Test Chip

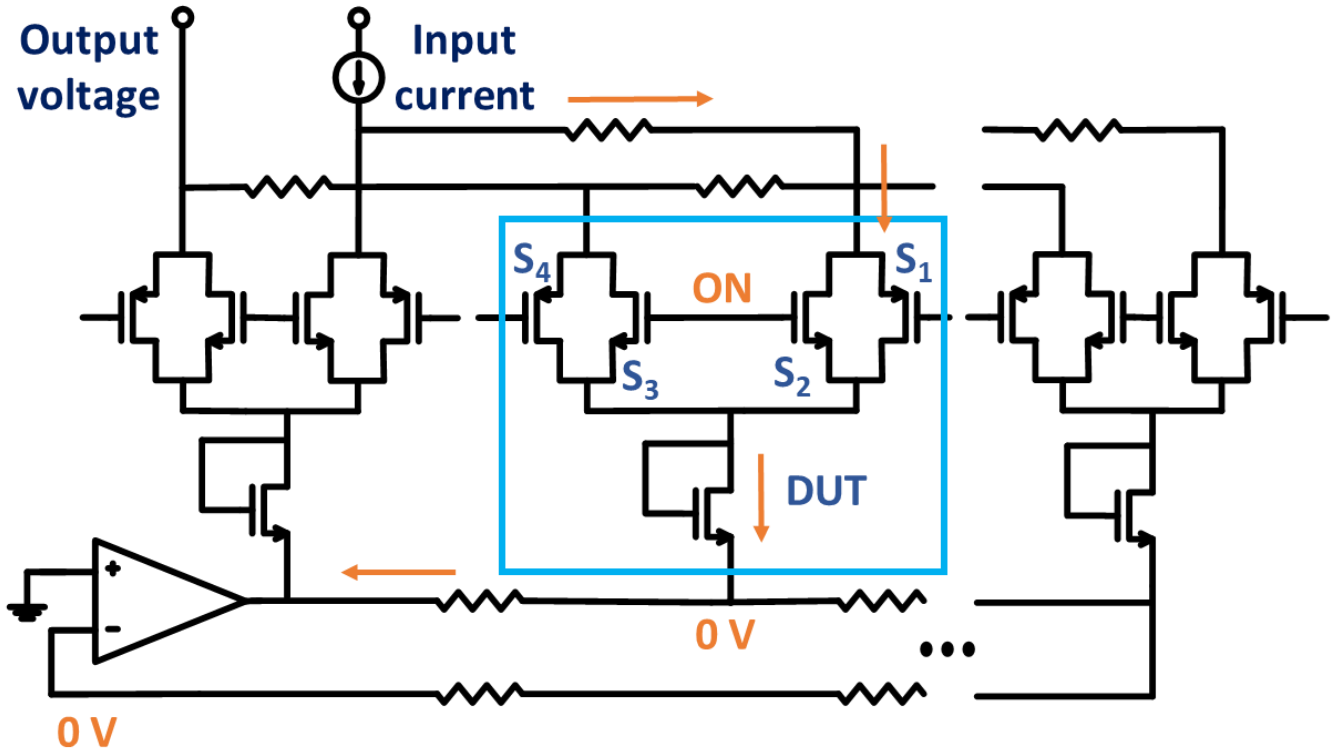


- Measured 195,904 devices across 30 dies on a 3mm x 3mm die area in 12nm FinFET
- Modeled distance-dependent variations and their impact on CC and NonCC layouts
- Applied findings to DAC design to reduce area, parasitics, and complexity

[Madhusudan, ESSDERC23]

6

Test Chip: Design



At constant current, V_{GS} of each DUT depends on its V_{TH} and β

- DUT has low random variations with W/L=1150nm/280nm ($240 \cdot WL_{MIN}$)
- DUT is measured at 4 currents in strong inversion with V_{OV} = 200 mV
- Source voltage is not affected by parasitics using OTA with feedback [TSM 2001]

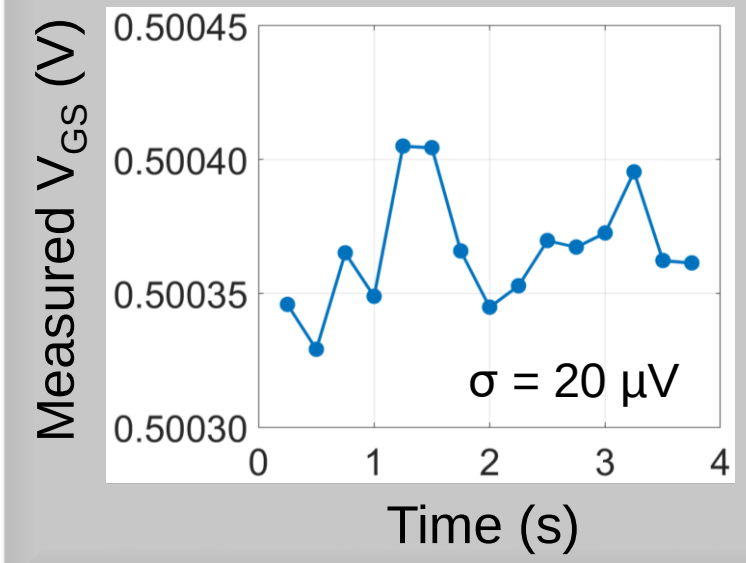
[Madhusudan, ESSDERC23]

7

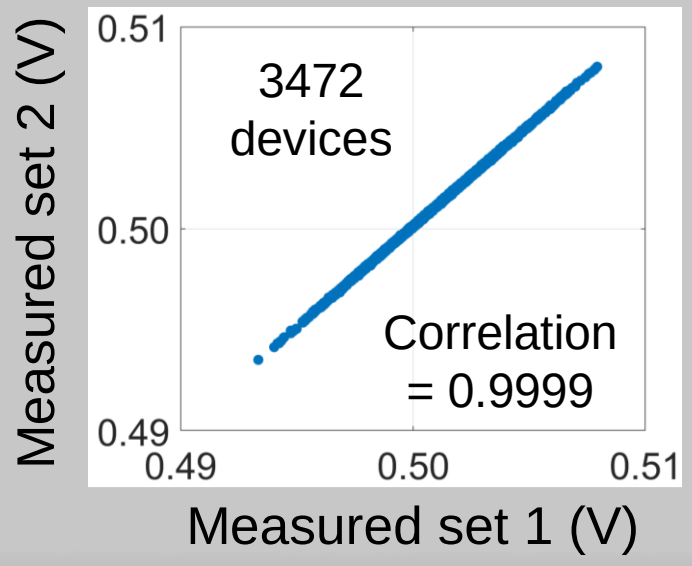
Measurement: Validation

- σ is low for multiple measurements of same DUT
- DUT relationships are highly correlated when measured on different days
- DUT obeys the square-law relationship between I_D and V_{GS}

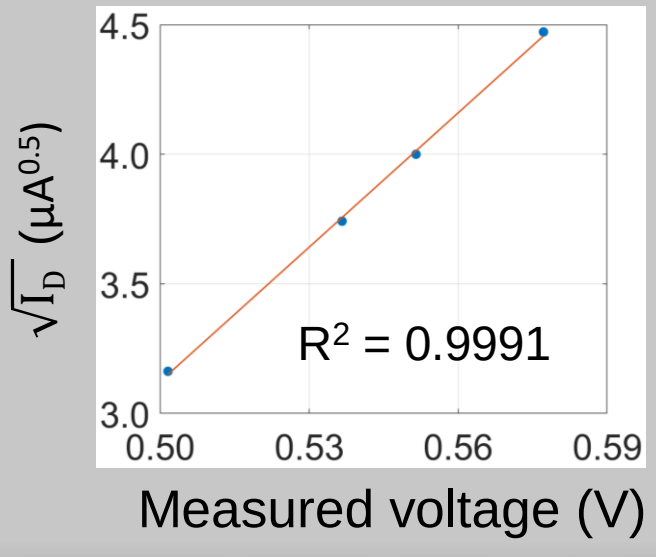
Noise impact



Repeatability



Square-law validity

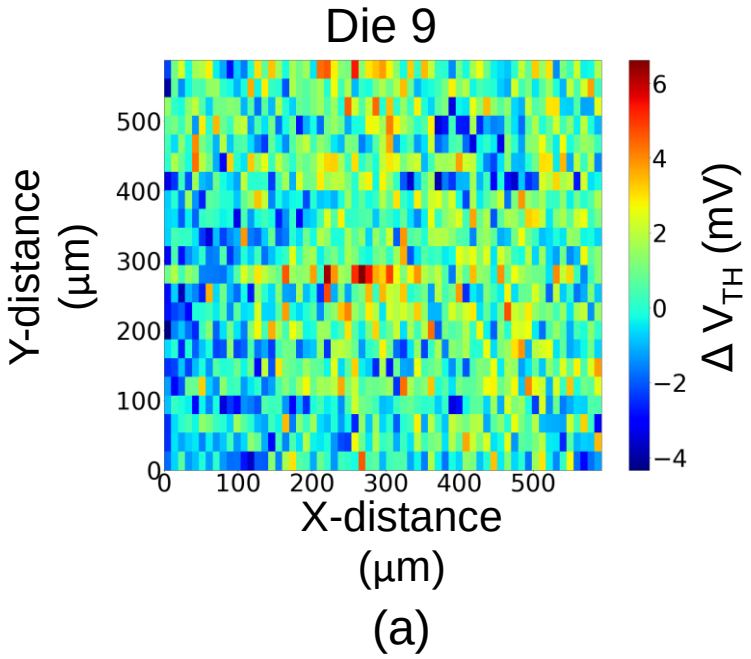


[Madhusudan, ESSDERC23]

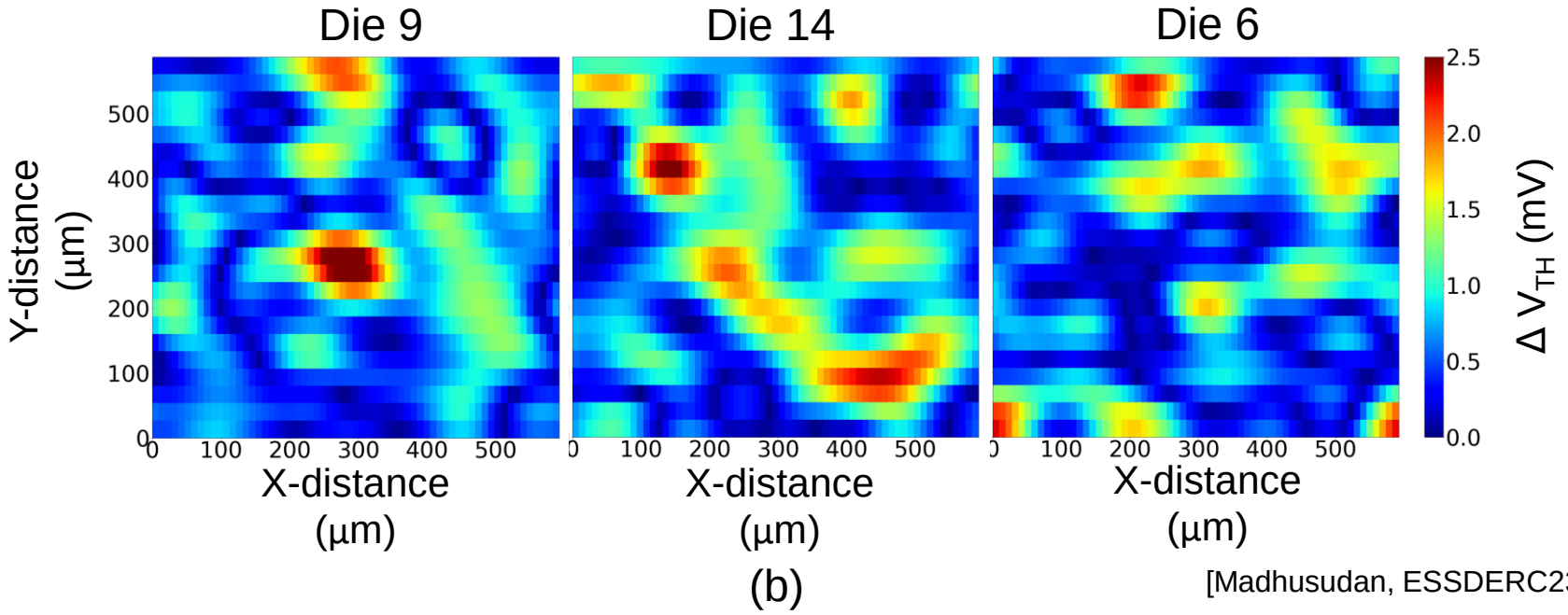
8

Measurement: ΔV_{TH} Surface

- In (a), high frequency changes convey that random variations are high
  - Even though the device size is large ($240 \cdot WL_{MIN}$)
- In (b), distance-dependent changes are observed after low pass filtering
  - Spatially correlated regions that are different on each die (not linear)



(a)

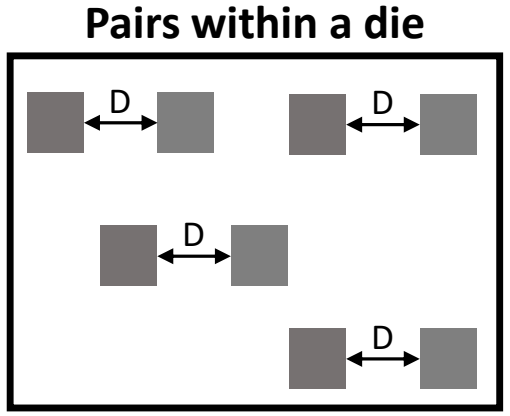


(b)

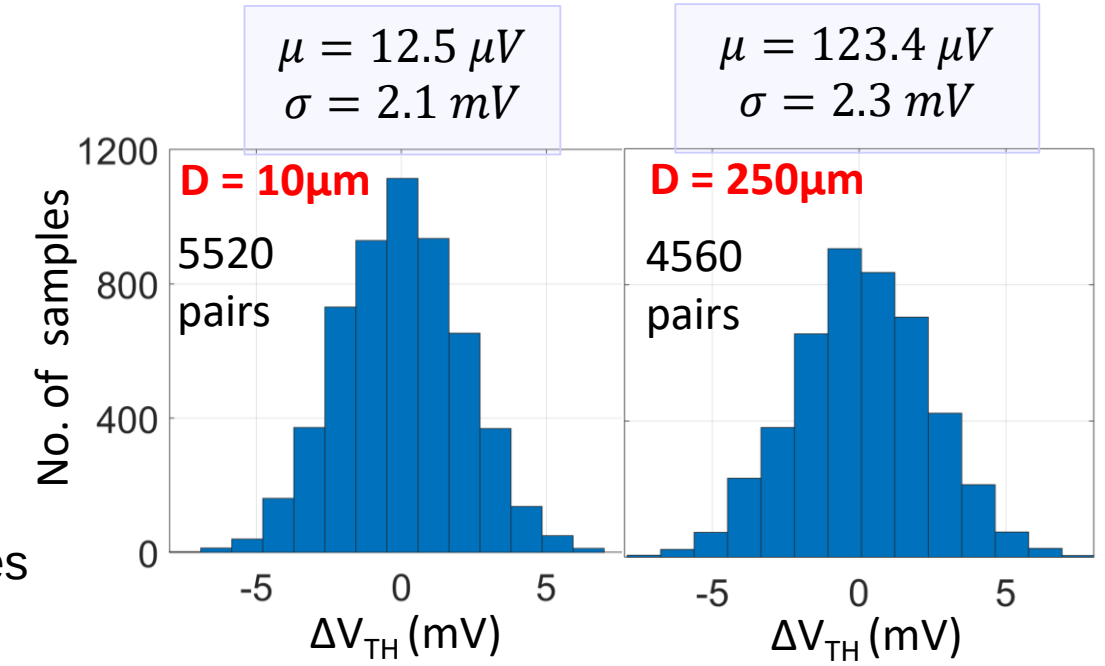
[Madhusudan, ESSDERC23]

9

Measurement: ΔV_{TH} Variations



ΔV_{TH} between pairs of devices separated by D

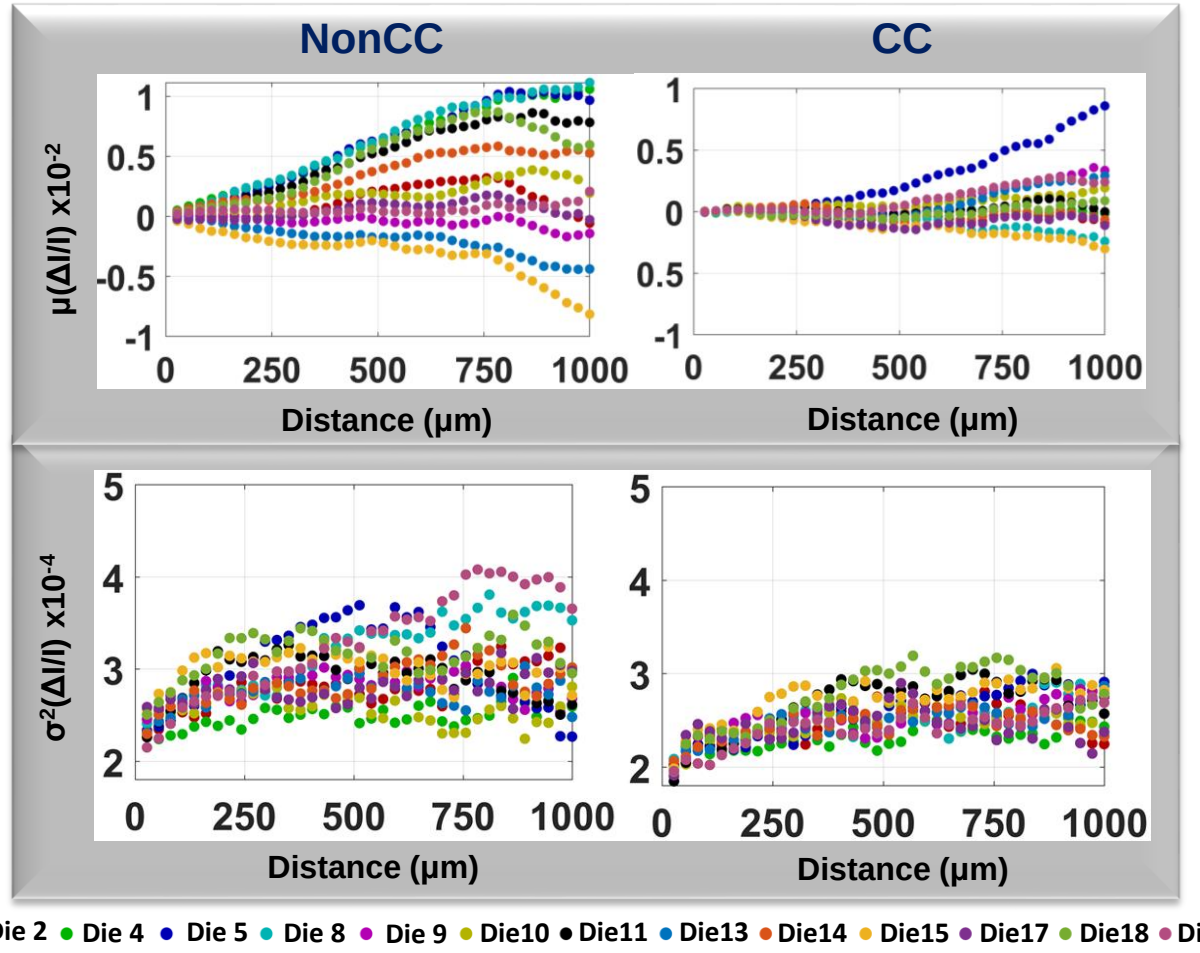


- At D = 10 µm, random variations dominate and µ ≈ 0 and σ ≈ σ_{RANDOM}
- At D = 250 µm, µ + σ ≈ σ_{RANDOM} + 15%, even though σ_{RANDOM} is low (large device)
- Distance-dependent variations are small compared to random variations

[Madhusudan, ESSDERC23]

10

Modeling: Variations on multiple die

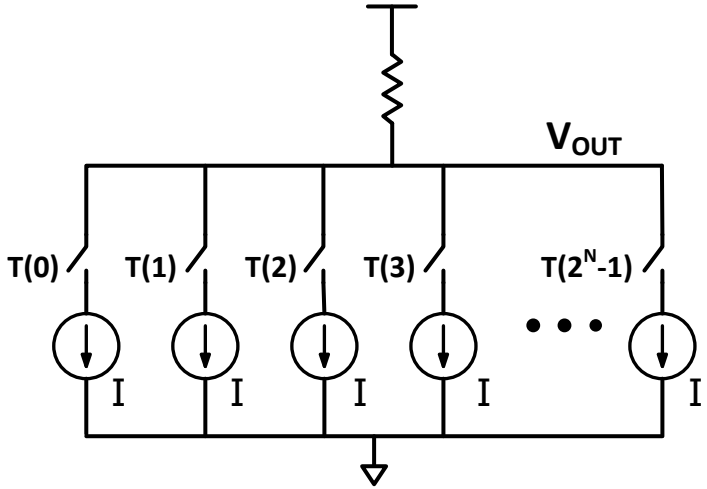


- Variations on 13 out of 30 die
  - > 5,000 pairs at each point
- At smaller distances, μ and σ of NonCC and CC are comparable
- CC does not cancel all distance-dependent variations

[Madhusudan, ESSDERC23]

11

Application: Unary DAC Design



Current source sizing:

$$\sigma^2(\Delta I/I)_{SPEC} = \sigma^2(\Delta I/I)_{RANDOM} + \sigma^2(\Delta I/I)_{D-D}$$

- Design procedure for W/L
  1. Use $\sigma^2(\Delta I/I)_{SPEC} = \sigma^2(\Delta I/I)_{RANDOM}$ → to find approximate layout area
  2. From estimated area → Find $\sigma^2(\Delta I/I)_{D-D}$
  3. From spec and $\sigma^2(\Delta I/I)_{D-D}$ → Find the new $\sigma^2(\Delta I/I)_{RANDOM}$
  4. From new $\sigma^2(\Delta I/I)_{RANDOM}$ → Find the device size (WL)
  5. From no. of bits and WL → Estimate layout area

[Madhusudan, ESSDERC23]

12

Application: Unary DAC Design

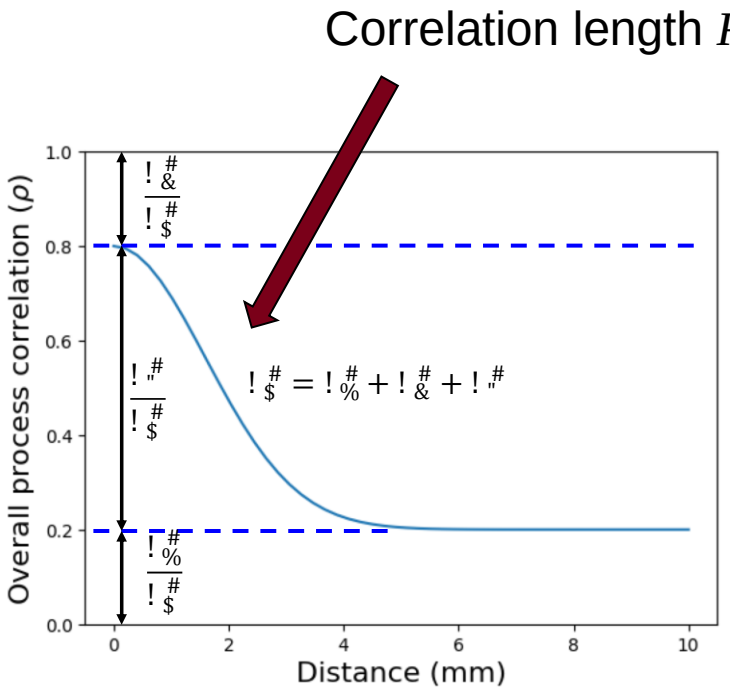
- NonCC can meet specifications for a lower layout area even in 6-bit
- NonCC cannot meet specifications in a 10-bit DAC
- Distance-dependent component cannot be neglected even for CC in 10-bit DAC

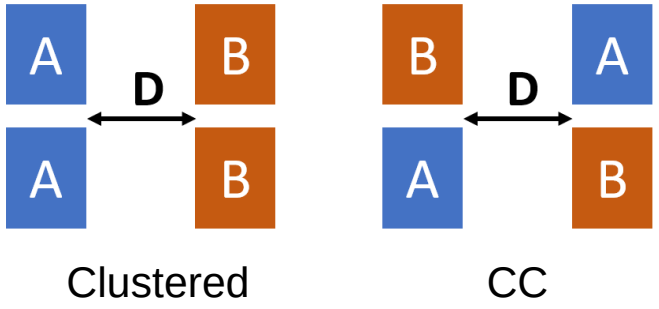
Step	Parameter	6-bit DAC		8–bit DAC		10-bit DAC	
		NonCC	CC	NonCC	CC	NonCC	CC
	$\sigma^2(\Delta I/I)_{SPEC}(10^{-4})$	8.87		2.22		0.55	
1+2	$\sigma^2(\Delta I/I)_{D-D}(10^{-4})$	0.4	0	0.6	0.2	0.9	0.3
3	$\sigma^2(\Delta I/I)_{RANDOM}(10^{-4})$	8.47	8.87	1.62	2.02	-	0.25
4	Device WL (μm^2)	0.162	0.155	0.849	0.680	-	5.50
5	Total layout area (μm^2)	230	306	2958	3418	-	80800

[Madhusudan, ESSDERC23]

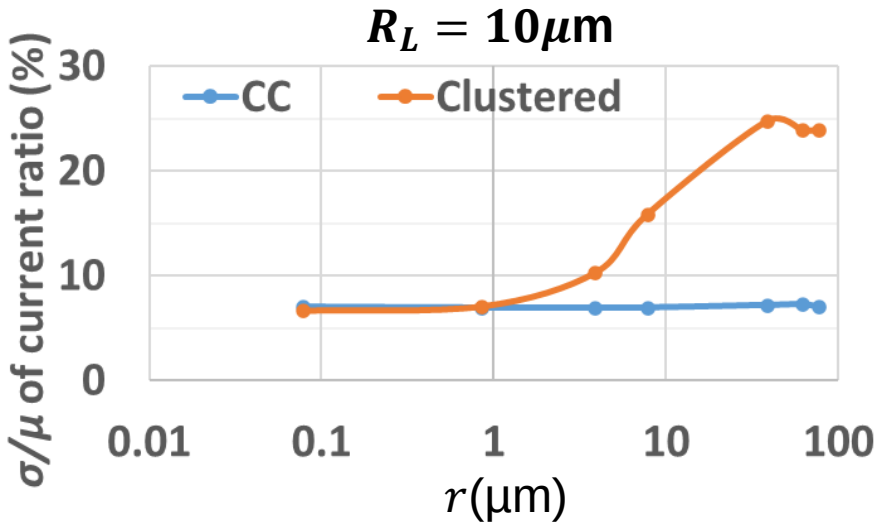
13

When is CC Layout (Un)necessary?





[Sharma, DATE21]



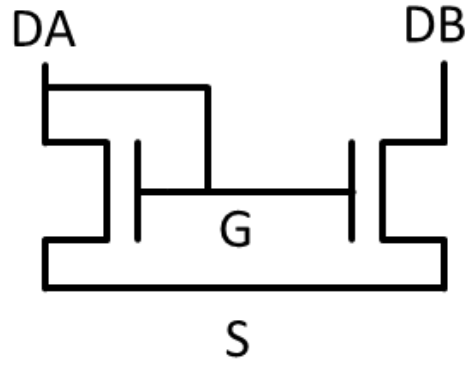
CC is not beneficial when layout size $\ll$ R_L

[Sharma, DATE21]

14

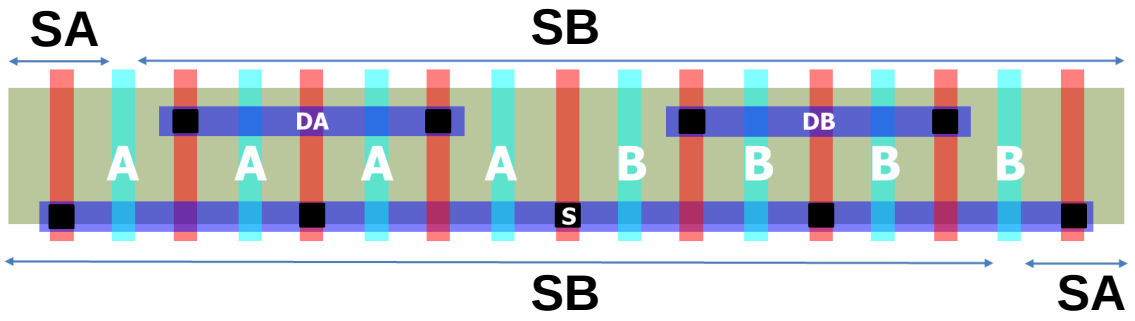
When is CC Layout (Un)necessary?

- LDEs affect the mean value: CC does not match LDEs

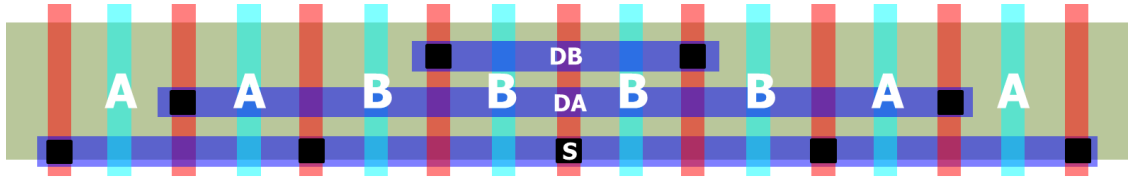


Current mirror

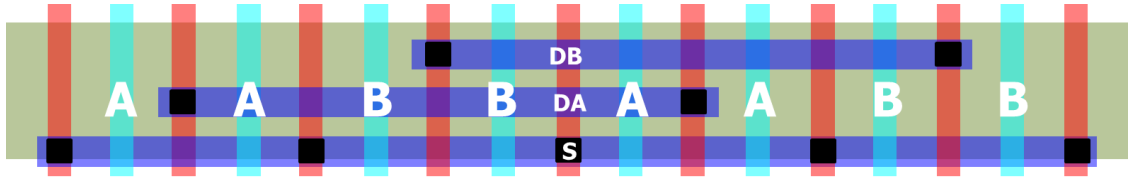
$$V_{th} \propto \frac{1}{\mathrm{LOD}} = \sum_{i=1}^{n} \left(\frac{1}{\mathrm{SA}_i + 0.5L_g} + \frac{1}{\mathrm{SB}_i + 0.5L_g} \right)$$



P1: Clustered



P2: CC



P3: Interdigitated

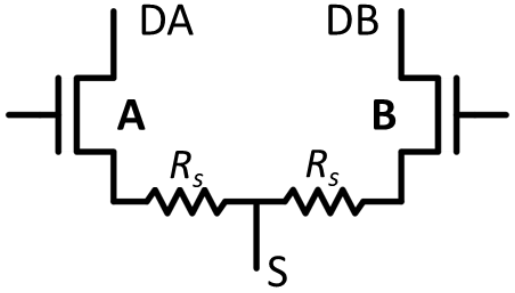
[Sharma, DATE21]

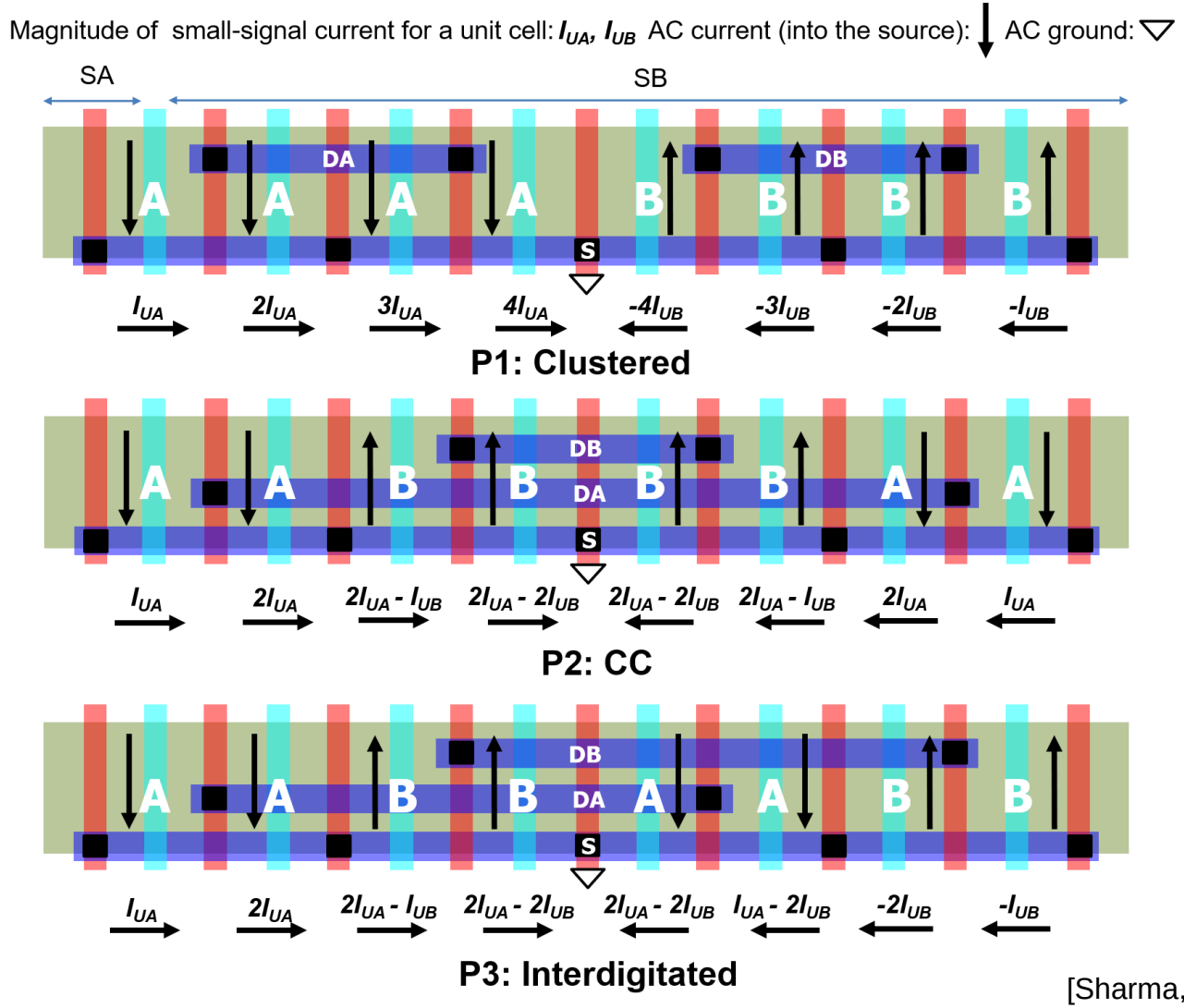
[Sharma, DATE21]

15

When is CC Layout (Un)necessary?

- Impact of parasitics

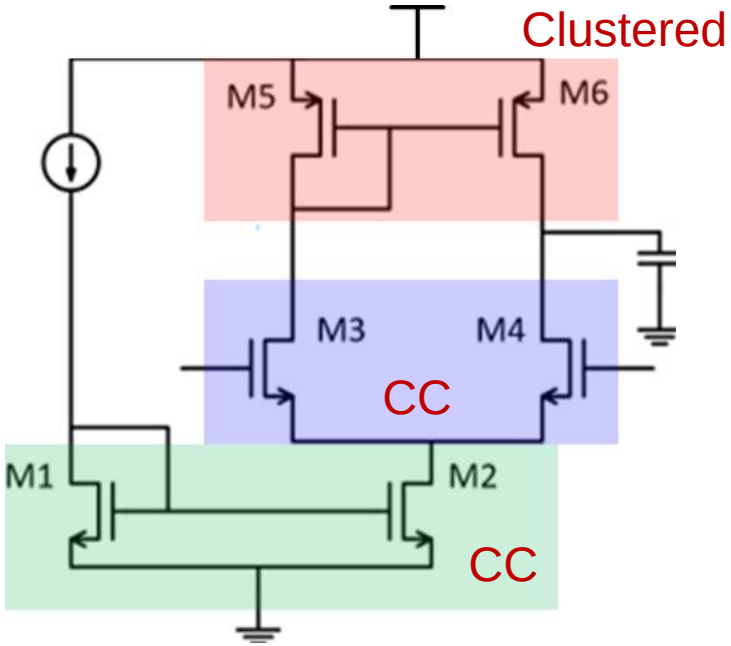




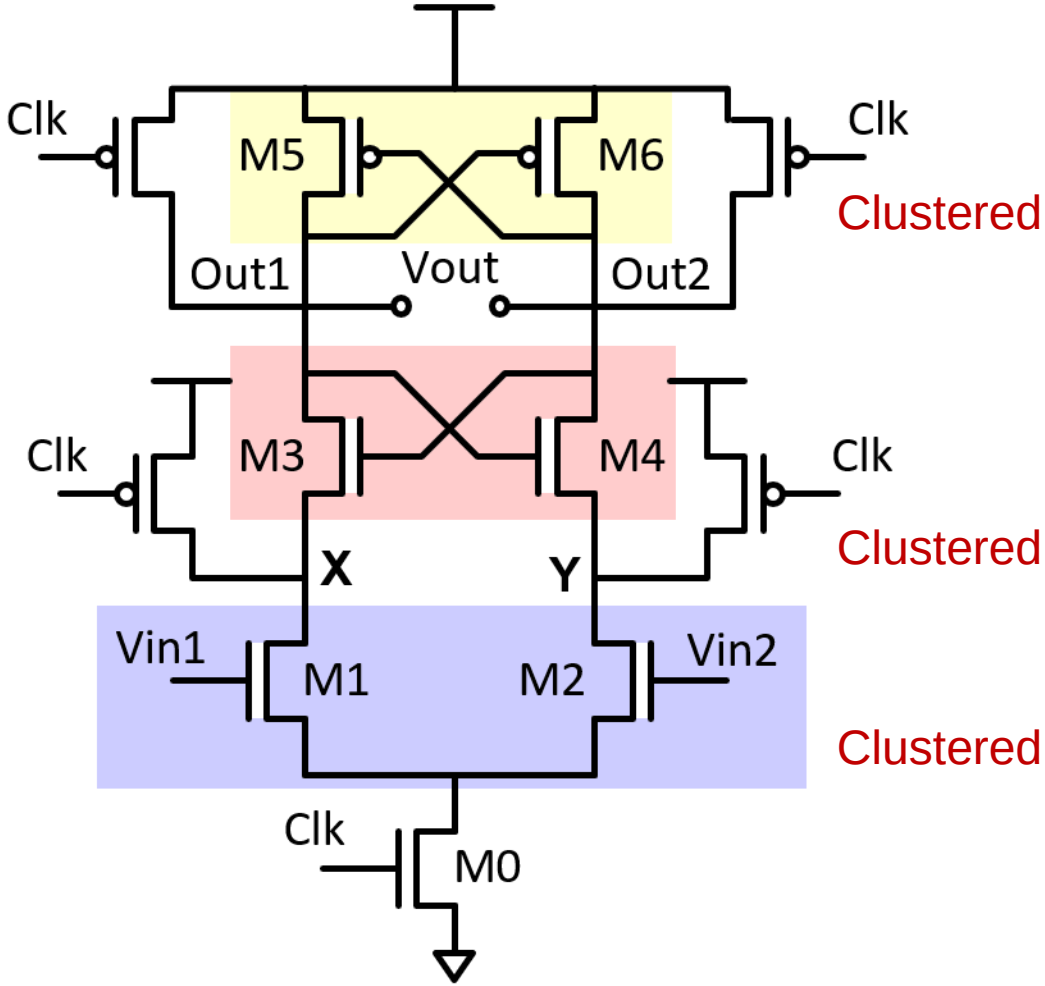
[Sharma, DATE21]

16

Optimal Layouts May Differ from Block to Block



[Sharma, DATE21]



[Sharma, DATE21]

17

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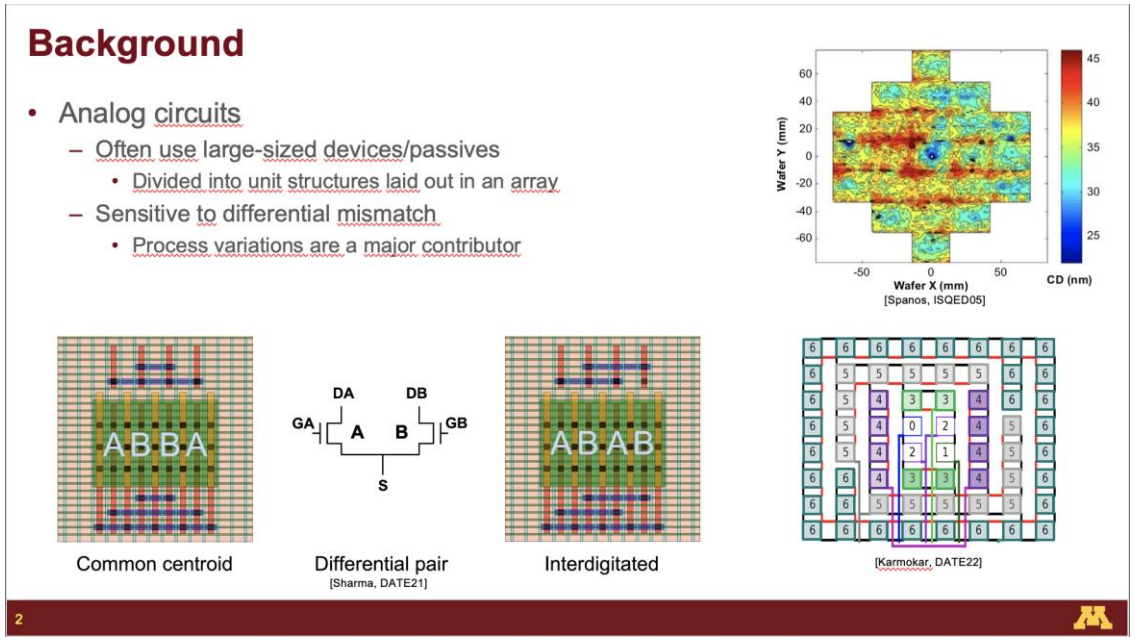

[From our ASPDAC22 talk]

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  - Designer input
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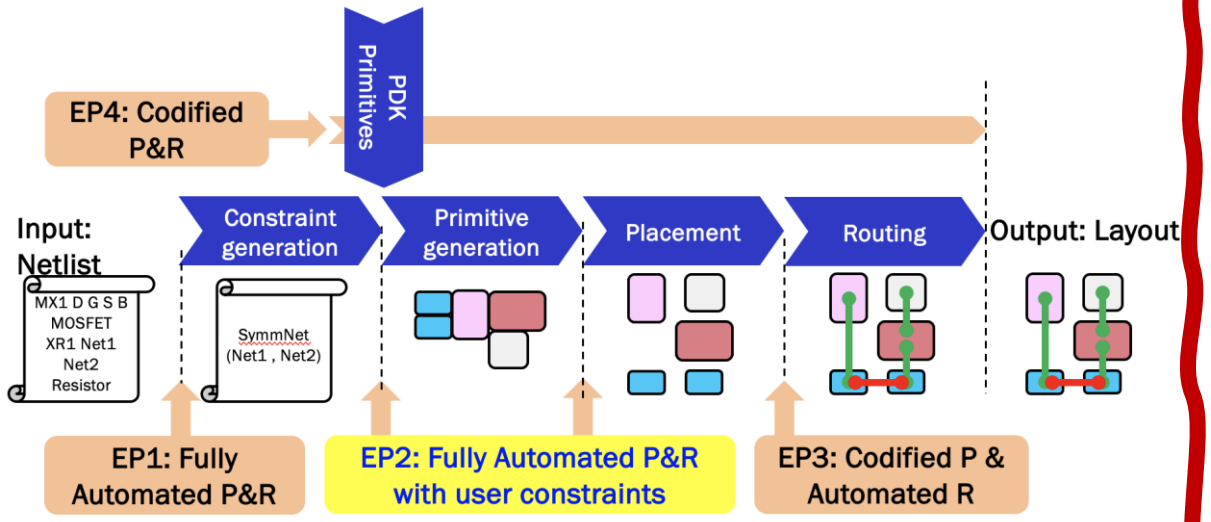
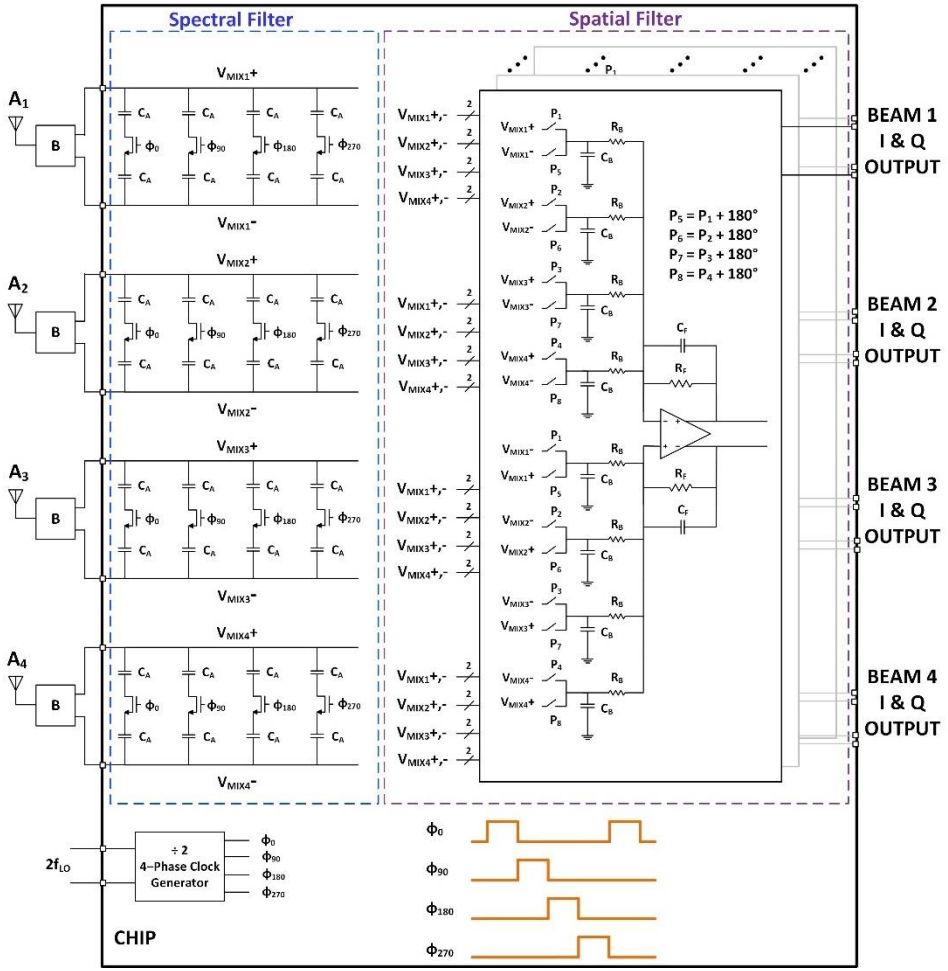
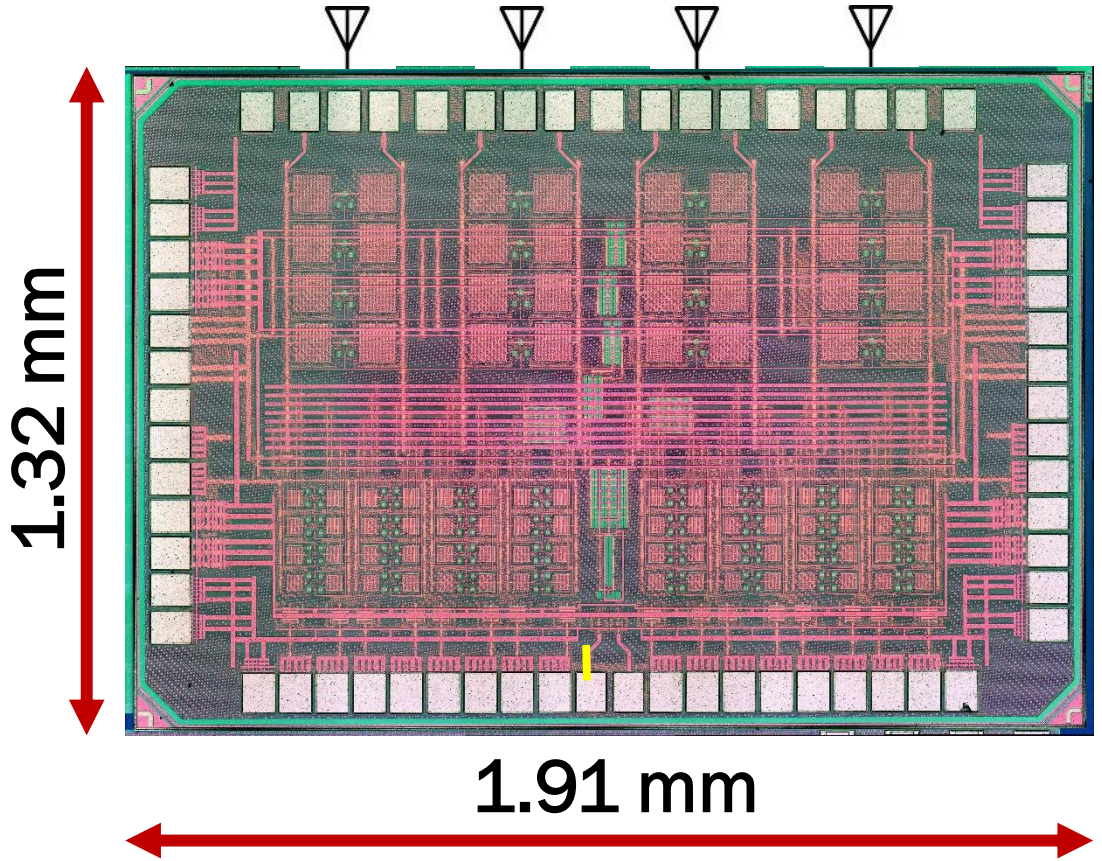


Building real systems with ALIGN

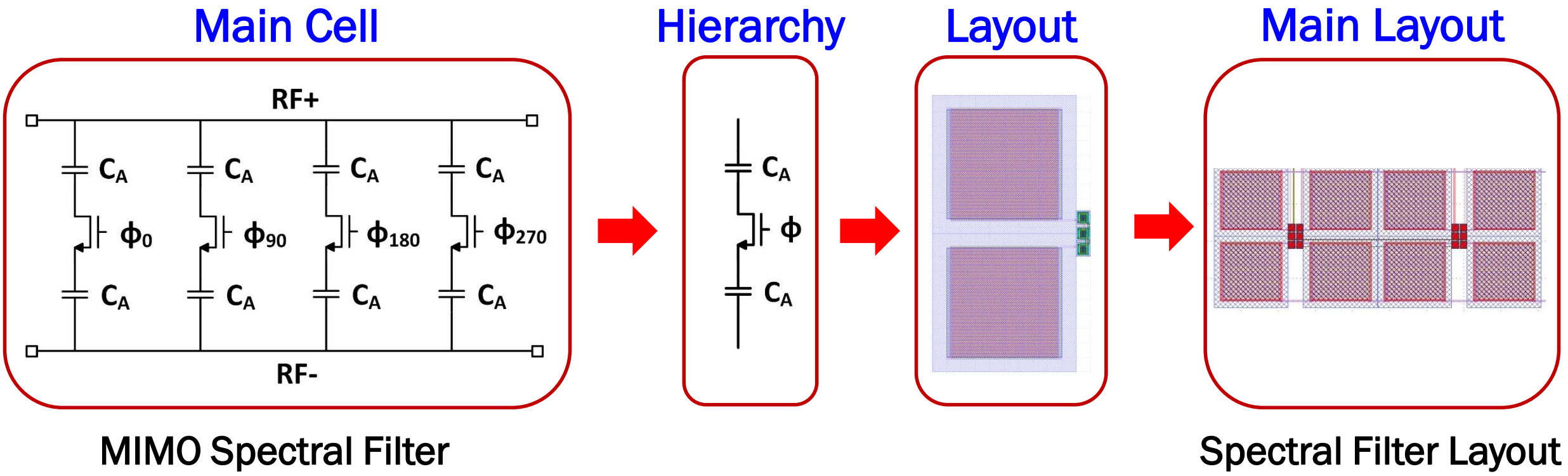
- MIMO receiver published ISSCC21



Manual Layout

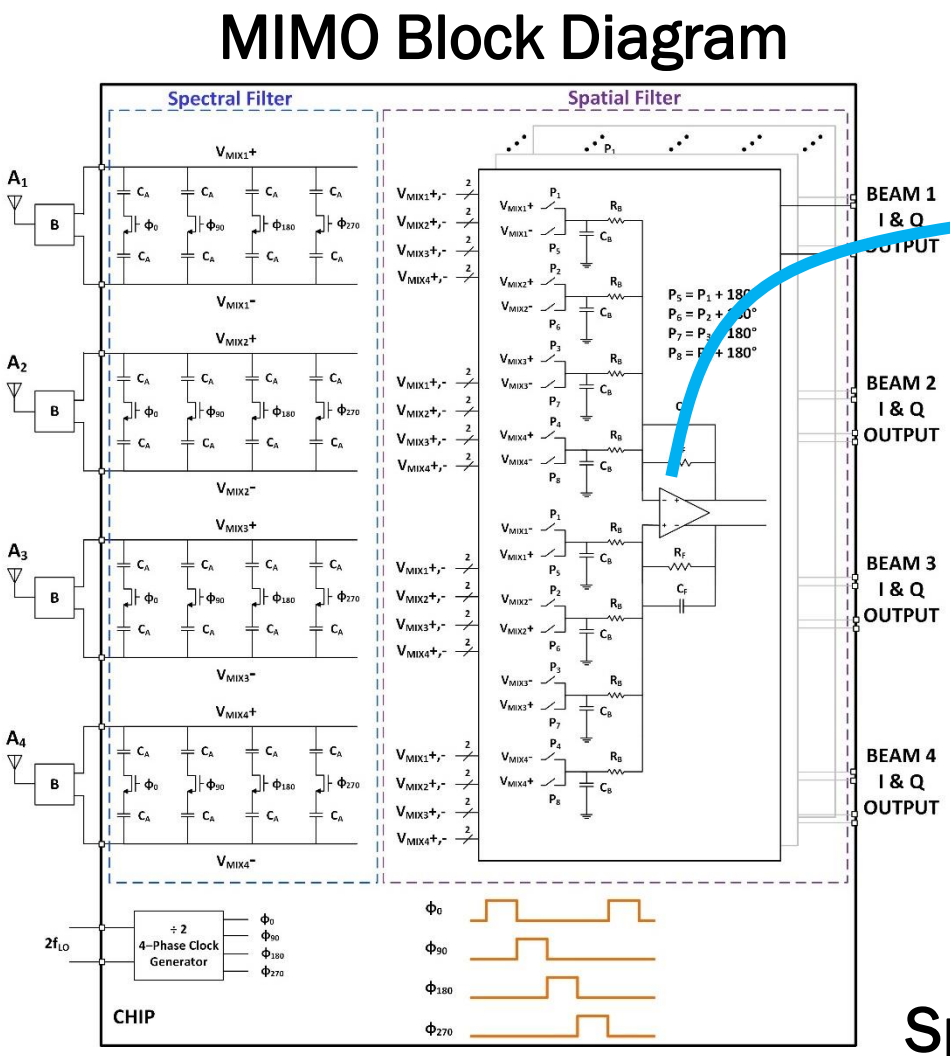


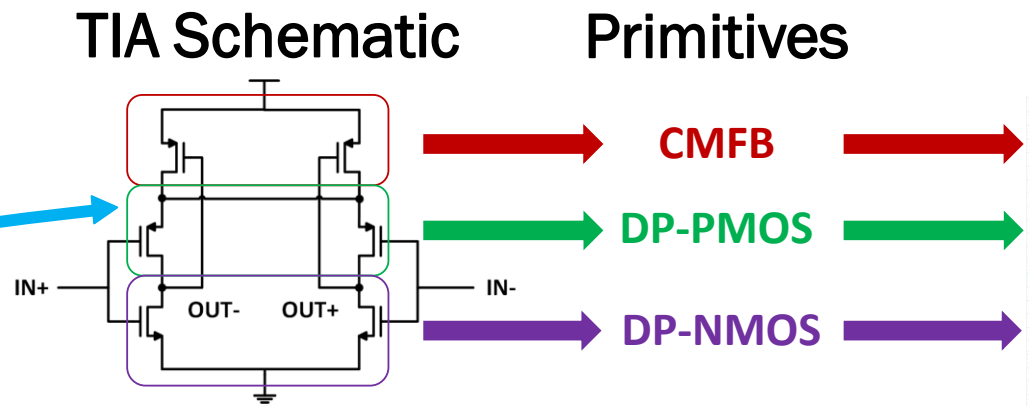
Hierarchical Layout Generation: Spectral filter

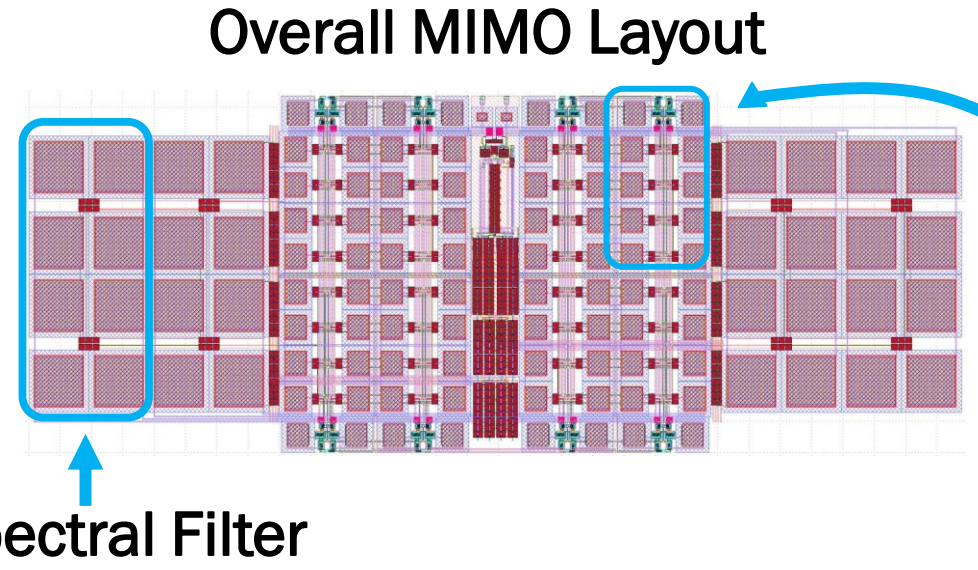


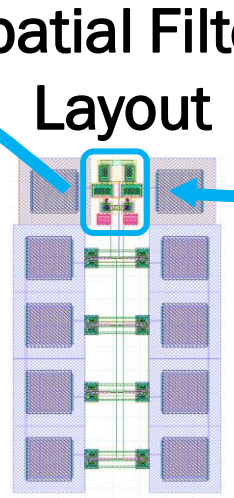
Create additional hierarchies to reduce layout generation time

Hierarchical Layout Generation: Spatial filter

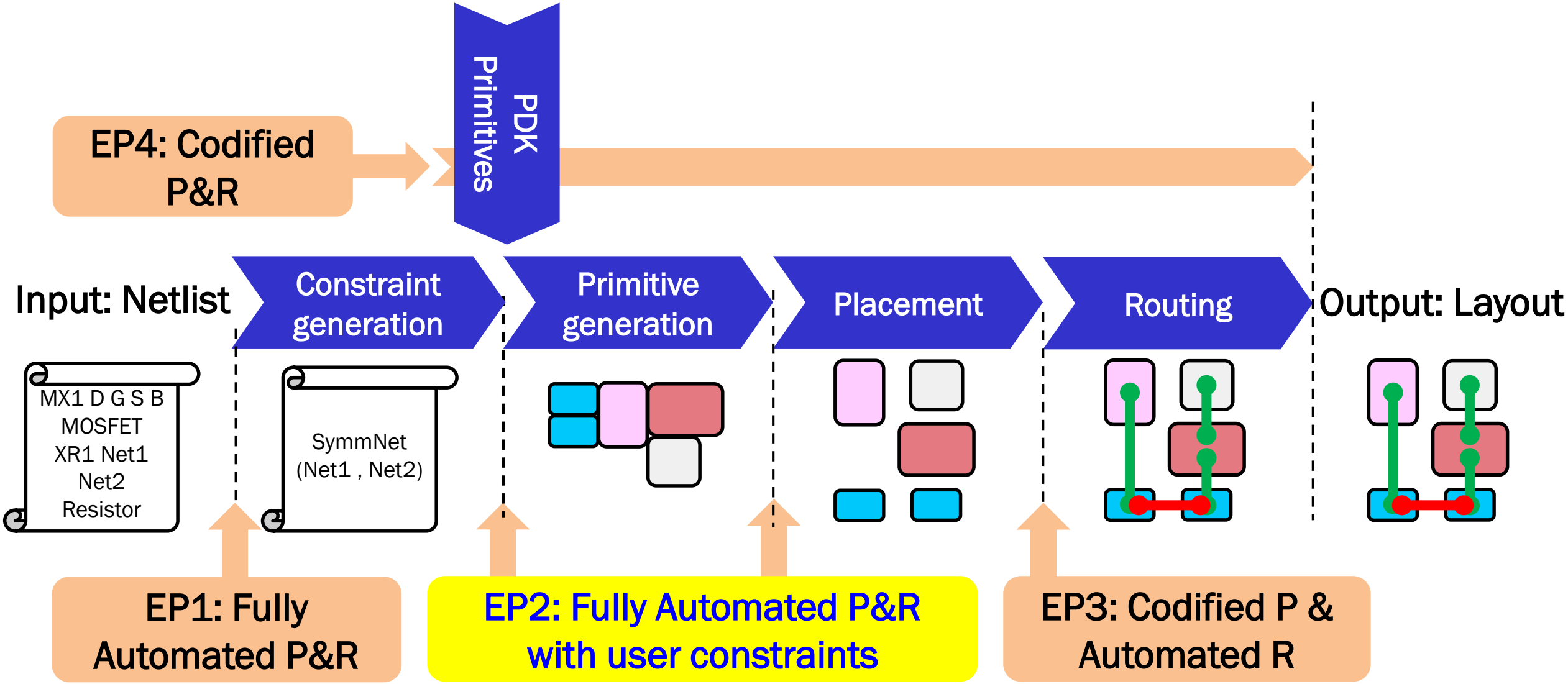








ALIGN Flow with Multiple Entry Points (EPs)

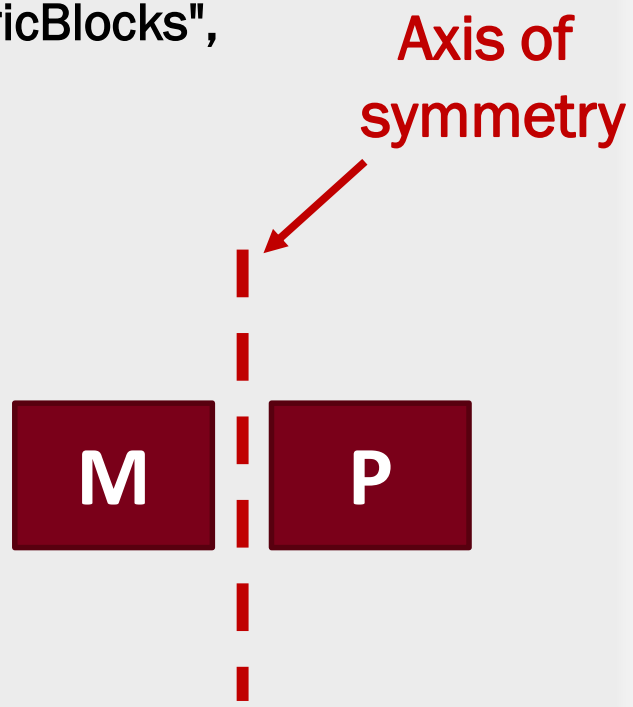


User Constraints

Placement

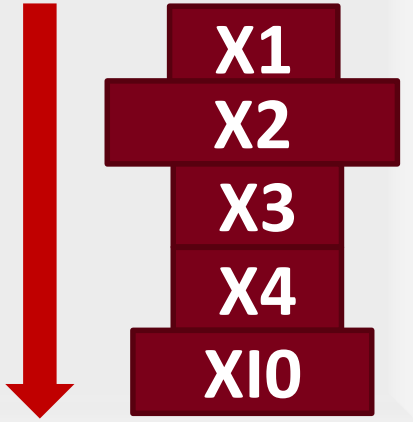
Symmetric Block

```
{
 "constraint":"SymmetricBlocks",
 "direction": "V",
 "pairs": [["M", "P"]]
 },
```



Block Ordering

```
{
"constraint": "Order",
"direction": "top_to_bottom",
"instances": ["X1", "X2", "X3", "X4", "XI0"]
 }
```

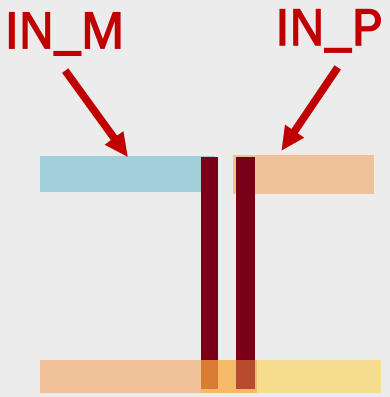


User Constraints

Routing

Symmetric Net

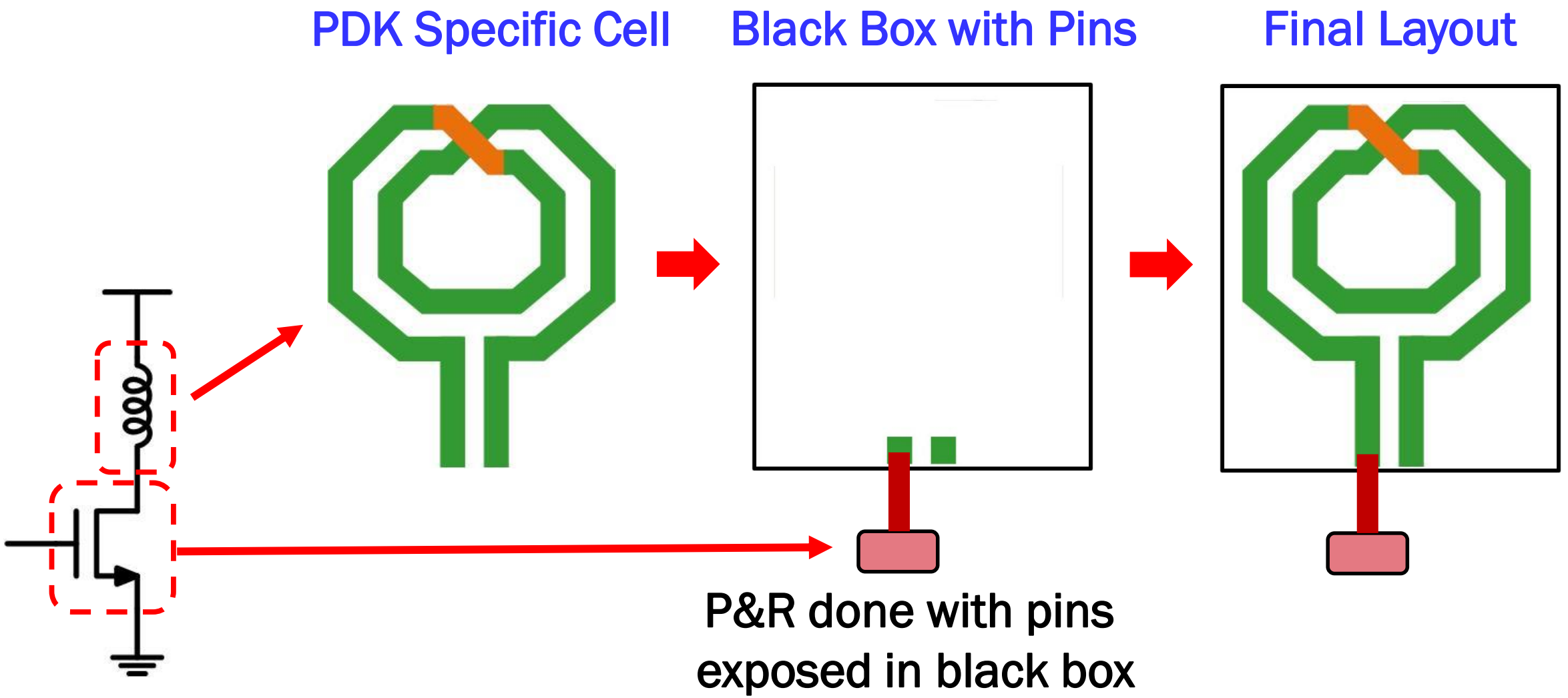
```
{
 "const_name": "SymmNet",
 "net1": {"name": "IN_M“ },
 "net2": {"name": "IN_P“  },
 }
```



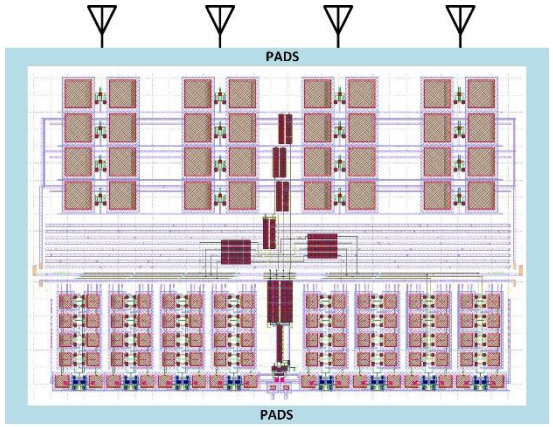
Net-specific Metal Width & Spacing

```
{
  "nets": [
    {"name": “net1",  "widths": {"M1":1.0, "M2":1.0.  },
   "directions": {"M4":"O"},
   "preferred_layers":["M4", "M5"],
   "spaces": {"M4":0.2} ]
 }
```

Black Box Methodology

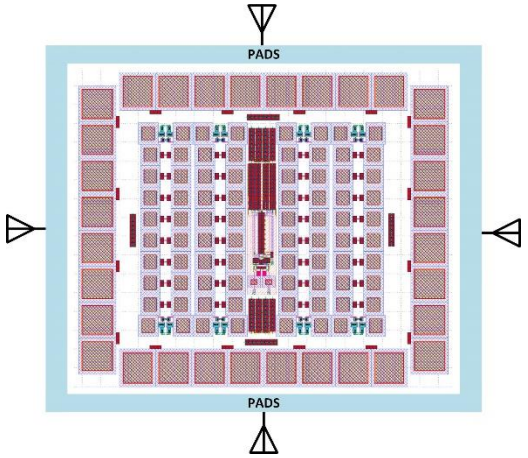


Multiple Floorplans

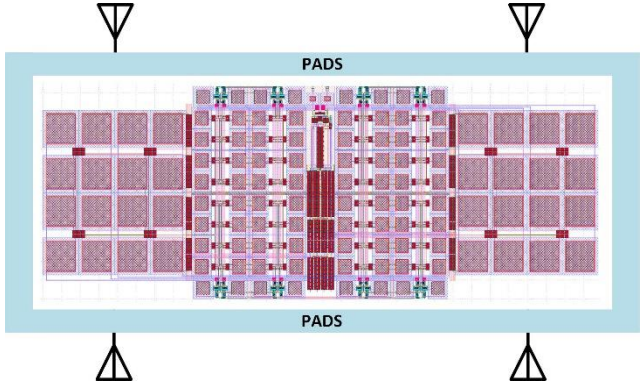


Manual (AR = 3:2)

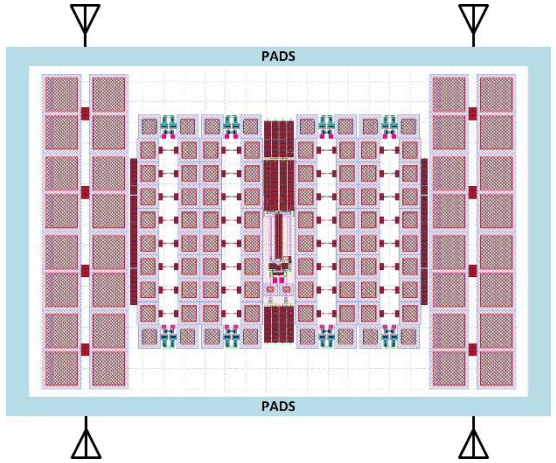
AR = Aspect Ratio



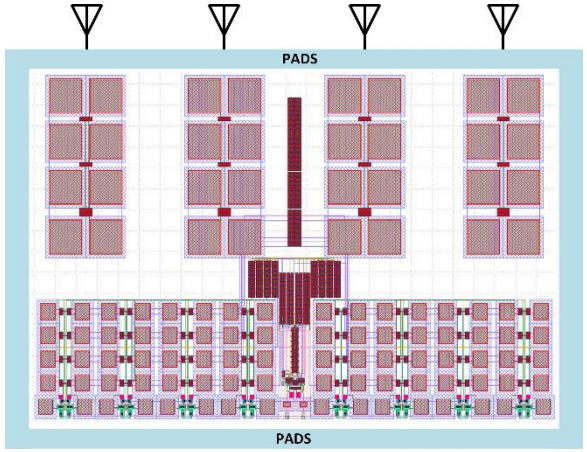
Floorplan 1 (AR = 1.2:1)



Floorplan 2 (AR = 2.6:1)

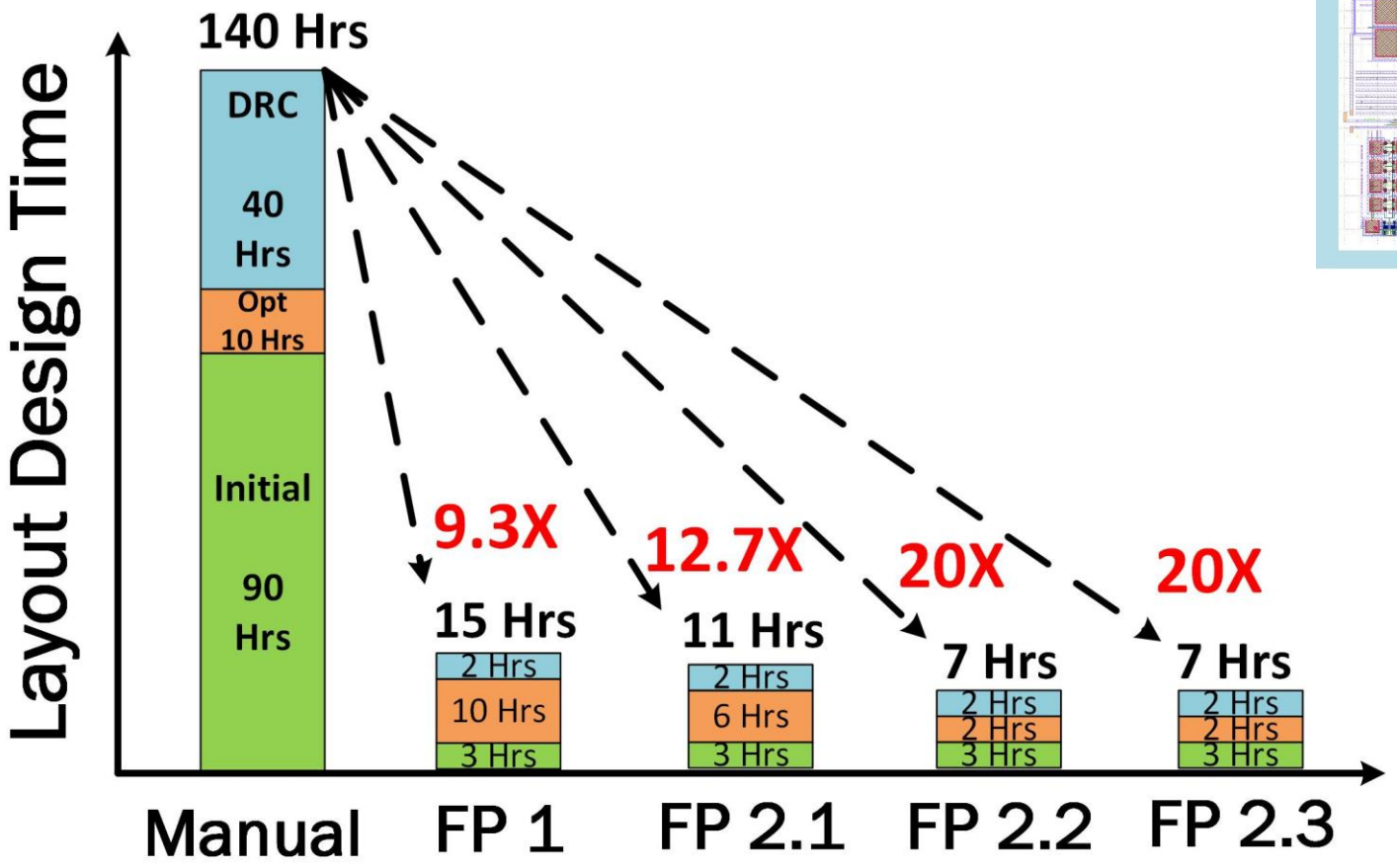


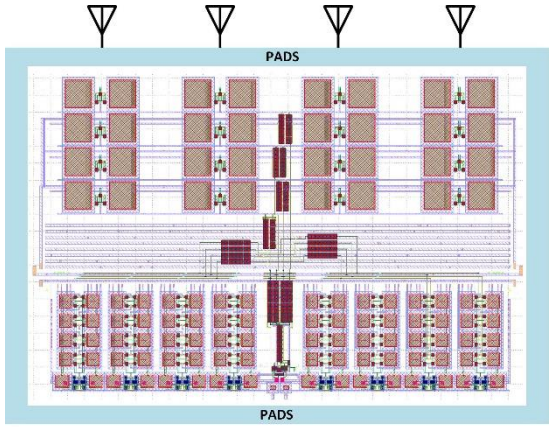
Floorplan 3 (AR = 3:2)



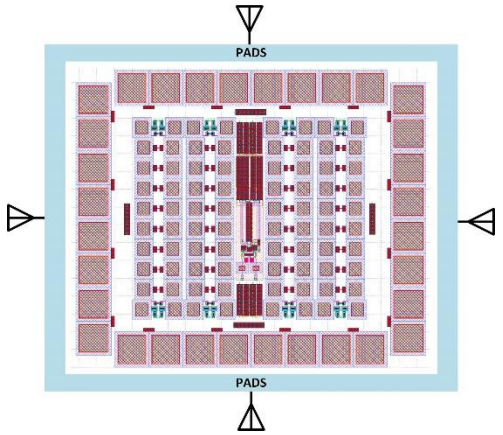
Floorplan 4 (AR = 3:2)

Productivity Improvement

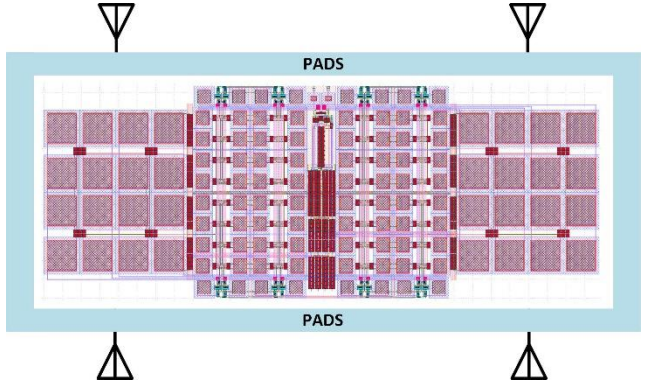




Manual



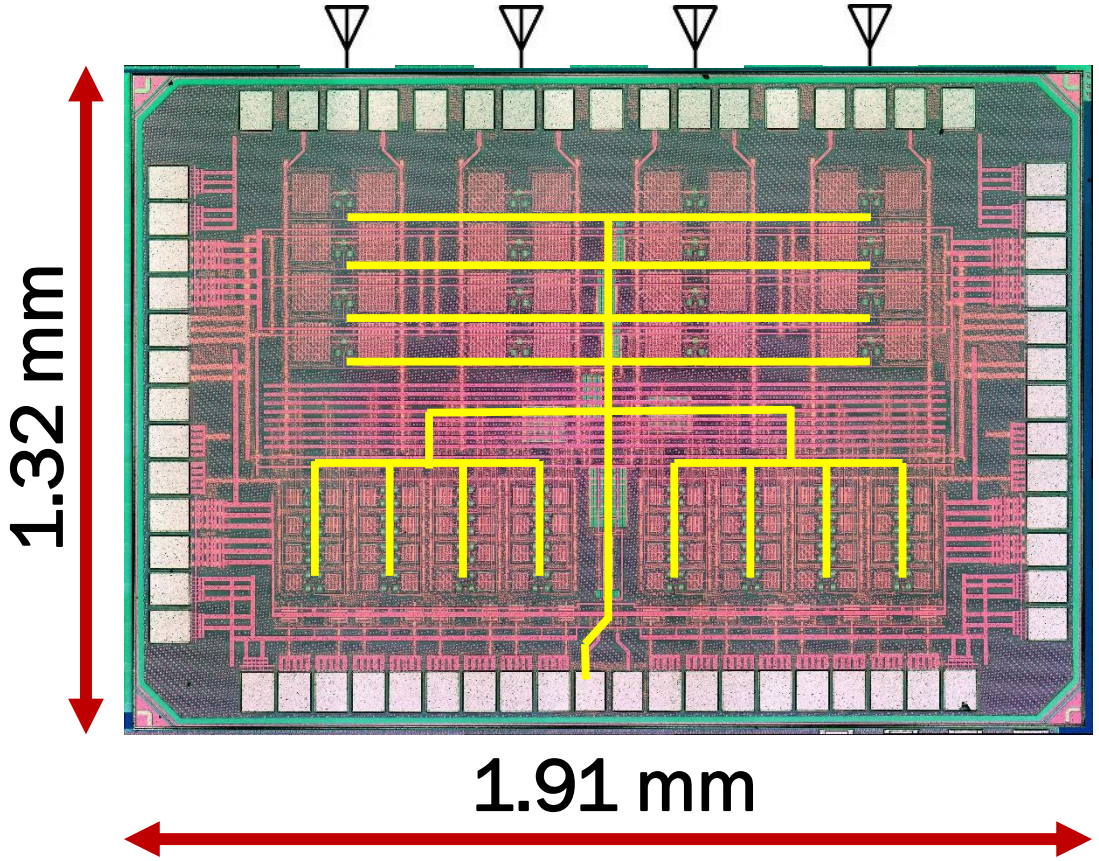
Floorplan 1



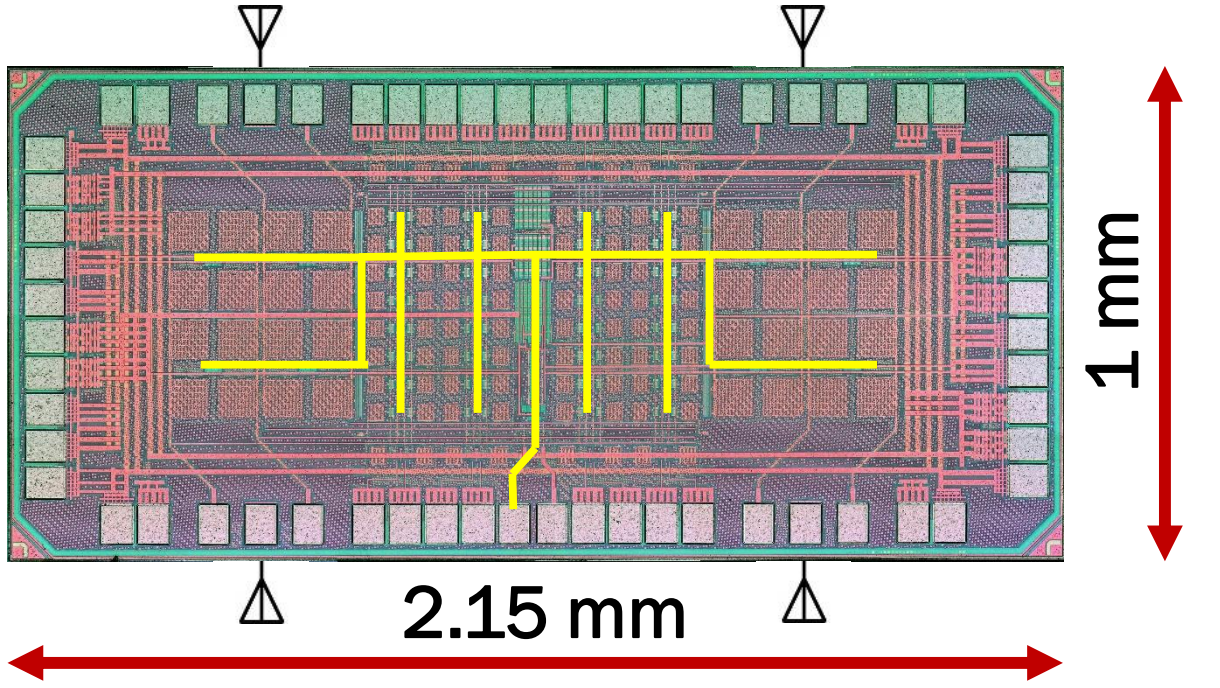
Floorplan 2

Die Photos

Manual Layout

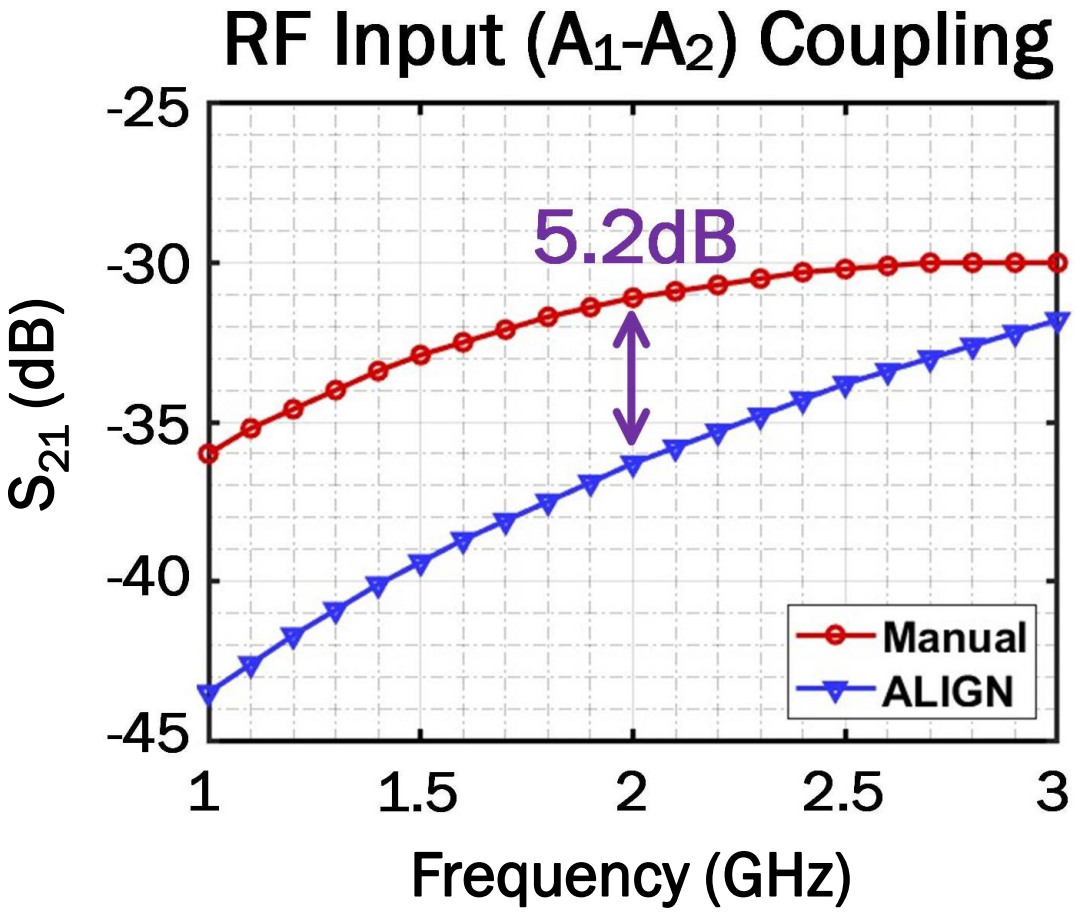


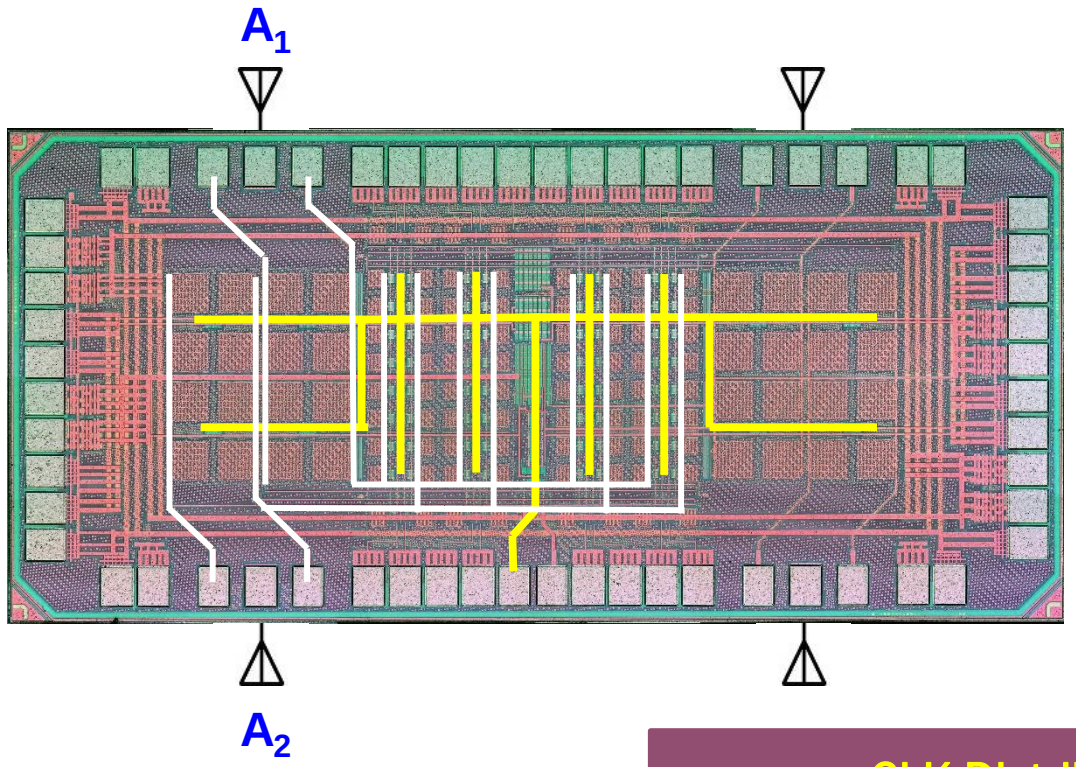
ALIGN Layout



Area reduction by 14% (39% without PADS)

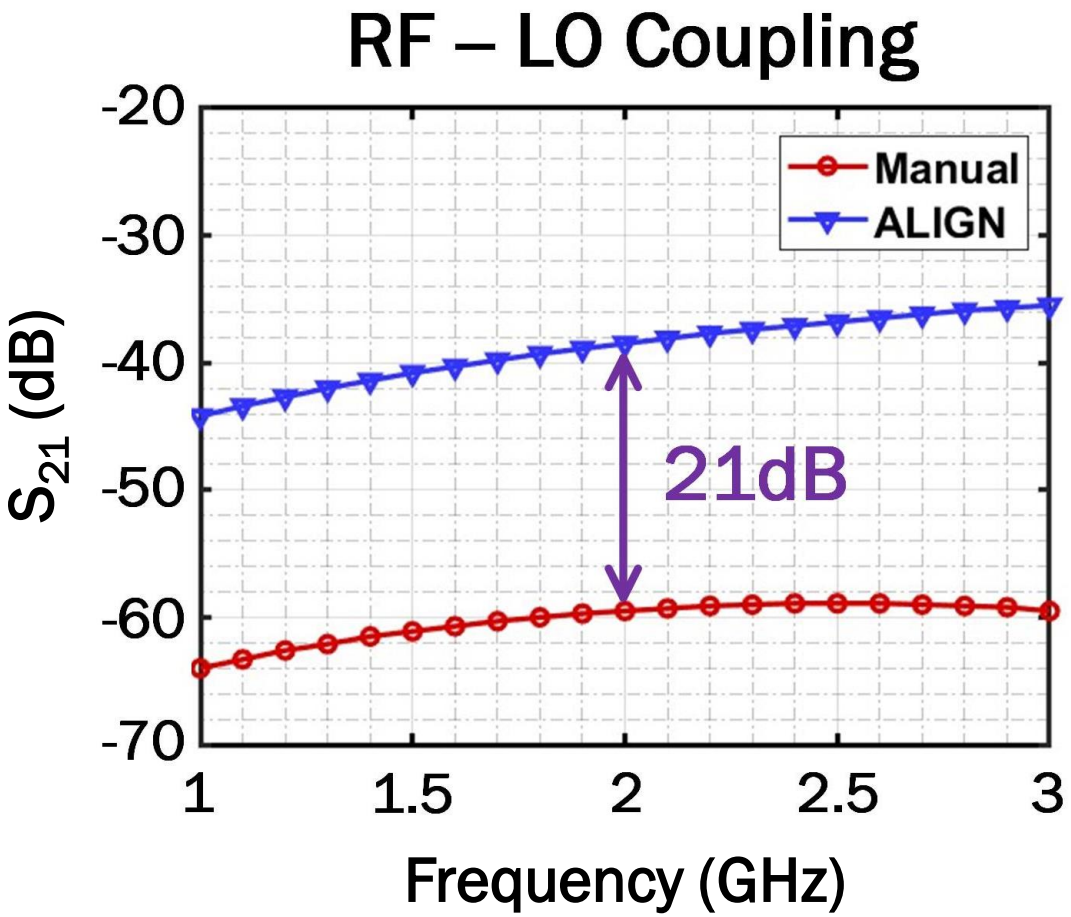
Coupling EM Simulation

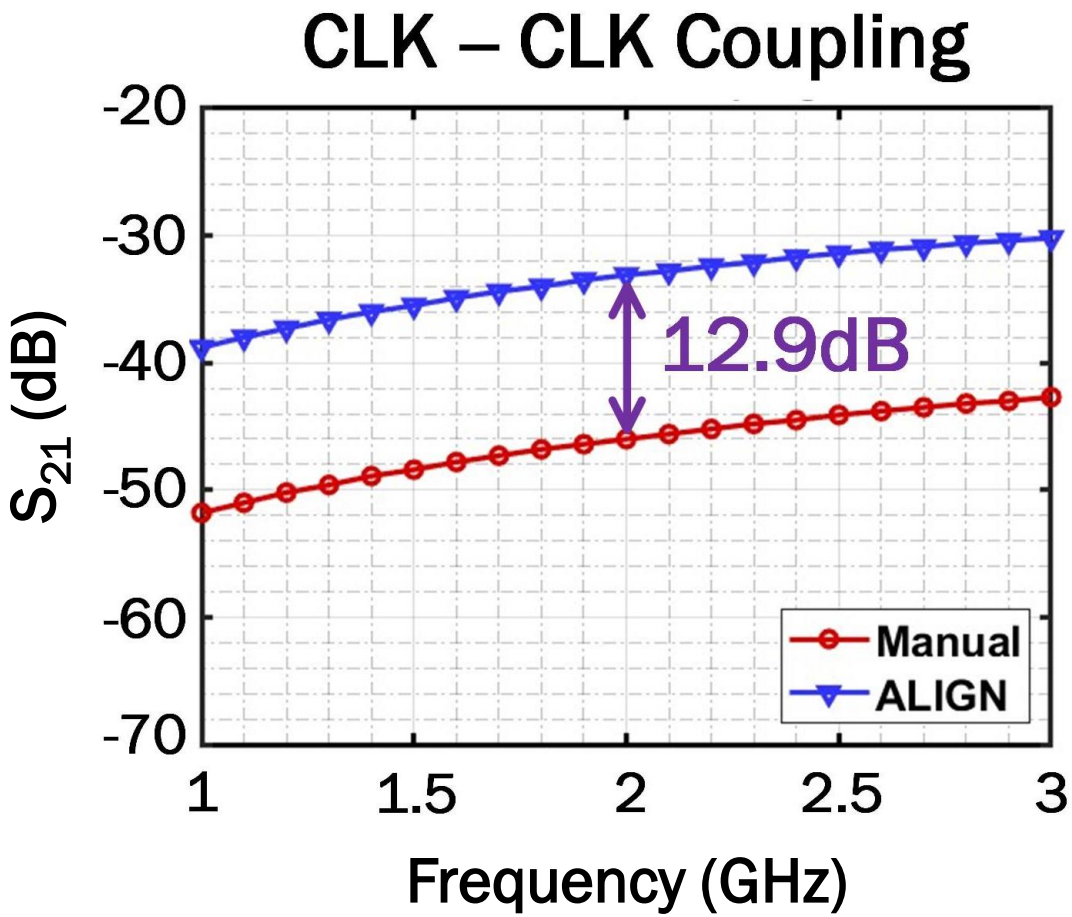




ALIGN decreased coupling between antenna inputs A_1– A_2

Coupling EM Simulation



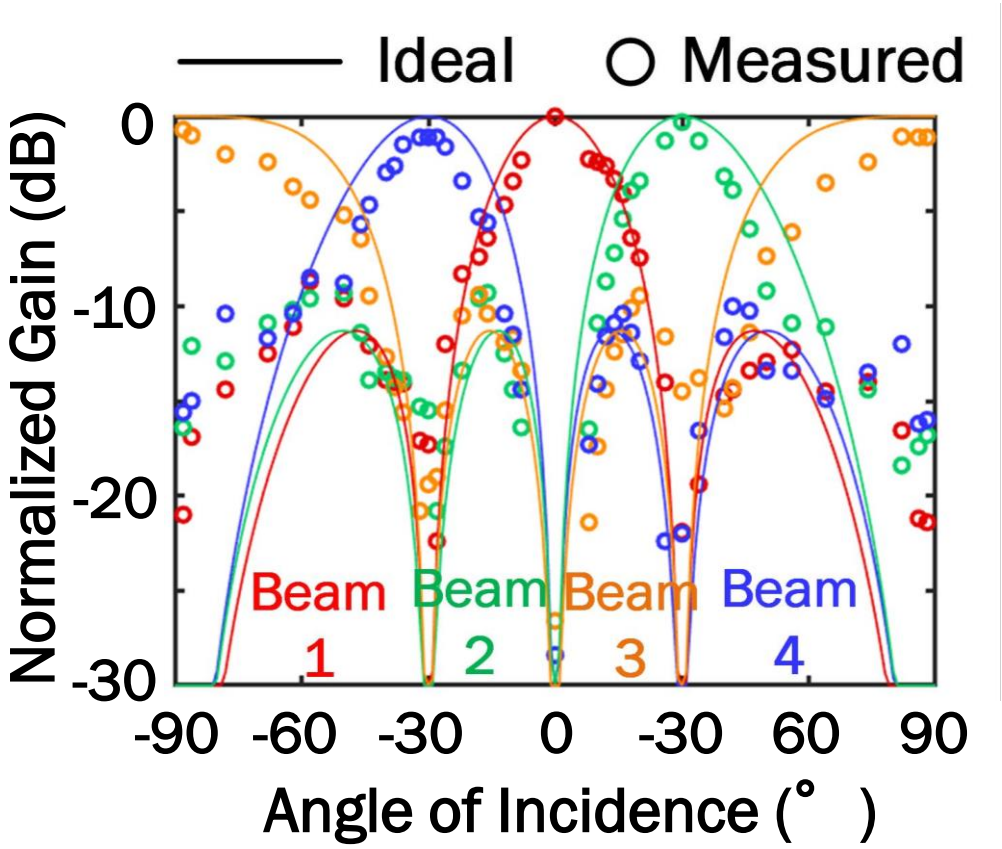


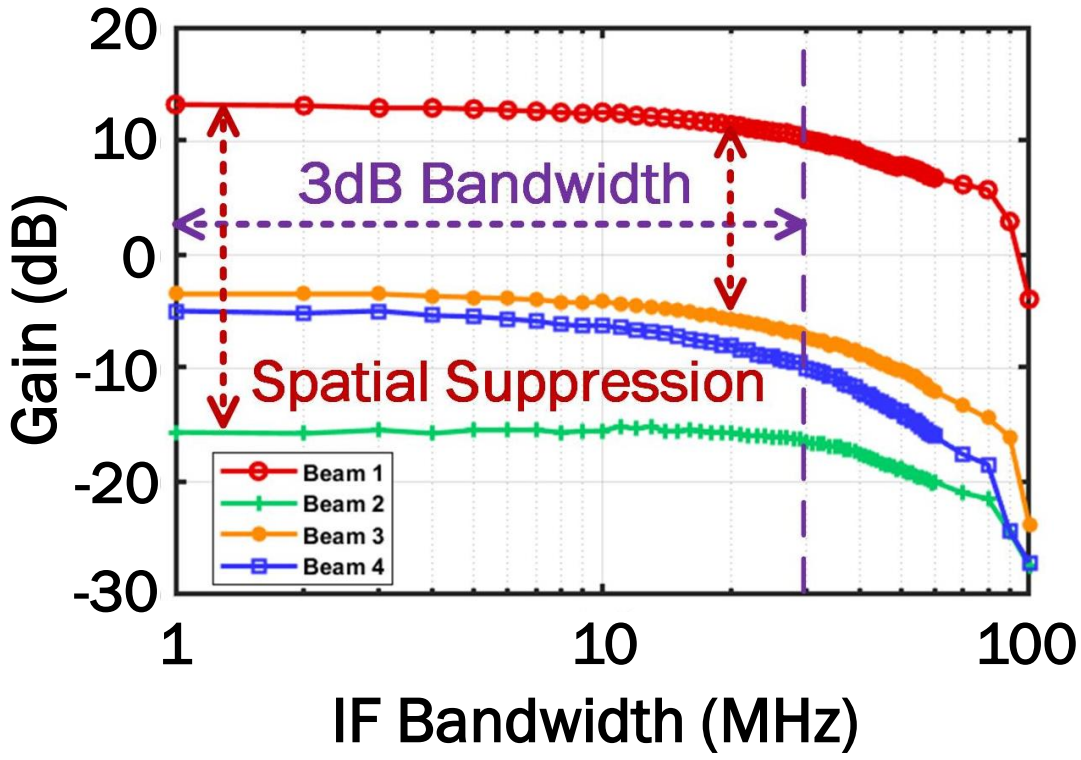
ALIGN layout increased coupling between RF and LO ports

Tradeoff between coupling on differential lines vs. on antenna inputs typical in manual layout

ALIGN speeds up exploration

Measurement: Spatial Gain & IF Bandwidth

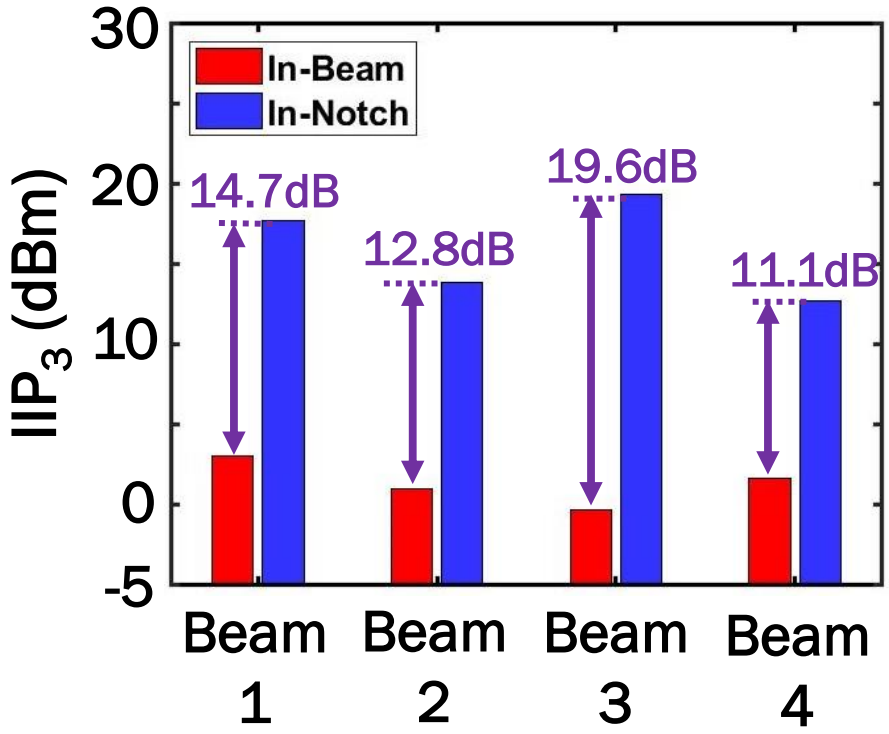




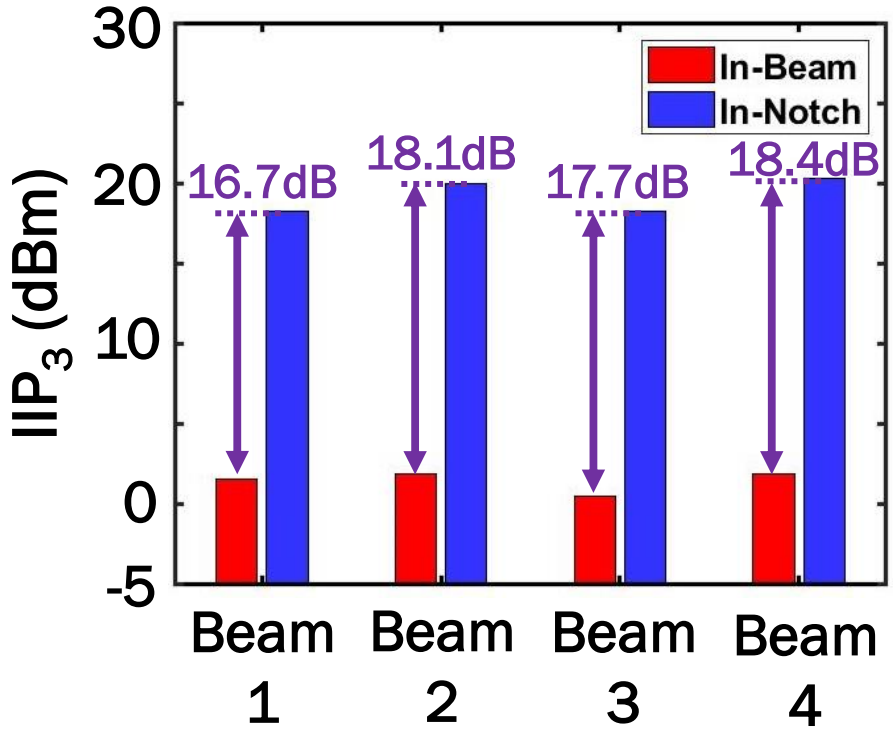
3dB bandwidth: ALIGN numbers better than manual

Measurement: IIP_3 - All Beams

Manual Layout



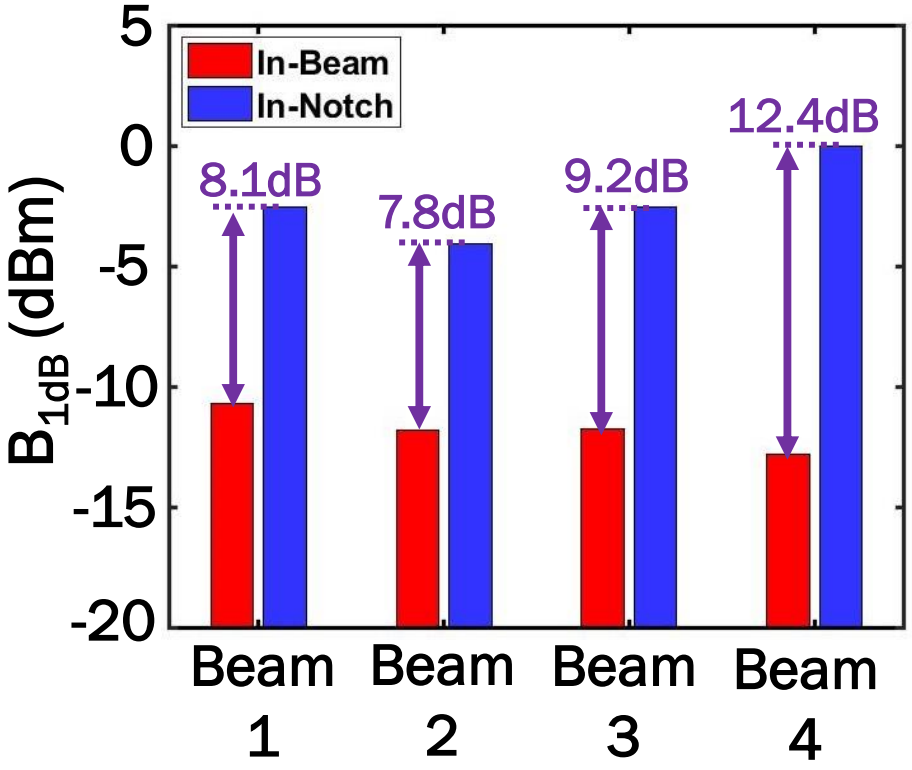
ALIGN Layout



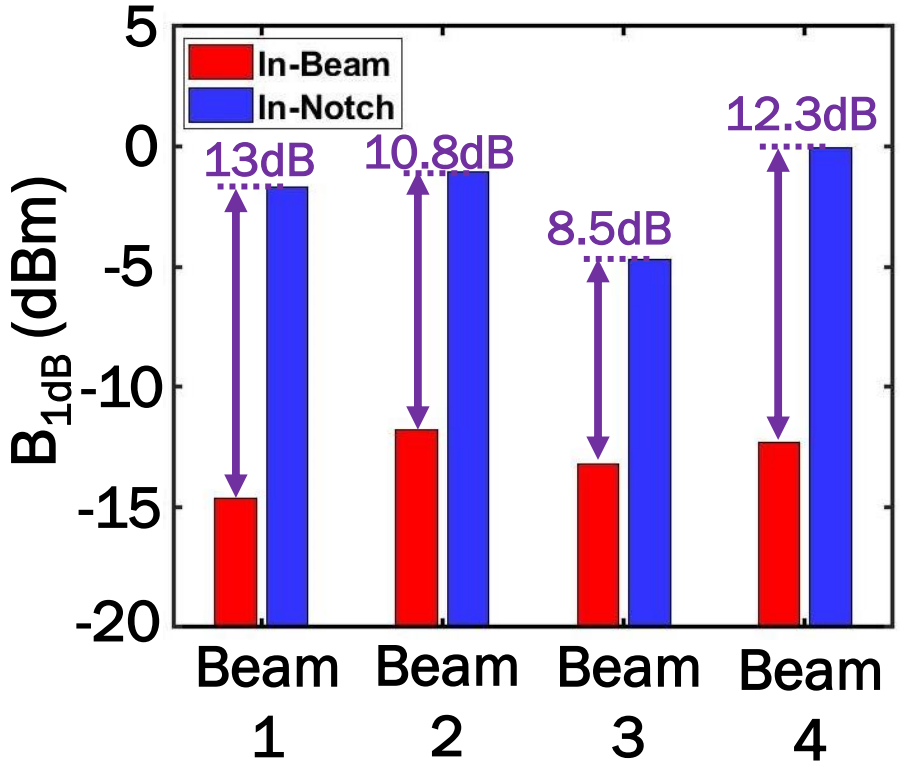
IIP_3 for all beams: ALIGN numbers similar to manual

Measurement: B_{1dB} All Beams

Manual Layout



ALIGN Layout



B_{1dB} for all beams: ALIGN numbers similar to manual layout

Comparison Table

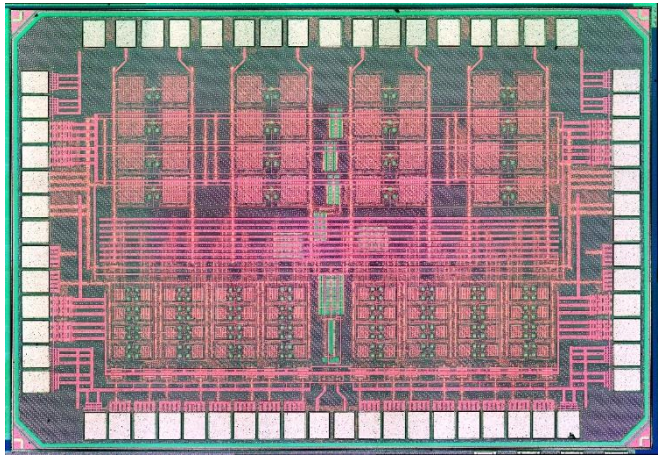
		Manual Layout [6]	This Work
Technology		65nm CMOS	65nm CMOS
Operating Frequency Range (GHz)		1 – 3	1 – 2.3*
Max Spatial Suppression (dB)		27	28.4
Power (mW)		130 – 242	130 – 175
Area (mm^2)		2.52	2.15
In-Band (dBm)	In-Notch IIP_3	19.3	20.3
	In-Beam OIP_3	18.1	14.9
Out-of-Band IIP_3 (dBm)	In-Notch [Δf/BW = 2]	21.35	23.87
	In-Beam [Δf/BW = 4.6]	14.2	19.3
In-Band B_{1dB} (dBm)	In-Notch	0.26	–0.04
	In-Beam	–10.67	–11.8

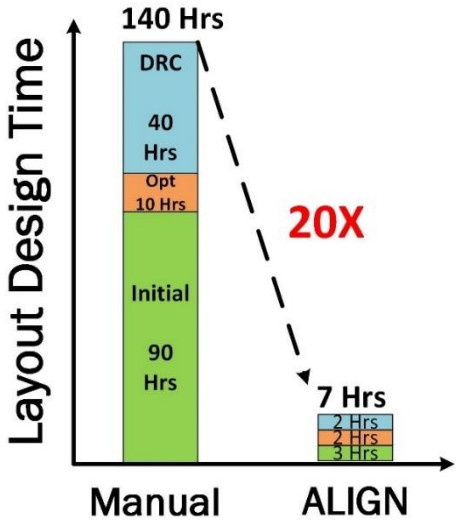
* Frequency can be improved by better clock buffer placement

Summary of the MIMO layout generation effort

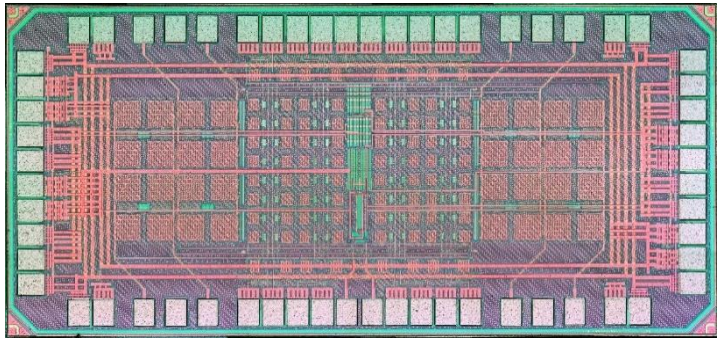
- ALIGN generates layout using hierarchy and defined primitives
- ALIGN reduces layout design time by ~20X
- ALIGN layout performance closely matches manual layout
- Design performance can be optimized with layout automation

Manual Layout





ALIGN Layout

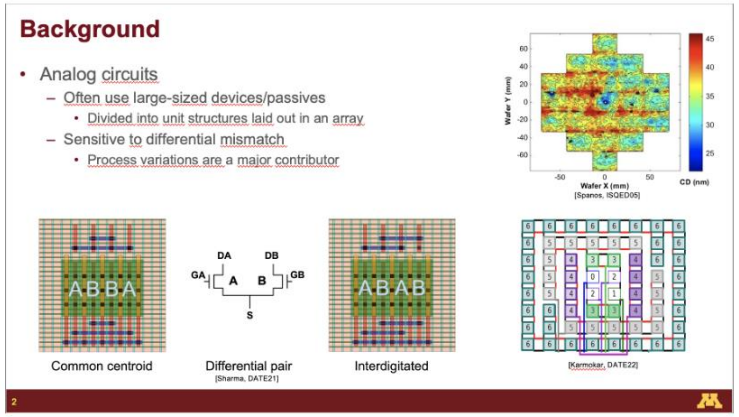


Conclusion: “A rising tide raises all ships”

- Analog designers are a tough bunch to please!
  - … but many accept that automation is essential
- Essential to overcome major limitations of prior efforts to give analog EDA a chance

Link to process?

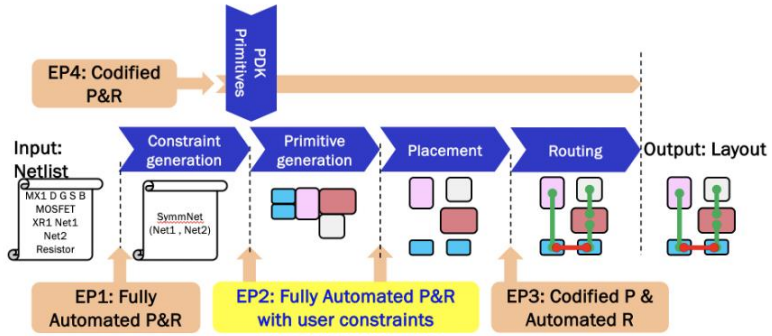
- Many conventional assumptions, which are unquestioned
- Lack of support from publicly-available measured data



[From our ASPDAC22 talk]

Link to the designer?

- Incorporating designer input critical
- EDA tools try to “automate it all”: this will not win over designers
- Need to support
  - Designer input
  - Designer-driven design-space exploration



- Move to a collaborative model