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Performance-Driven Analog Layout Automation: Current Status and Future Directions

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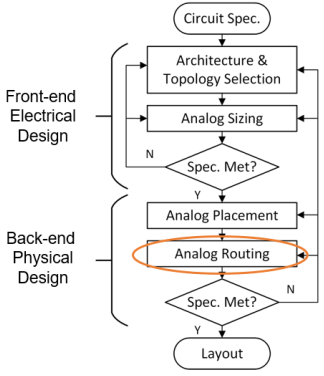
Outline

Introduction

Typical Automatic Analog Circuit Design Flow

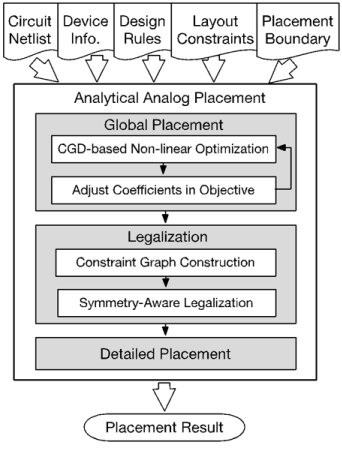
- Automated analog design often consists of front-end and back-end flows
- Physical design (back-end) is separated into placement and routing



The design flow of analog circuits.

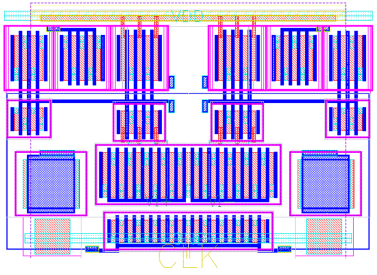
What is Analog Placement?

- Input
  - Circuit netlist
  - Device information
  - Design rules
  - Layout constraints
  - ...
- Output: a legal placement solution
- Constraints
  - Symmetry
- Objectives
  - Area, Wirelength, ...
  - Post-layout metrics: Offset_Voltage, CMRR, Gain, Bandwidth, Noise, ...

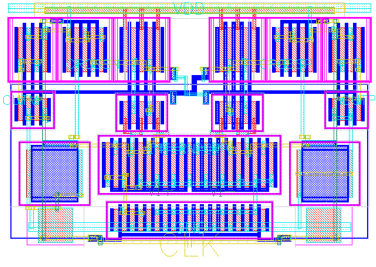


The framework for analog placement.

What is Analog Routing?



A result of the placed comparator.



The routing solution.

- The metal connection is added to the layout.

Related Work

Existing Problems

Analog circuit placement and routing are critical to optimal performance, but obtaining a decent circuit layout requires significant time and expertise:

- Unlike digital circuits, analog circuits are sensitive to layout parasitics and coupling, which can complicate the relationship between performance and layout.
- There lacks a practical way to produce generalized performance models for layout implementation[1].

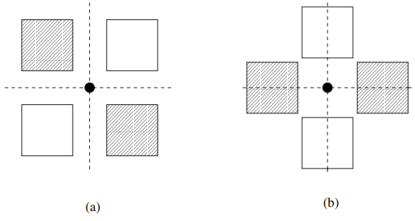
[1] **Hao Chen et al. (1993). "Challenges and opportunities toward fully automated analog layout design". In:** *The Journal of Supercomputing* **41.11, pp. 1674–4926.**

Existing Problems: Performance-Driven Placement

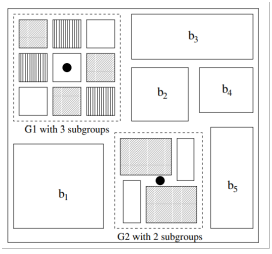
The existing analog layout placement methods are mainly focused on optimizing *proxy* objectives for performance:

- **Symmetry and common centroid**[2]*;*

Qiang et al. propose to handle the common centroid constraint in placement to reduce parasitic mismatch.



2-D symmetry (b) does not include placement (a) which also satisfies the common centroid constraint.



A packing with two common centroid groups.

[2]**Qiang Ma, Evangeline F. Y. Young, and K. P. Pun (2007). "Analog placement with common centroid constraints".** In: *Proc. ICCAD*, pp. 579–585.

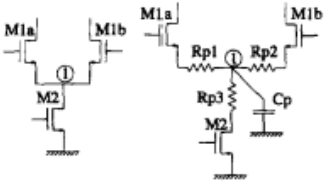
- **Linear approximation model**

Lampaert et al.[3] present a new approach toward the performance-driven placement of analog integrated circuits by introducing a performance degradation term.

The performance degradation ΔP_j for the j th performance characteristic due to interconnect parasitics can be determined using the precalculated sensitivity information:

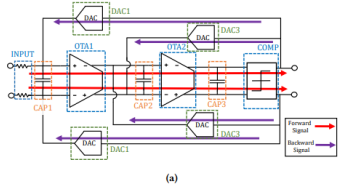
$$\Delta P_j = \sum_{k=1}^{m} \left(S^j_{C_{p,k}} C_{p,k} + \sum_{i=1}^{n_k} S^j_{R_{p,ki}} R_{p,ki} \right) \tag{1}$$

where m is the number of nodes minus the ground node and n_k is the number of terminals of net k.



- **Current path and signal flow**[4]

Zhu et al.[5] propose to consider the critical signal paths in automatic AMS placement.



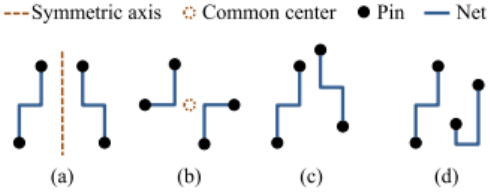
[4]**Keren Zhu, Hao Chen, Mingjie Liu, et al. (2020). "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow".** In: *Proc. ICCAD*, pp. 1–9.

Existing Problems: Performance-Driven Routing

The analog router cannot adopt specialized layout strategies for specific circuit classes like human layout experts, so *proxy* heuristic method is honored in performance-driven analog routing.

- **Symmetry** has been widely adopted as an essential component of the analog routing problem[6].

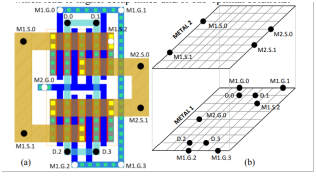
Ou et al. propose different levels of geometrical matching constraints[7].



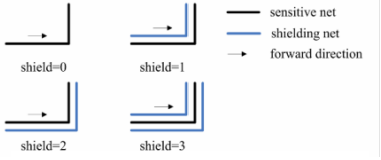
(a) Symmetric constraint. (b) Common-centroid constraint. (c) Topology-matching constraint. (d) Length-matching constraint.

[6] **Linfu Xiao et al. (2010). "Practical placement and routing techniques for analog circuit designs".** In: *Proc. ICCAD*; **Hung-Chih Ou, Hsing-Chih Chang Chien, and Yao-Wen Chang (2012). "Non-uniform multilevel analog routing with matching constraints".** In: *Proceedings of*

Other works optimize power routing[8] and propose shielding critical nets[9].



Optimize power routing.



Shielding critical nets.

[8] **Ricardo Martins et al. (2014). "Electromigration-aware and IR-drop avoidance routing in analog multiport terminal structures".** In: *2014 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, pp. 1–6.

[9] **Qiang Gao et al. (2010). "Analog circuit shielding routing algorithm based on net classification".** In: *Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design*, pp. 123–128.

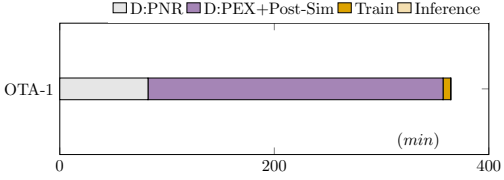
Case Study

Case 1: Analog Performance Modeling Lifecycle

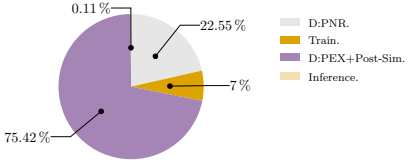
The performance modeling cycle can be divided into three stages:

- **Data Acquisition**: The data acquisition stage includes **PNR** and parasitic parameter extraction (**PEX**) and post-layout performance simulation (**Post-Sim**).
- **Model Training**: The model training stage mainly includes the **Training** time for performance models.
- **Performance-aware PNR Inference**: The performance-aware PNR inference includes the model **Inference** time and a single **augmented PNR** process.

Figure 11 presents a case study focusing on the lifecycle for building a performance model on Operational Transconductance Amplifier (OTA) layout design.



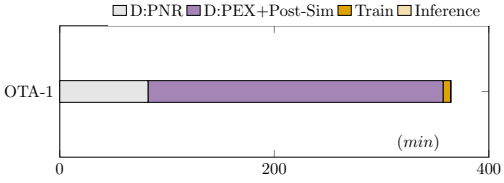
(a)



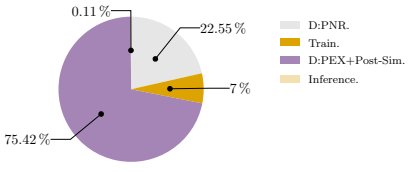
(b)

The runtime breakdown of different methods on OTA1 benchmarks.

Observations from Case 1



(a)



(b)

The runtime breakdown of different methods on OTA1 benchmarks.

We can draw two important observations from Case 1:

1. The **Data Collection** occupies **most** of the modeling lifecycle, which accounts for 92.89%.
2. The time required to obtain **inputs** << the time required to obtain **labels**. (*The PEX and Post-Sim time is roughly equivalent to 3-4 PNR iterations.*)

How to shorten the performance modeling lifecycle effectively?

Reduce the time spent on data acquisition, especially PEX and Post-Sim.

There are several promising solutions:

- From advancements in hardware-accelerated EDA workflows[10], we can see that parallelizing PEX and Post-Sim is an effective solution.
- Considering the cost of acquiring data inputs and labels, selecting representative samples through active learning[11] may also be an economically efficient approach.
- ...

[10] **Siting Liu et al. (2022). "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler". In:** *Proc. DATE*; **Zhuolun He, Yuzhe Ma, and Bei Yu (2022). "X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweepline Algorithms". In:** *Proc. ICCAD*.

[11] **Yuzhe Ma et al. (2018). "Cross-layer optimization for high speed adders: A pareto driven machine learning approach". In:** *IEEE TCAD* **38.12, pp. 2298–2311.**

Case 2: Exploring Model Transferability

In the case shown in the Table 1, we quantitatively discuss the issue of performance model transferability on OTA designs.

From Scratch

- A small amount of sampling data for the current design is collected.
- We then model the prediction as a binary classification problem to achieve accurate predictions[12].

Transfer

- The pre-trained model obtained from other designs is leveraged.
- We can obtain a relatively accurate model with a few samples through fine-tuning, which requires less time.

[12] **Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020b). "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning".** In: *Proc. DATE*, pp. 496–501.

Case 2: Exploring Model Transferability

We mainly consider two scenarios of Transfer:

Transfer between the same topology

- We first train a performance model on OTA3. **OTA3 has the same topology and different sizing configurations as OTA1.**
- We then test the accuracy of model predictions on OTA1.

Transfer between different topologies

- We first train a performance model on OTA3. **OTA3 has different topologies from OTA2.**
- We then test the accuracy of model predictions on OTA2.

Observations from Case 2

Table: Placement prediction results for training from scratch and transfer learning results.

Design	Prediction Accuracy Metrics	From Scratch	Transfer	Acc-Δ
OTA1	Offset Voltage(%)	**95.54**	91.67	3.87
	CMRR(%)	**91.96**	77.68	14.29
	BandWidth(%z)	**96.43**	95.54	0.89
	DC Gain(%)	**93.62**	88.01	5.61
	Noise(%)	**91.96**	79.14	12.82
OTA2	Offset Voltage(%)	**81.35**	65.39	15.96
	CMRR(%)	**82.33**	62.02	20.31
	BandWidth(%)	**80.71**	72.14	8.58
	DC Gain(%)	**81.35**	59.50	21.85
	Noise(%)	**88.80**	69.29	19.52

From these data results, we can identify two important findings:

- The transferability of the models varies under different scenarios and metrics, with the accuracy reduction ranging from 3% to 22%.
- Transfer between different sizing configurations is often easier than transfer between different topologies.

Lessons from the Performance Modeling Transferability

From a Generalization Perspective

- We consider how to improve transfer training by obtaining effective pretraining weights using methods like meta-learning[13].

From a Detection Perspective

- We consider different distributions to determine when the transfer is safe.
- Current research on out-of-distribution (OOD) detection[14] provides technical support for identifying when the model is effective.

[13] **Timothy Hospedales et al. (2021). "Meta-learning in neural networks: A survey".** In: *IEEE Transactions on Pattern Analysis and Machine Intelligence* **44.9, pp. 5149–5169**.

[14] **Qitian Wu et al. (2022). "Energy-based Out-of-Distribution Detection for Graph Neural Networks".** In: *Proc. ICLR*.

Case 3: Navigating the Multi-Objective Pitfall

In this case, we aim to demonstrate the importance of multi-objective optimization by comparing the placements obtained through weighted-based Bayesian optimization (BO) and multi-objective optimization Bayesian optimization (MOBO)[15] in four OTA benchmarks.

Weighted Method

- It is common practice to use a user-defined figure-of-merit (FOM) representation, a weighted sum of post-layout simulation metrics.

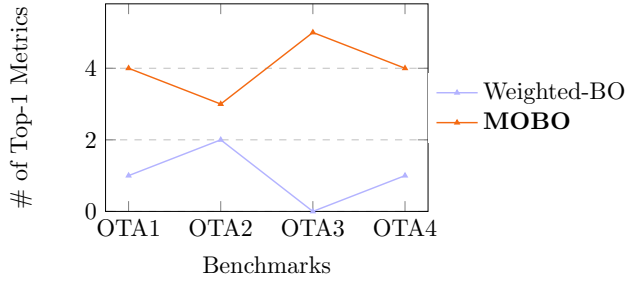
Multi-objective Optimization

- One alternative objective is to find solutions not dominated by others, known as **Pareto optimal solutions**.
- The problem of finding Pareto optimal solutions given multiple criteria is called **multi-objective optimization**.

[15] **Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020a). "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis".** In: *Proc. DAC*, pp. 496–501.

Observations from Case 3

As shown in Figure 13, the MOBO method outperforms Weighted-BO in terms of the number of top-1 metrics achieved for the obtained layout.



The number of top-1 metrics for different methods.

- MOBO achieves top-1 performance in almost all metrics in Offset Voltage, CMRR, BandWidth, and DC Gain.
- For all designs, MOBO outperforms the Weighted-BO for 3 to 5 metrics.

Lessons from the Multi-Objective Pitfall

- The results corroborate that the multi-objective optimization method moves the layout solution toward the Pareto frontier.
- Recent advancements have been witnessed in the field of multi-objective optimization, especially for **gradient-based strategies**[16].
- It is imperative to carefully consider how these advancements in the field of multi-objective optimization can be applied to enhance performance-driven analog layout automation.

[16] **Jörg Fliege and Benar Fux Svaiter (2000). "Steepest descent methods for multicriteria optimization".** In: *Mathematical Methods of Operations Research* 51, pp. 479–494; **Stefan Schäffler, Reinhart Schultz, and Klaus Weinzierl (2002). "Stochastic method for the solution of unconstrained vector optimization problems".** In: *Journal of Optimization Theory and Applications* 114, pp. 209–222; **Jean-Antoine Désidéri (2012). "Multiple-gradient descent algorithm (MGDA) for multiobjective optimization".** In: *Comptes Rendus Mathematique* 350.5-6, pp. 313–318.

Perspectives and Future Directions

Perspectives and Future Directions

- Our quantitative case study demonstrates important future directions in performance model training and physical design optimization.
- The need for efficient and performance-driven analog physical design calls for further research.
- In this section, we give our perspectives on the challenges and opportunities in future research in the field.

Efficient Data Acquisition

- Data collection bottleneck in building performance models;
- Active learning for selecting representative samples[17];
- Smart layout selection for an efficient training process;
- Accelerating simulation for more training data[18];

[17] **Yuzhe Ma et al. (2018). "Cross-layer optimization for high speed adders: A pareto driven machine learning approach".** In: *IEEE TCAD* 38.12, pp. 2298–2311.

[18] **Tengcheng Wang et al. (2023). "Accelerating Sparse LU Factorization with Density-Aware Adaptive Matrix Multiplication for Circuit Simulation".** In: *Proc. DAC*; **Dan Niu et al. (2023). "OSSP-PTA: An Online Stochastic Stepping Policy for PTA on Reinforcement Learning".** In: *IEEE TCAD* 42.11, pp. 4310–4323.

Better Transferability

- Transferring pre-trained models to unseen circuits Managing multimodal input features;
- A general multimodal neural network for performance modeling may benefit the field[19];
- Adopting a pretraining methodology for data efficiency[20];

[19] **Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020c). "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning".** In: *Proc. DATE*; **Yaguang Li et al. (2020). "A Customized Graph Neural Network Model for Guiding Analog IC Placement".** In: *Proc. ICCAD*.

[20] **Keren Zhu, Hao Chen, Walker J. Turner, et al. (2022). "TAG: Learning Circuit Spatial Embedding from Layouts".** In: *Proc. ICCAD*.

Placement and Routing Representation

- Placement and Routing Representation: An overlooked problem in ML-enabled performance-driven analog physical design is how to represent placement and routing. The work[21] treats the performance modeling as a black box.
- Bridging Placement and Routing Representation for Optimization: BO-based framework tunes net weights as a proxy to generate different placements in[22].

[21] **Yaguang Li et al. (2020). "A Customized Graph Neural Network Model for Guiding Analog IC Placement".** In: *Proc. ICCAD*.

[22] **Mingjie Liu, Keren Zhu, Xiyuan Tang, et al. (2020). "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis".** In: *Proc. DAC*.

Multi-objective Optimization

- Complexity of analog circuit performance
- Multiple competing performance metrics
- Efficient and effective multi-objective physical design optimization

THANK YOU!