Powering Innovation That Drives Human Advancement

Emag-Aware ML-Based Layout Optimization for High-Speed IC Design

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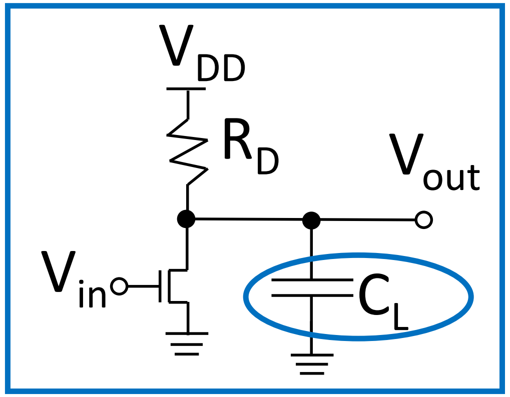
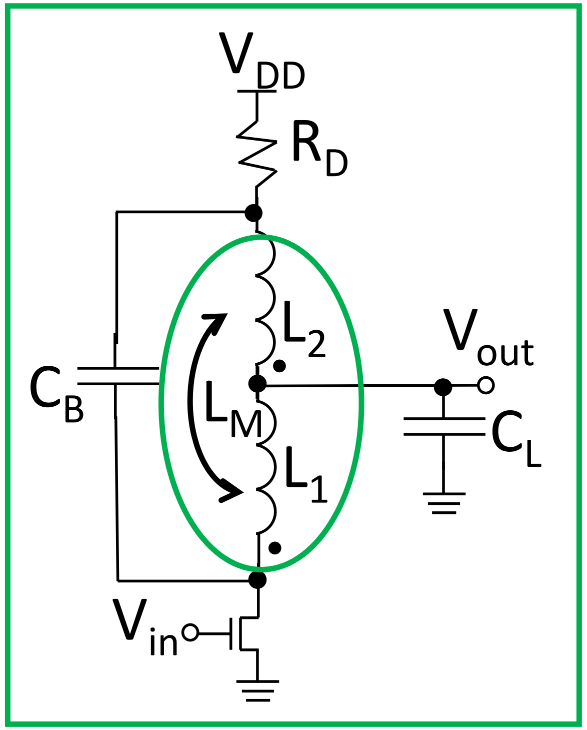
Overview

- Signal integrity challenges and solution of high-speed IO design
- Overview of memory read and write circuit using a single bump
- Traditional design approach and the drawbacks
- Proposed design approach using machine learning and the benefits
- Review of layout and circuit to be co-optimized
- Results of optimization
- Scaling to larger designs
- Summary

SI Challenge with High-Speed IO Design

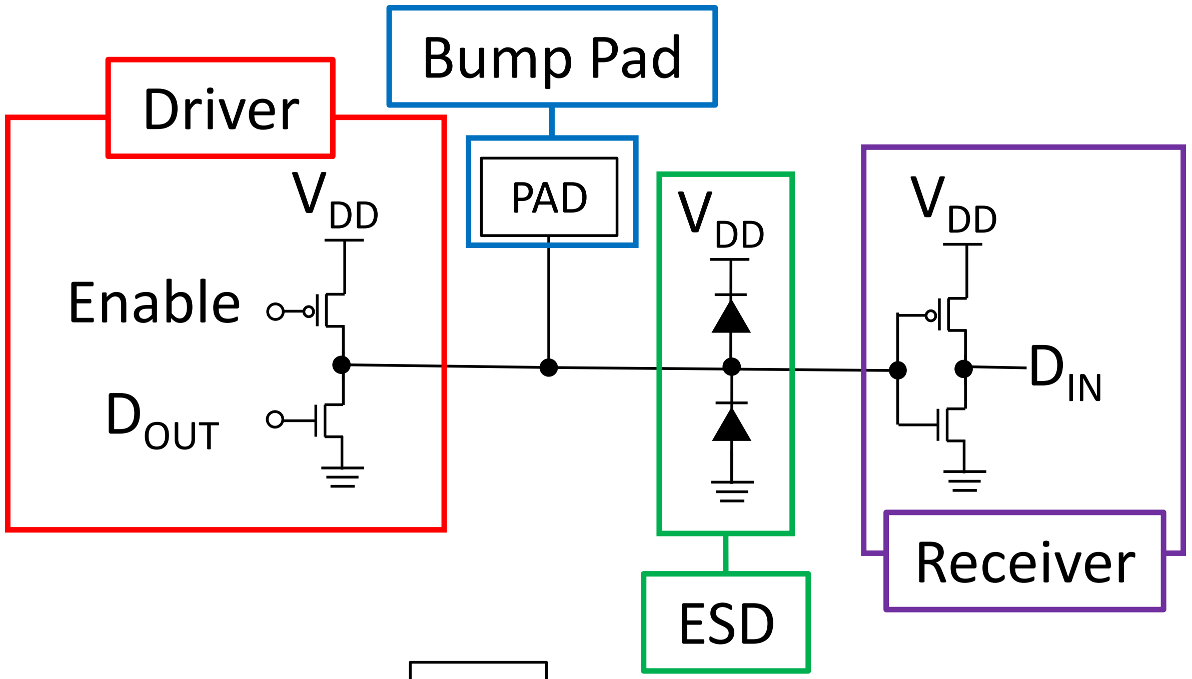
- Parasitic capacitance (C_L) limits bandwidth and eye opening
  - Electrostatic Discharge (ESD) protection
  - Solderbump pad and interconnect
  - Input capacitance of next stage
- Capacitance must be compensated for
- Tektronix pioneered T-coil use in 1940s, and the T-coil moved on die around 1990s
- T-coil advantages
  - Large bandwidth
  - Small size means low loss and high-density

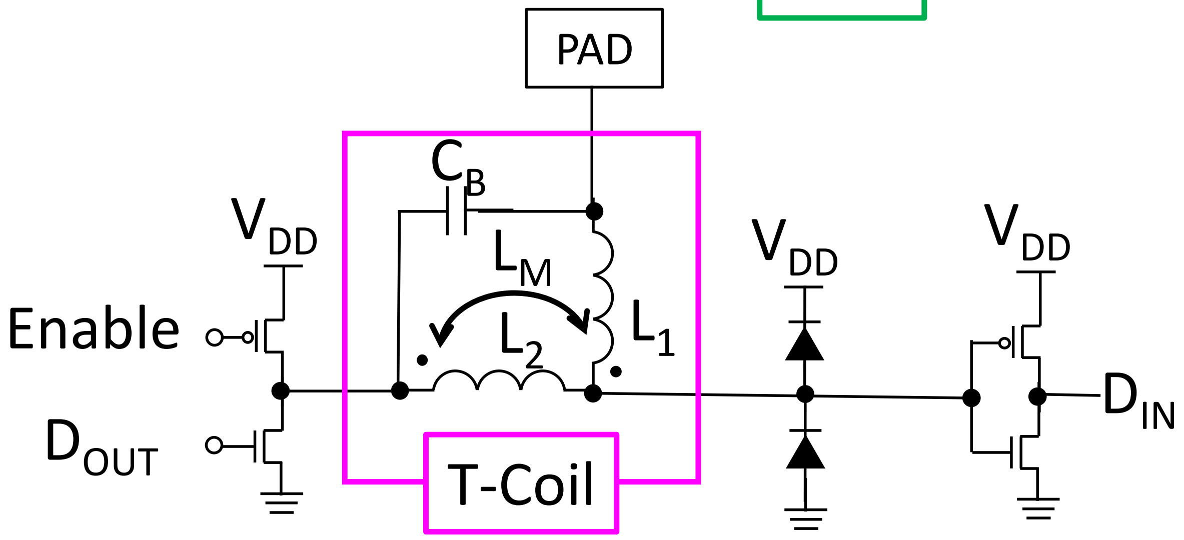




Bidirectional Pad

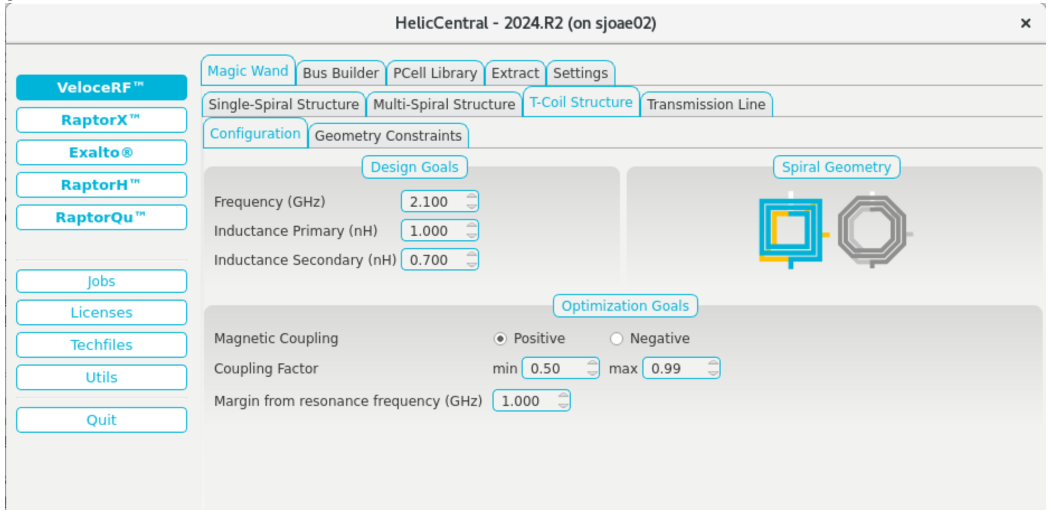
- For memory, data typically written and read from same pad
- ESD typically included in circuit
- Add T-Coil to compensate for:
  - Pad capacitance
  - ESD
  - Load of receiver
- Design degrees of freedom
  - Sign of coupling factor
  - Magnitude of coupling factor
  - Value of L_1, L_2, and C_B





Present Design Flow

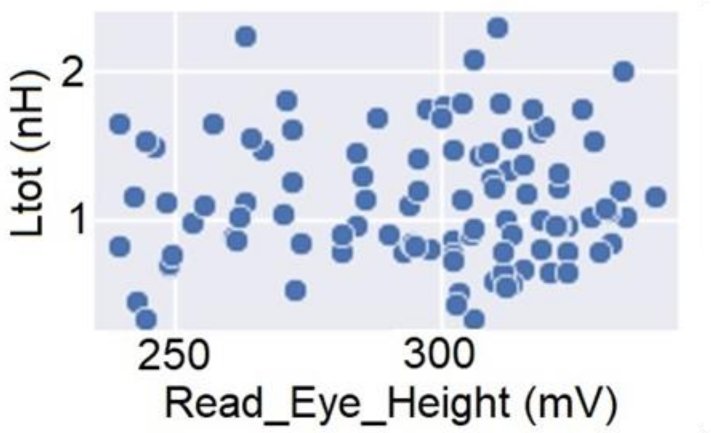
- Decide on values of L_1, L_2, C_B, and sign/value of mutual inductance (L_M)
  - Selected with SPICE analysis to minimize loss and/or maximize height of eye diagram
- Synthesize geometry by either:
  - Electromagnetic expert designs custom T-coil manually with EM tool such as RaptorX or HFSS
  - Use automatic T-coil synthesis tool like VeloceRF

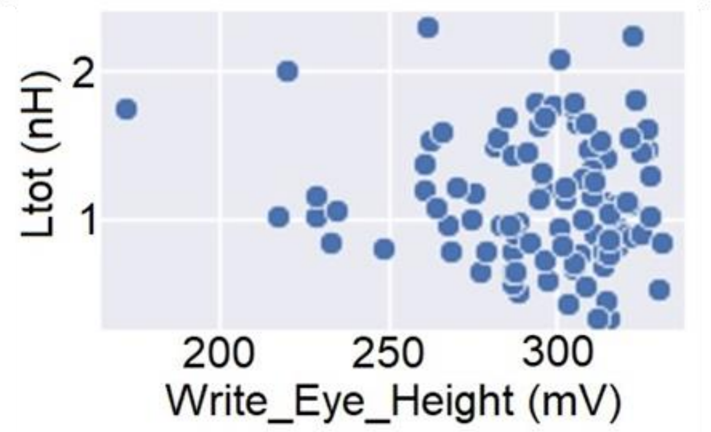


- Verify T-coil performance with SPICE analysis to confirm goal is achieved
- Iterate this loop until goal is reached

Drawbacks With the Present Design Flow

- Requires hard-to-find expertise
- Optimizing to auxiliary parameters
  - Often inductance is not correlated with design metric
- Optimized without consideration of environment
- Time consuming design flow for single T-coil means:
  - Locks in design of T-coil
  - Using the same T-coil for all IO pads
- Margin built into T-coil because:
  - Difficult to change later as layout progresses
  - Time consuming to customize for each IO pad



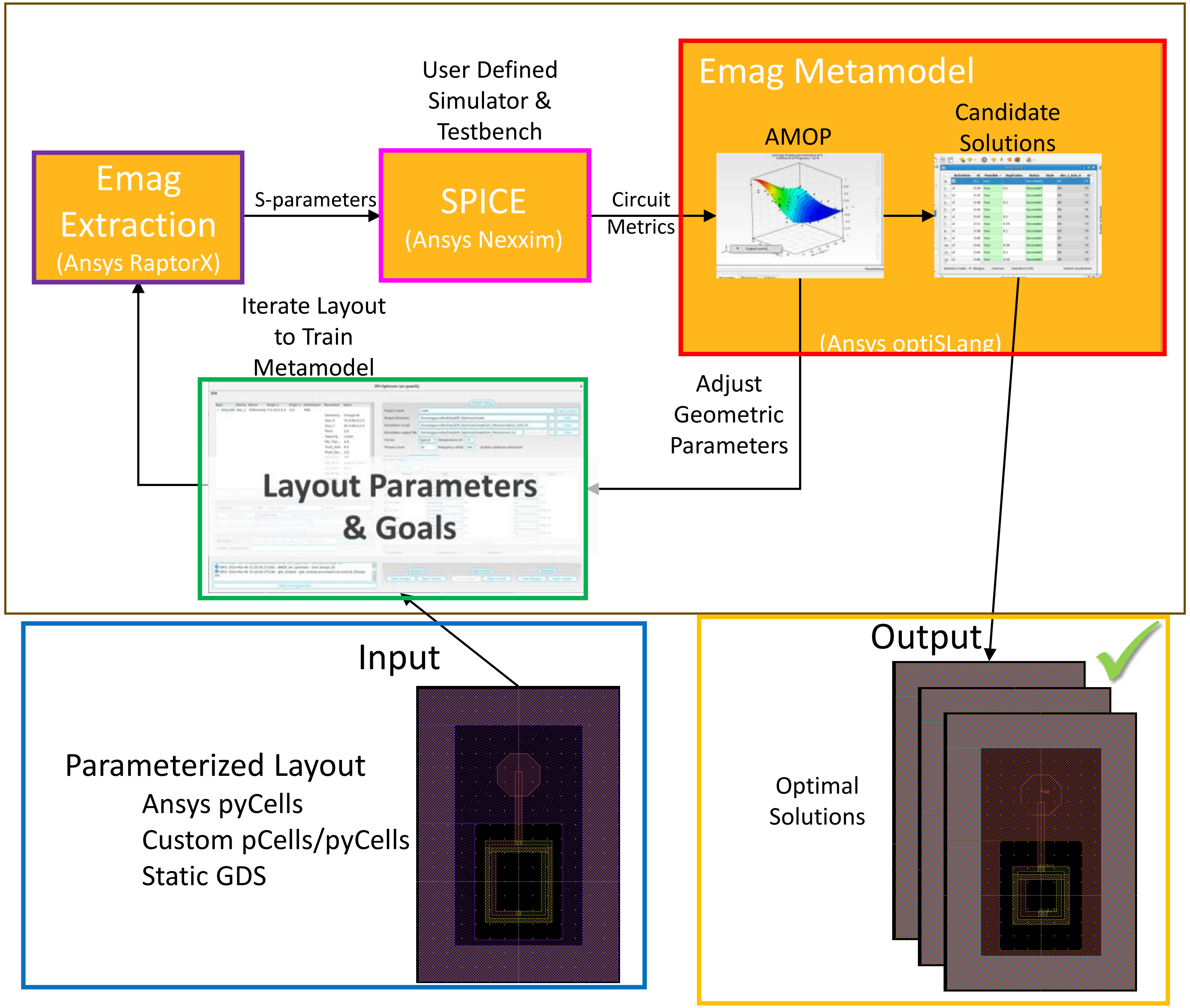


Requirements for Flow to Improve T-coil Synthesis

- Parameterized cells
  - This work uses the pCells from Ansys VeloceRF
- Electromagnetic extraction engine
  - This work uses Ansys RaptorX
- Arbitrary SPICE analysis
  - This work uses Ansys Nexxim
- Optimization algorithm
  - This work uses an adaptive metamodel of optimal prognosis (AMOP)
- Software to synchronize all tools
  - This work uses Ansys optiSLang

Proposed Optimization Flow

- Build layout to be optimized
- Define optimization goals and size of space to optimize over
- Perform training loop:
- Repeat training loop until metamodel training is completed
  - Speed up training by running EM extractions in parallel
- Select optimal answer
- Validate with EM extraction



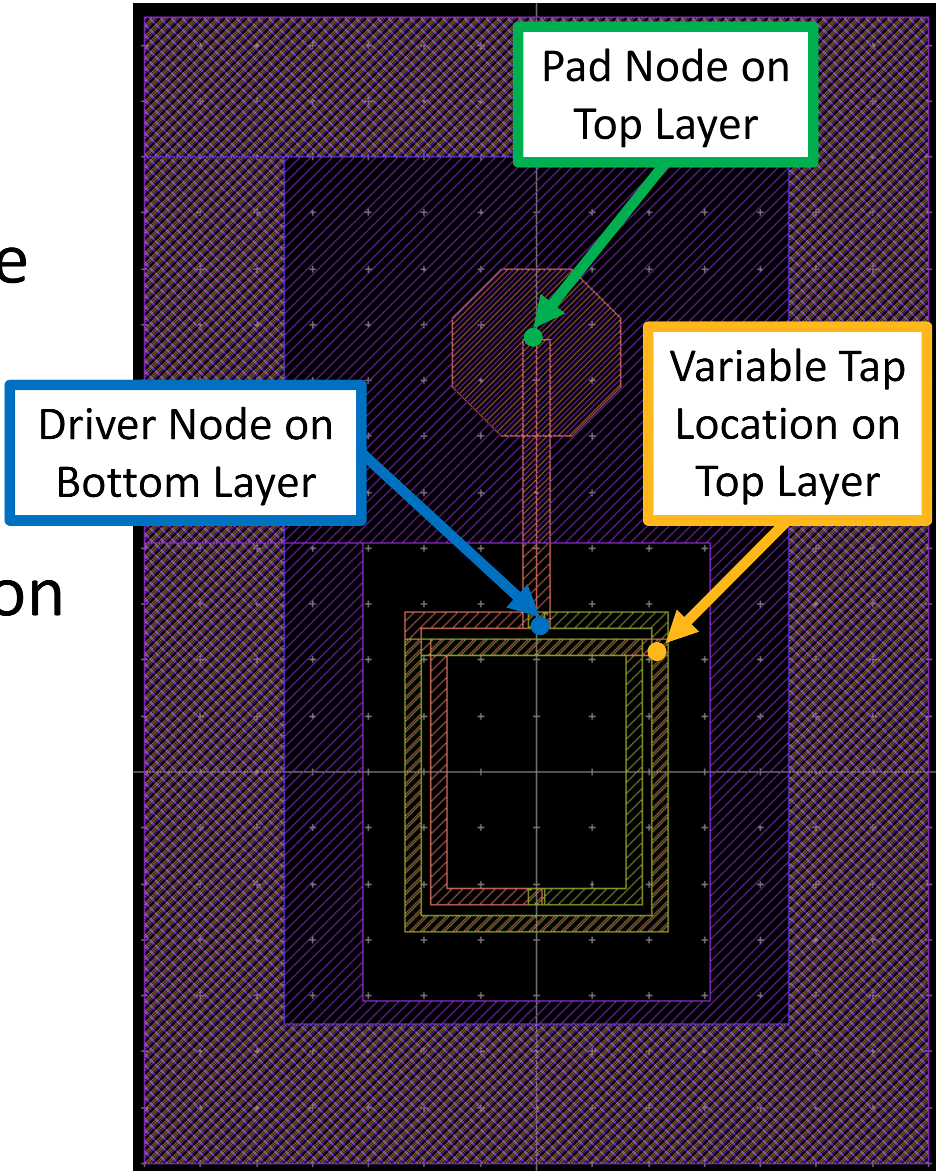
Benefits of Automation

- Automates design of T-coil
  - Reduces time required of engineers
  - Reduces error from manual work
  - Reduce the need for an electromagnetics expert
- AMOP adaptively finds the parameters the design is most sensitive to
  - Minimize computationally expensive electromagnetic extractions
  - Select different metamodel for each output parameter for optimal accuracy
- Trained metamodel useful for fast what-if analysis
- Finds optimal design based on desired circuit metrics
- Revisit optimization again when environment around T-coil changes as design evolves

Starting Design

- Using 7nm process
- Place T-coil on top two metal layers to minimize resistance
- Representative power/ground around spiral
- Bondpad and interconnect included in extraction
- Constrain coil to fit in 60 μm x 80 μm hole

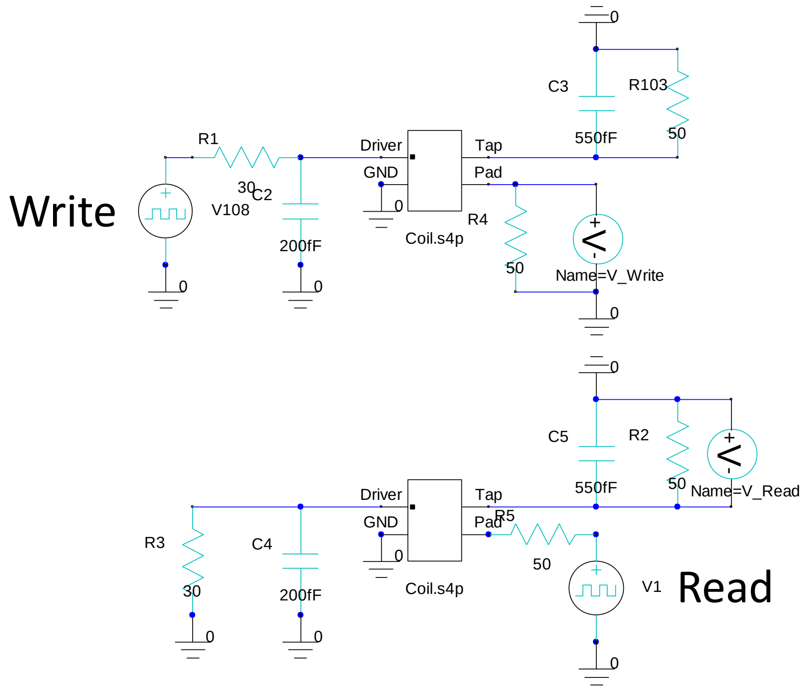
Parameter	Range
X dimension	35 - 60 μm
Y dimension	35 - 80 μm
Line Width	1.8 – 4.0 μm
Number of Turns	1 – 2.5 (step of 0.5)



SPICE Testbench

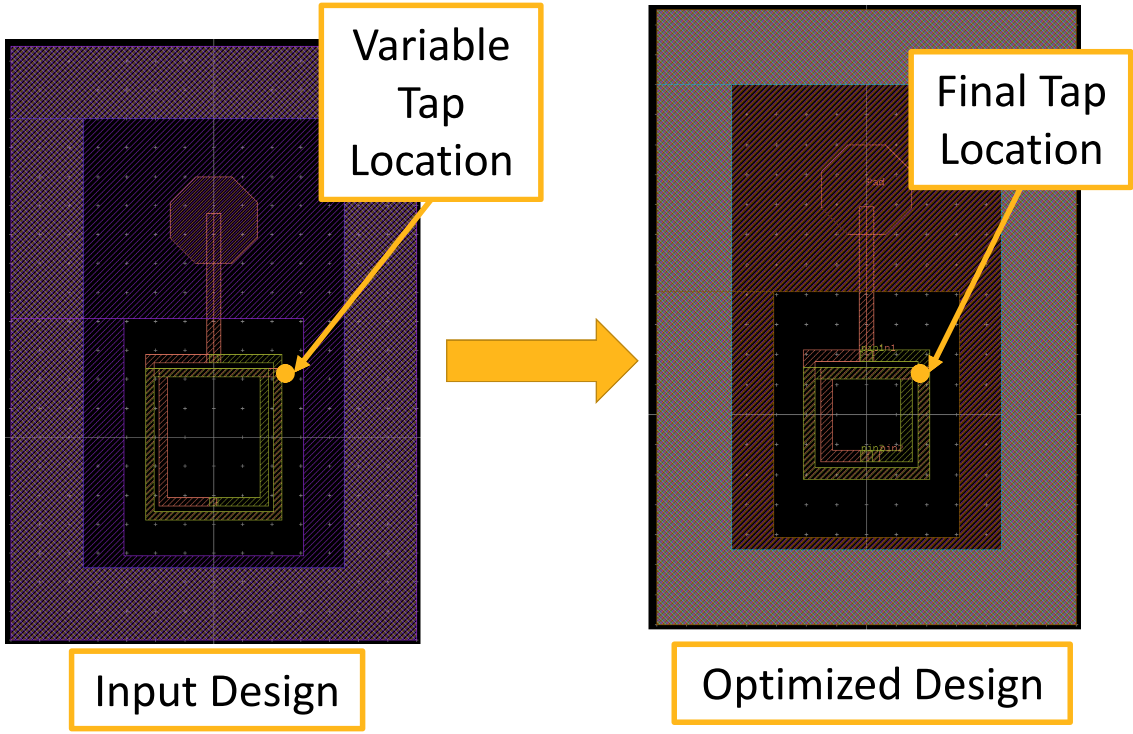
- S-parameters from electromagnetic extraction
- Extract read and write direction simultaneously
- Add capacitance to model:
  - Output capacitance of driver
  - ESD capacitance
  - Input capacitance of receiver
  - Generic source (with terminating impedance) with a 2^{18}-1 PRBS data stream
    - Can use driver/receiver models instead of simple capacitance as design progresses

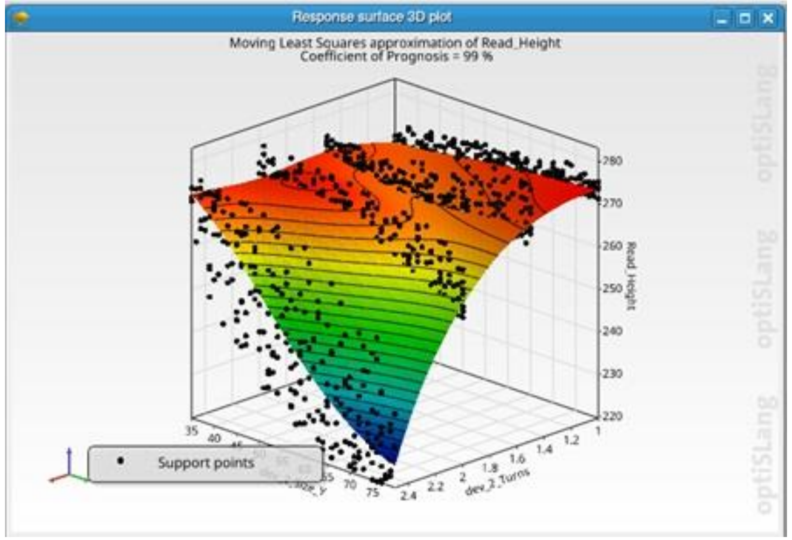
- **Time domain**: Maximize eye height for 9.6 Gbps
- Circuit used to find eye height



Optimization Results

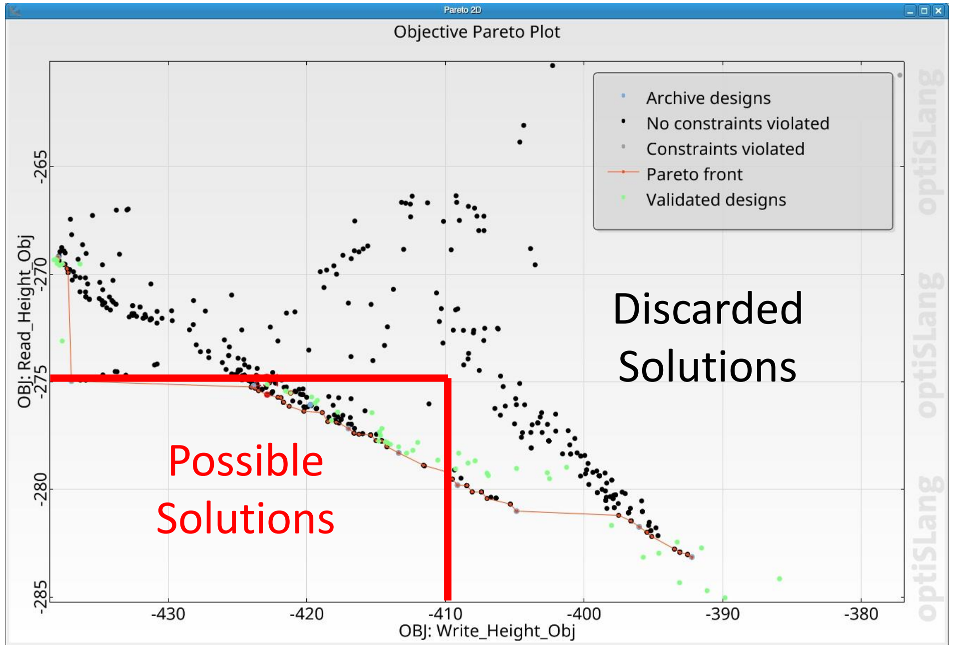
- Train model using 10 parallel RaptorX runs
- Use 8 threads per run
- Total optimization time: 253 min (4.2 hrs)
- Spiral is 37μm x 35 μm :
  - Line Width: 3.6 μm
  - Line Spacing: 1.8 μm
  - Turns: 1.5

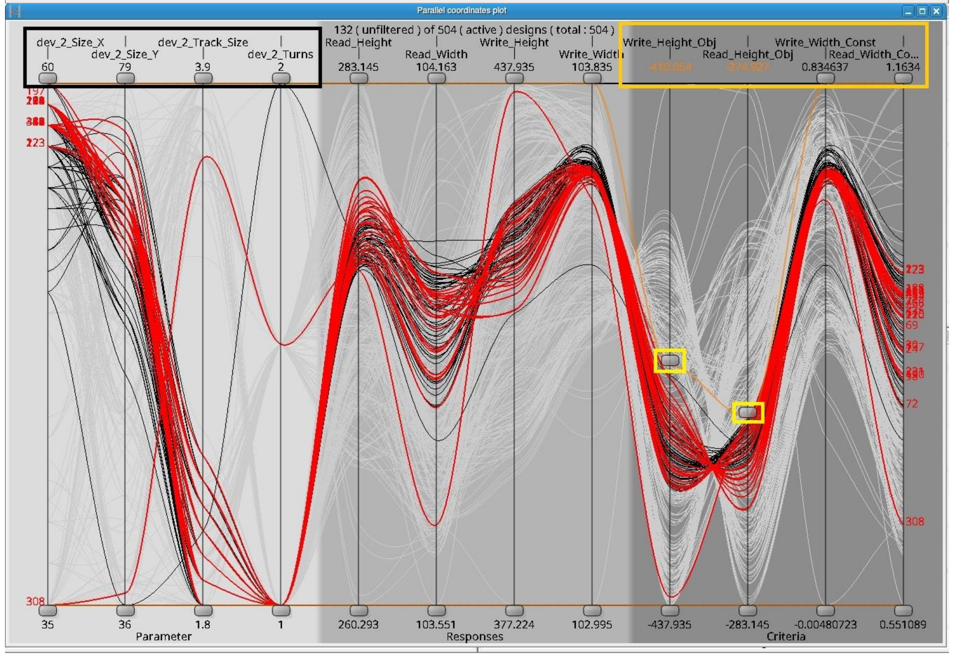




Exploring Trade-Off

- See contention between eye height in read direction vs. write direction with Pareto plot
- Quickly explore which designs may hit minimum targets with parallel plots
- Instantaneously identify trends and trade-offs in space to find best possible solution
- Extract metamodel generated layout with RaptorX to demonstrate accuracy of metamodel prediction





	Metamodel	RaptorX	Difference
Read Eye Height	274.96 mV	273.10 mV	-0.7%
Write Eye Height	436.98 mV	437.65 mV	+0.2%

Scaling to Eight Neighboring T-Coils

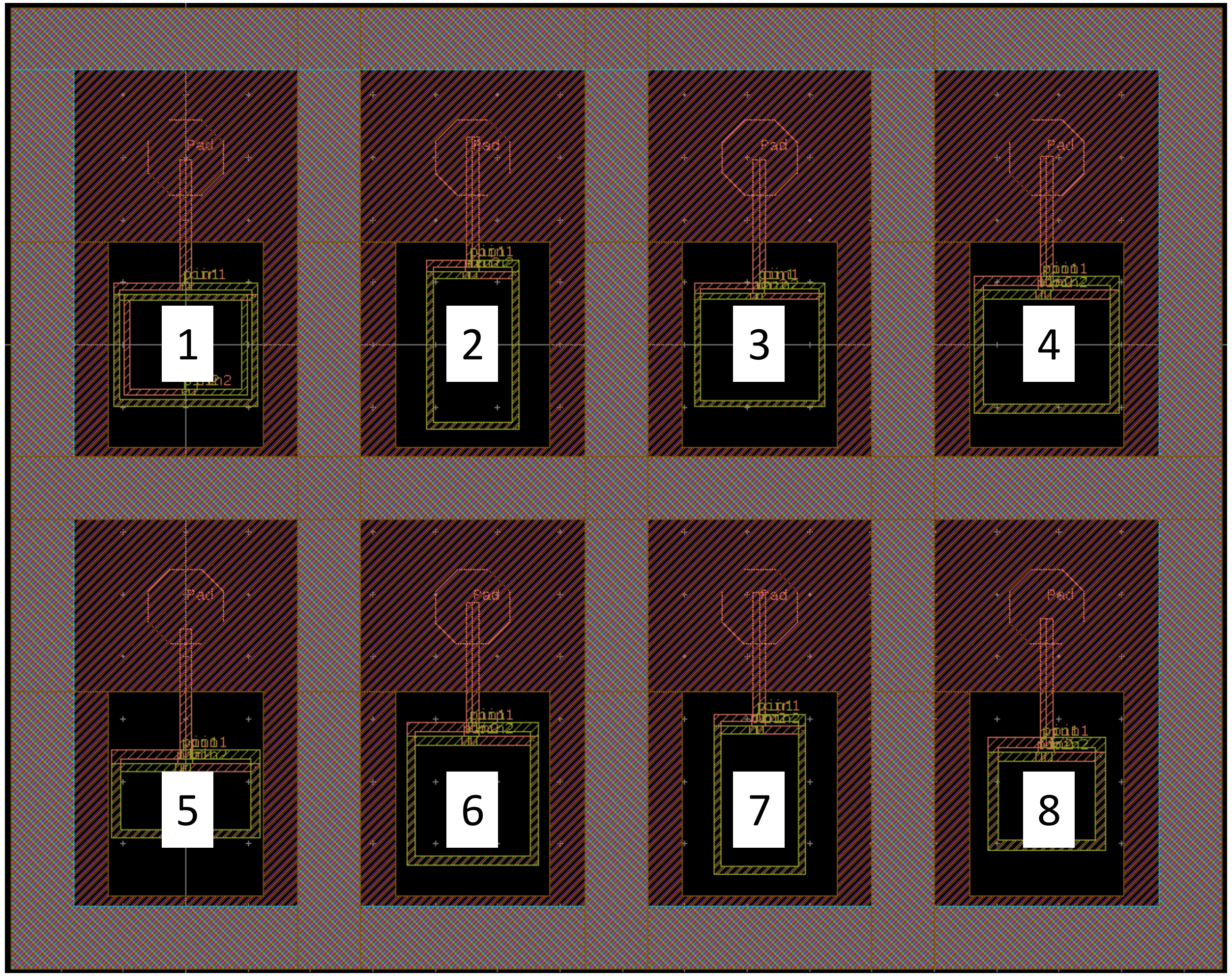
- Representative power/ground around spiral
- Constrain coil to fit in 60 μm x 80 μm hole
- Sweep all coils independently
- Modify SPICE testbench to accommodate eight coils giving each source a different data stream

Parameter	Range
X dimension	35 - 60 μm
Y dimension	35 - 80 μm
Line Width	1.8 – 4.0 μm
Number of Turns	1 – 2.5 (step of 0.5)

Results of Optimization

- Results include crosstalk and surrounding metal
- Total optimization time: ~19 hours
  - 10 Extractions in parallel
  - 8 threads each

Coil 1	Coil 2	Coil 3	Coil 4
X = 37 μm Y = 40 μm LW = 3.2 μm N = 2.5	X = 44 μm Y = 38 μm LW = 3.8 μm N = 1.0	X = 49 μm Y = 70 μm LW = 2.5 μm N = 1.0	X = 49 μm Y = 37 μm LW = 2.1 μm N = 1.0
Coil 5 X = 60 μm Y = 38 μm LW = 3.0 μm N = 1.0	**Coil 6** X = 51 μm Y = 46 μm LW = 2.7 μm N = 1.0	**Coil 7** X = 44 μm Y = 52 μm LW = 3.8 μm N = 2.0	**Coil 8** X = 42 μm Y = 52 μm LW = 3.7 μm N = 1.0

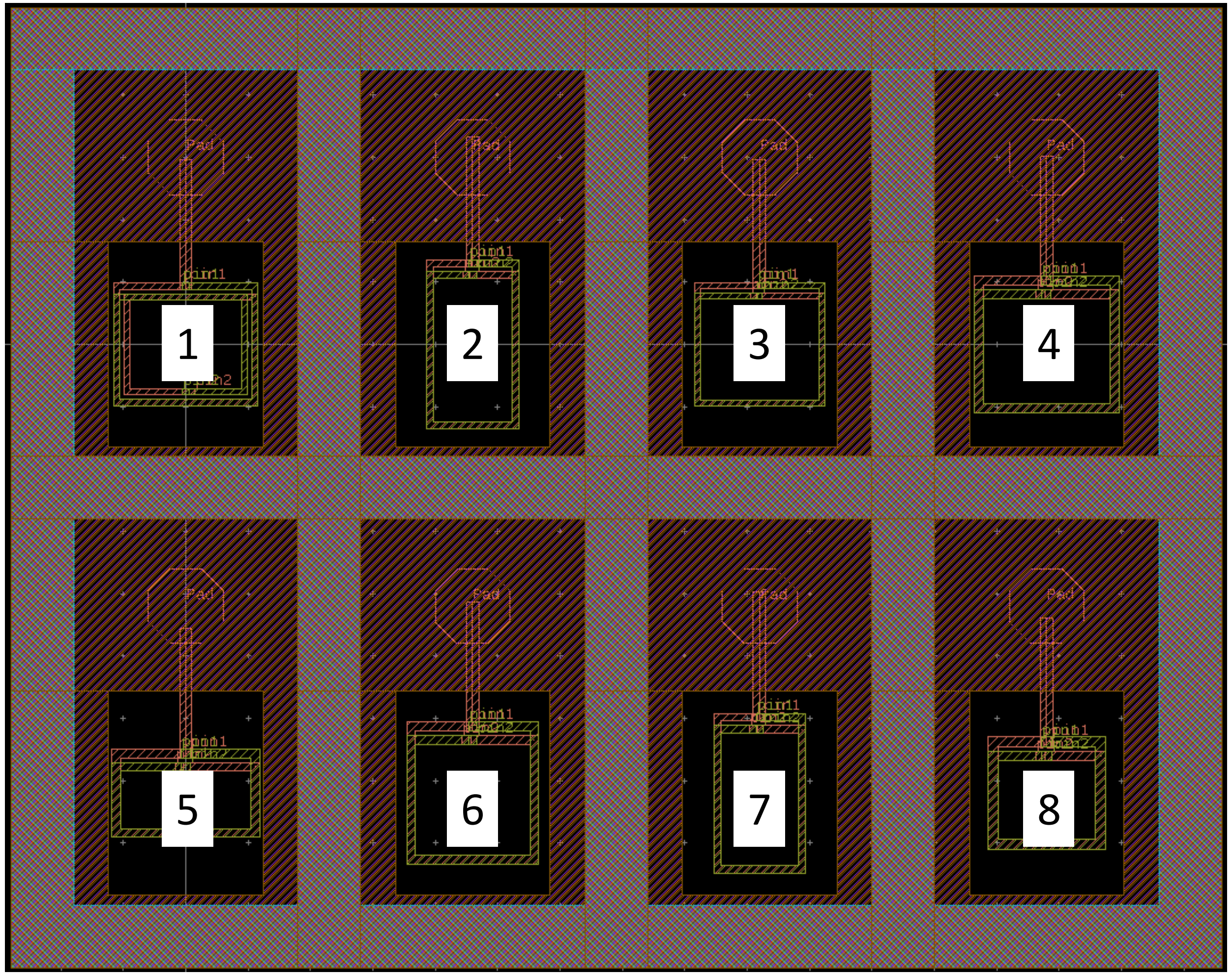


Accuracy of Prediction

- EM extraction vs metamodel prediction
- Difference range: -0.2% to +1.7 %

Read Eye Height	Metamodel	RaptorX	Difference
Coil 1	272.88 mV	272.36 mV	-0.2%
Coil 2	266.41 mV	266.42 mV	0%
Coil 3	271.26 mV	274.32 mV	1.1%
Coil 4	269.30 mV	271.66 mV	0.9%
Coil 5	266.827 mV	271.23mV	1.7%
Coil 6	269.15 mV	271.33 mV	0.8%
Coil 7	268.91 mV	270.20 mV	0.5%
Coil 8	266.47 mV	268.51 mV	0.8%

Write Eye Height	Metamodel	RaptorX	Difference
Coil 1	415.53 mV	417.44 mV	0.5%
Coil 2	432.73mV	434.03 mV	0.3%
Coil 3	420.37 mV	424.94 mV	1.1%
Coil 4	427.638 mV	429.12 mV	0.3%
Coil 5	426.75 mV	433.60 mV	1.6%
Coil 6	428.82 mV	432.99 mV	1.0%
Coil 7	415.46 mV	420.00 mV	1.1%
Coil 8	430.03 mV	435.45 mV	1.3%



Summary

- T-coils common way to extend bandwidth for high-speed IOs
- Traditional approach synthesizes coil manually based on auxiliary parameters (e.g., self and mutual inductance)
- Proposed ML design approach automates the layout synthesis which optimizes geometry based on the actual metric of interest (e.g., eye height)
- Demonstrated flow on a single coil for a memory interface
- Trained metamodel allows for instantaneous exploration of design trade offs if design goals are in contention
- Demonstrated scaling by optimizing entire byte lane
- Easy to extend to other designs:
  - Gain and noise figure of LNA, etc.