Analog Circuit Transfer Method Across Technology Nodes via Transistor Behavior

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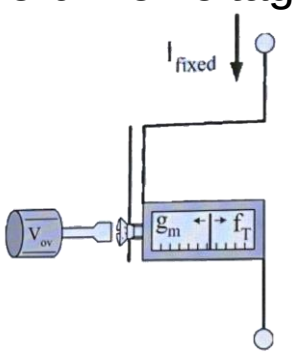
Content

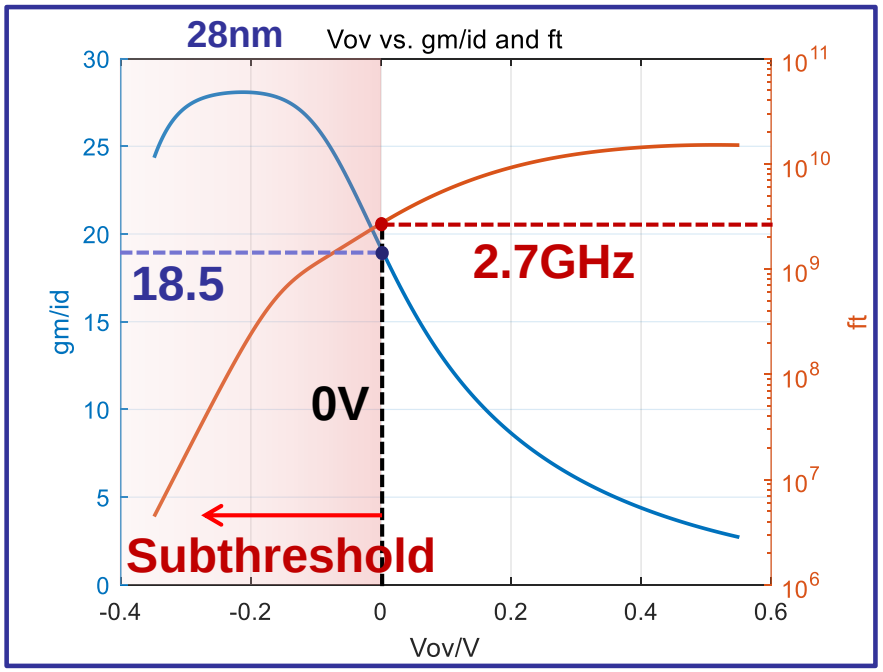
- Preliminaries
  - Linear circuit sizing methodology
  - Limitations of g_m/i_d design approach
  - Challenges in design methodology
- Framework
- Experimental Result
- Conclusions

Linear Circuit Sizing Methodology

V_{ov} -based

Overdrive voltage





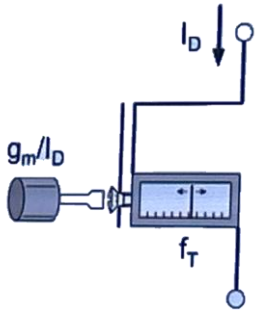
Preset V_{ov} (V_{GS} - V_{th}) to sizing

W = **L***gm/(u*C***Vov**)>0 !

***28nm, ft<2.5GHz, Vov<0**
Vov method fails.

V_{ov} fails in subthreshold region

g_m/i_d -based



Preset g_m/i_d to sizing

Saturation

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_d}{V_{GS}-V_{TH}}$$

$$\frac{g_m}{I_d} = \frac{2}{V_{GS}-V_{TH}}$$

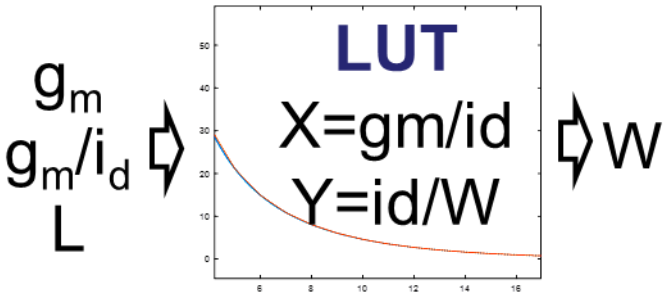
Sub-Threshold

$$g_m = \frac{\frac{W}{L}I_{ds0}e^{\frac{\gamma(V_{gs}-V_{th})}{nkT}}}{n\frac{kT}{q}} = \frac{I_{ds}}{n\frac{kT}{q}}$$

$$\frac{g_m}{I_d} = \frac{1}{n\frac{kT}{q}}$$

The g_m/i_d-based Sizing Methodology

- **step0. Build LUT**: g_m/i_d vs. i_d/W
- **step1. Set *g_m***: calculate g_m-GBW relation from schematic
  - e.g. $g_m=2\pi*GBW*C_L$
- **step2.Preset *L***
  - High-speed: L=min, high gain: L=max
- **step3.Preset *g_m/i_d***
  - Based on noise & swing requirements
- **step4. Calculate i_d&W**: extract W from i_d/w vs. g_m/i_d LUT



g_m/i_d&L selection experience-dependent, unscaling

Summary: Design Methodology

g_m = ***f*** (GBW, C_L,… given by the spec.)

Vov

Assuming a **V_{ov}** and **L**;

W = **L***gm/(u*C***Vov**)

Analytical Approximation

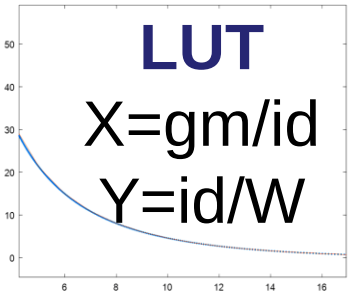
$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

gm/id

Assuming a **g_m/i_d** and **L**;

W = ***LUT*** (gm,**gm/id**,**L**);

g_m
i_d
L



W

- Subthreshold: PVT variations amplified exponentially, need to keep V_{ov} always >0, remains intuitive as overdrive voltage
- G_m/i_d method extends design space to weak inversion region
  - Process-dependent g_m/i_d and L selection
  - Less intuitive parameter (No unit) selection (even for V*)

Content

- Preliminaries
  - Linear circuit sizing methodology
  - Limitations of gm/ID design approach
  - Challenges in design methodology
- Framework
  - Invoke f_T: Transistor behavioral circuit representation
  - TBCR-based sizing methodology
  - Analog circuit transfer method across technology nodes
- Experimental Result
- Conclusions

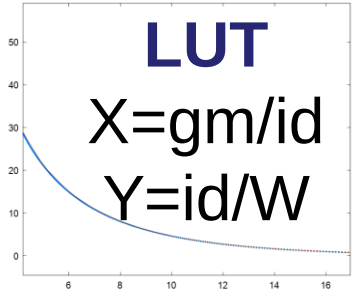
Challenge

- To identify a design-centric parameter that minimizes the process-dependent variations in g_m/i_d.
- To develop a dynamic optimization method that calculate optimal g_m/i_d and L based on PVTs, thereby leveraging the advantages of g_m/i_d methodology.

$g_m = \boldsymbol{f}\,(GBW, C_L, \ldots)$

g_m is only related to design and specifications

g_m
g_m/i_d
L



W

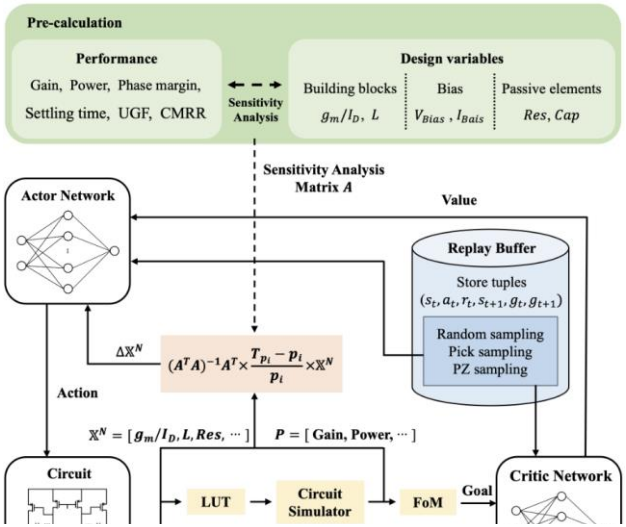
g_m
X

G()

W,L

X: decouple with size and technology

DAC2023, g_m/I_D-RL



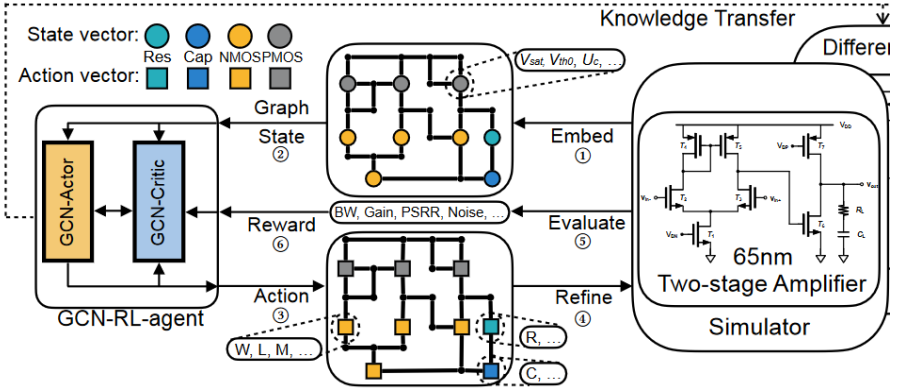
$$s_t = [\cdots, g_m/I_{D_i}, I_{Bj}, L_k, Res_l, C_m, \cdots]$$

g_m
g_m/i_d
L
⇨ **LUT** X=gm/id Y=id/W ⇨ W

Pros: g_m/i_d closely related to the performance of the circuit.

Cons: g_m/i_d and L process-dependent

DAC2020, GCN-RL



$$[0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, V_{sat}, V_{th0}, V_{fb}, \mu_0, U_c]$$

V_{sat}, V_{th0}
V_{fb}, μ
U_C
⇨ **GCN Actor& Critic** ⇨ W,L

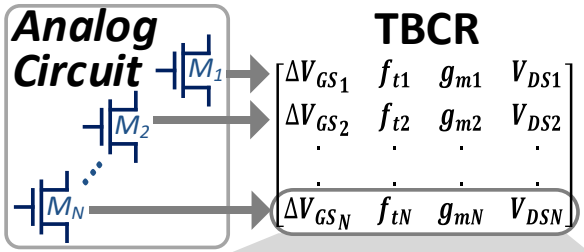
Cons:

1.Lots of parameter with unclear performance relationship

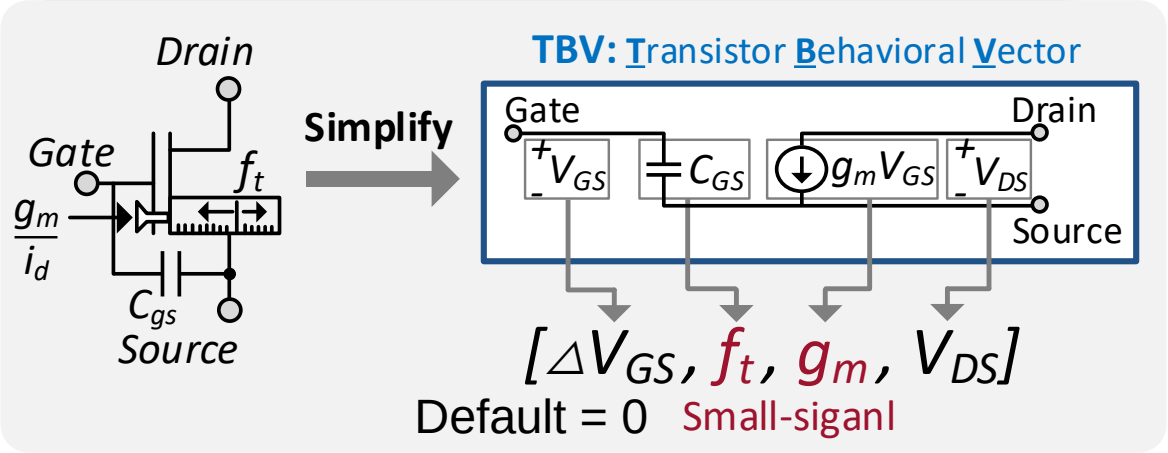
2.Model was not scaling

F_T-Based Methodology

gm = f(GBW, CL,…); ⇨ gm / f_t ⇨ **TBM()** ⇨ W,L



Parameter	Range in 22nm Tech.	Expression	Correlation
$g_m(A/V)$	[2e-7, ∞)	$\sqrt{2\mu C_{ox}\frac{W}{L}I_{ds}}$	$\sqrt{W/L}$
$f_t(Hz)$	[1e8,1e11]	$\frac{3\mu I_{ds}}{2\pi g_{m0}L^2}$	$1/L^2$
$\Delta V_{GS}(V)$	[-0.15,+0.15]	$\sqrt{\frac{4\pi f_{t0} g_{m0} L^3}{3\mu^2 C_{ox} W}}$	$L\sqrt{\frac{L}{W}}$
$V_{DS}(V)$	[0,0.8]	Non-analytic	$\sim L/W$



Design Example: 1MHz OTA

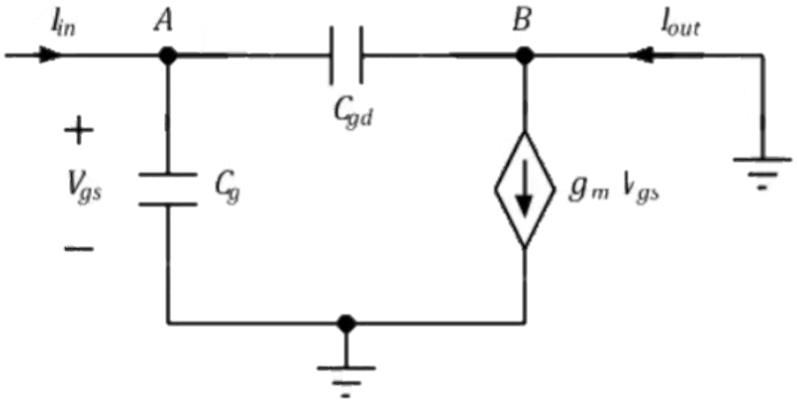
- Bandwidth limit by node's Cgs
- GBW = 1MHz → $f_t \approx$ 10MHz
- f_t solely determined by specs

g_m,f_t: key design metrics independent of technology.

ΔV_{gs}: bias point adjustment parameter, negligible (default=0).

V_{ds}: drain-source voltage for enhancing model accuracy.

Invoke F_T to Eliminate G_m/i_d and L



$$I_{in}(\omega) = j\omega\left(C_{gs} + C_{gd}\right)V_{gs}(\omega)$$

$$I_{out}(\omega) = \left(g_m - j\omega C_{gd}\right)V_{gs}(\omega)$$

$$\left|\frac{I_{out}(\omega)}{I_{in}(\omega)}\right| = \left|\frac{g_m - j\omega C_{gd}}{j\omega\left(C_{gs} + C_{gd}\right)}\right| = \frac{\sqrt{g_m^2 + \omega^2 C_{gd}^2}}{\omega\left(C_{gs} + C_{gd}\right)}$$

At low frequencies where $g_m >> \omega C_{gs}$:

$$\left|\frac{I_{out}(\omega)}{I_{in}(\omega)}\right| \approx \frac{g_m}{\omega\left(C_{gs} + C_{gd}\right)}$$

At high frequencies where $g_m << \omega C_{gs}$:

$$\left|\frac{I_{out}(\omega)}{I_{in}(\omega)}\right| \approx \frac{C_{gs}}{\left(C_{gs} + C_{gd}\right)}$$

The transition frequency can be derived:

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs}+C_{gd}} \approx \frac{g_m}{C_{gs}} \approx \frac{3\mu}{\frac{g_m}{I_d}L^2}$$

FT is combination of gm/id and L.

F_t represents the relationship between gate capacitances and transconductance, independent of W and the number of series-connected devices. Thus, ft can be used to substitute gm/id.

How to calculate g_m/i_d and L using f_t?

Physical Mechanism of F_T && Max. Self-gain

Main Concept: Find out which $\frac{g_m}{I_d}$ and L brings $\max_{\frac{g_m}{2\pi C_{gs}}=f_{t0}} g_m r_o$

Approximation 1: $r_o = \frac{1}{\lambda I_d}$, $\lambda \propto \frac{1}{L}$, $r_o \propto \frac{L}{I_d} = \frac{f(L)}{I_d}$

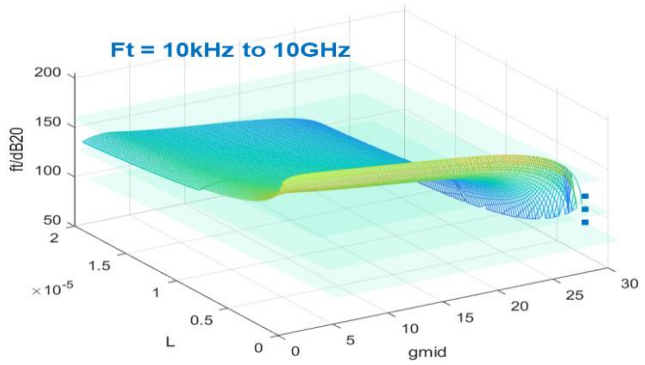
Approximation 2 : $\frac{\partial r_o}{\partial L} \xrightarrow{fixed\ Id} \frac{1}{I_d}\frac{\partial f(L)}{\partial L} > 0$

Result: Find optimal {gm/id,L} by $\begin{cases} \frac{g_m}{2\pi C_{gs}} = f_{t0} \\ max\{ f(L)\frac{g_m}{I_d}\} \end{cases}$

Two equations to get two parameters.

Solving F_T && Max. Self-gain

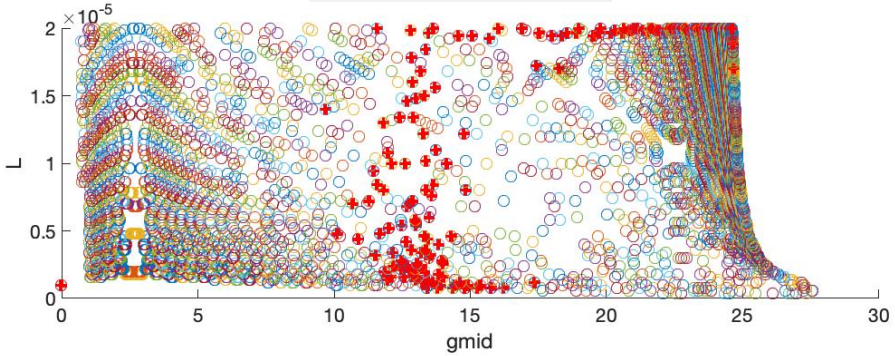
Sweep

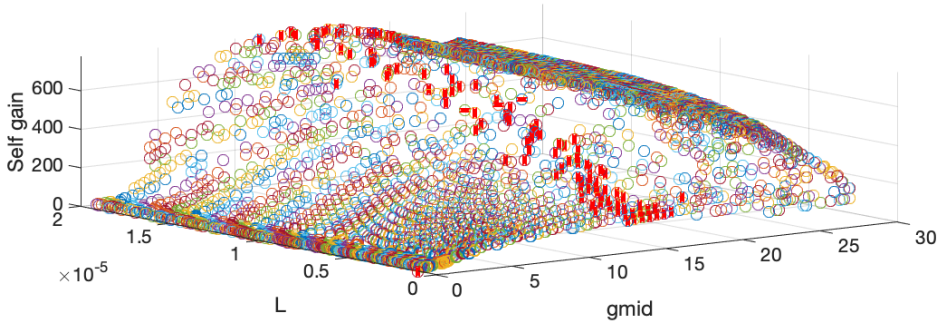


Surface Plot: ft vs {gmid, L}

Intersection points between the surface and reference plane.

Result





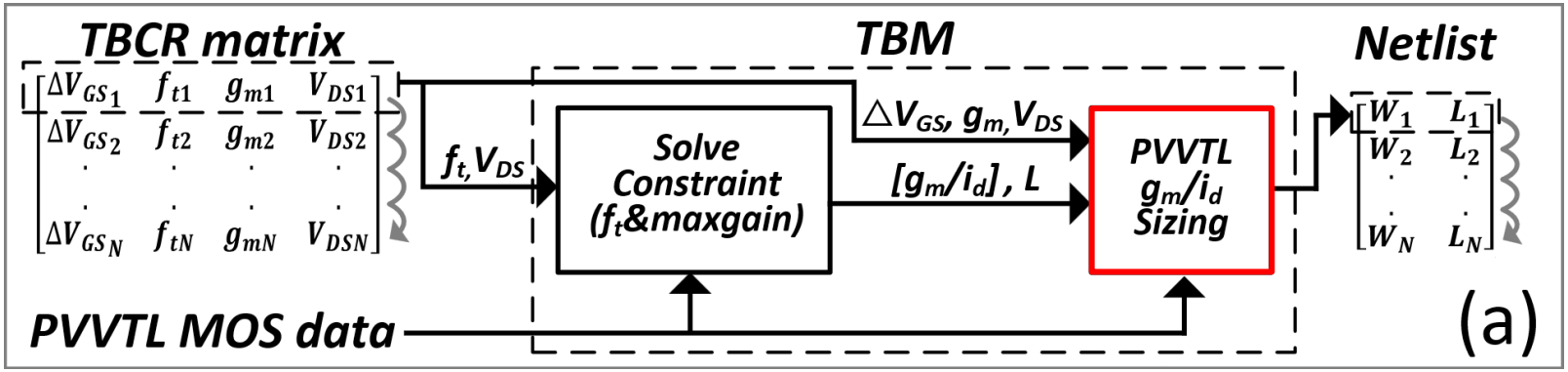
Belike

Circles: Valid solutions in the {gmid, L}

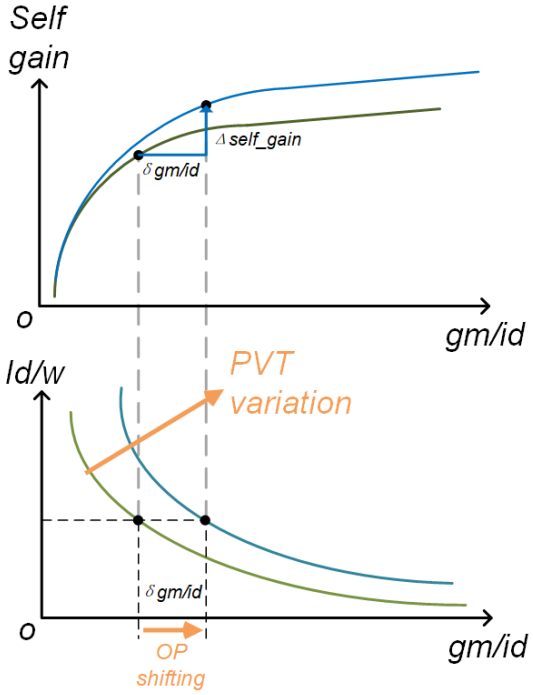
Red crosses: Points satisfying both ft and maximum self gain conditions

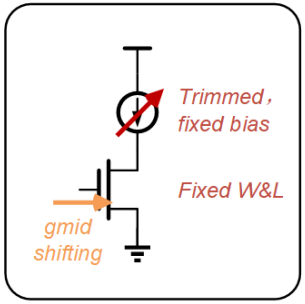
Find the strategy for minimum gain degradation in the (*gm/id, L*) while increasing f_t

g_m-worst Driven g_m/i_d Sizing Under PVTs



All PVT variations ultimately affect the current.
When both current and size are fixed, gm/id remains the only variable.



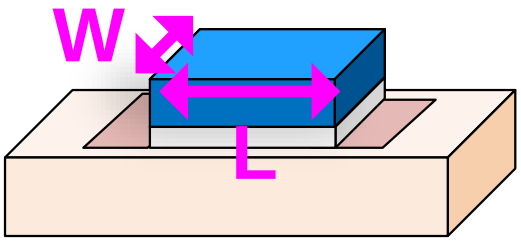


1. Find lowest id/w at worst-case corner with same gm/id
2. Evaluate avg. gm/id & assess performance metrics
3. Look-up: gm, vgt, vth, ro, Cgg, Cdd, n
4. Sizing at worst corner to meet gm specs

$$\Delta GBW = \frac{\Delta g_{m1}}{C_c} = \Delta g_{m1}\% \times GBW$$

Comparison of Size, G_m/i_d and F_T

W + L



· Enables comprehensive performance evaluation
-Significantly process-dependent

gm/id + L

g_m
g_m/i_d
L

⇨ **LUT** X=gm/id Y=id/W ⇨ W

· Direct correlation with g_m
- PVT sensitive
- Process-dependent

TBCR

g_m
f_t
V_{ds}
ΔV_{gs}

⇨ PVVTL MOS data → Solve Constraint (ft&maxgain) → PVVTL gm/id Sizing ⇨ W/L

· f_t as primary design parameter
· Intuitive and practically approach

Comparison

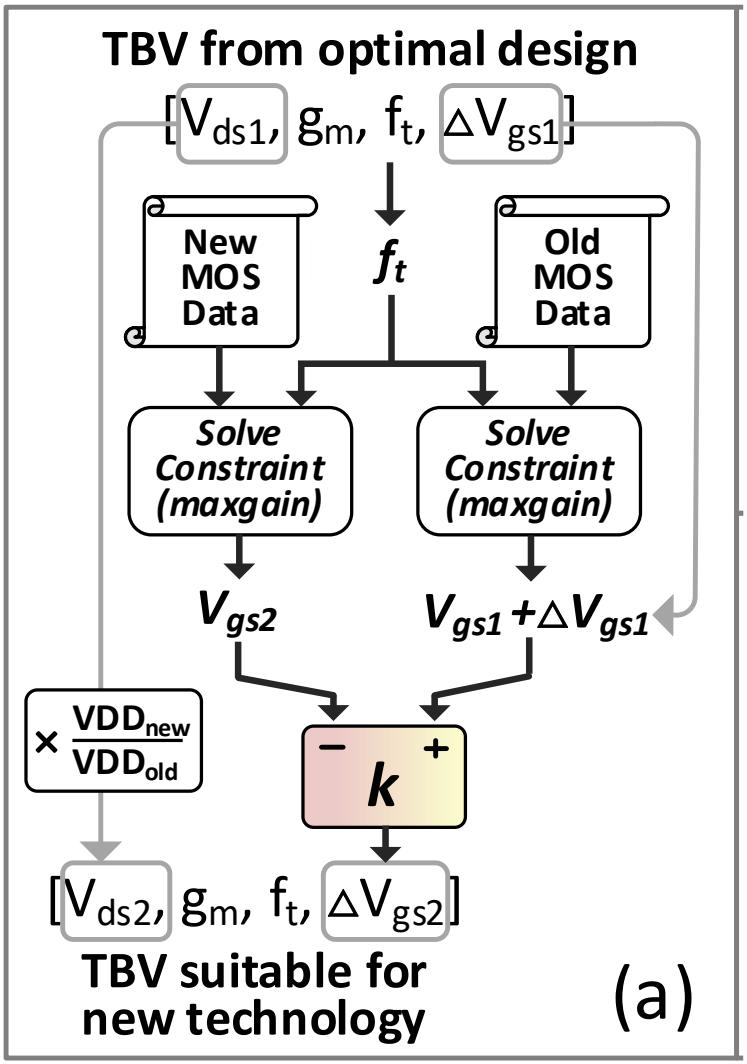
Full range of W&L → W&L (Vov) → gmid L → ft

Machine code → Assembly → C → Python

Optimal performance achievement ——— Intuitive usability

Calibration between Technology Node

The TBCR (ft-based) inherently independent to technology, all we need is **calibration.**



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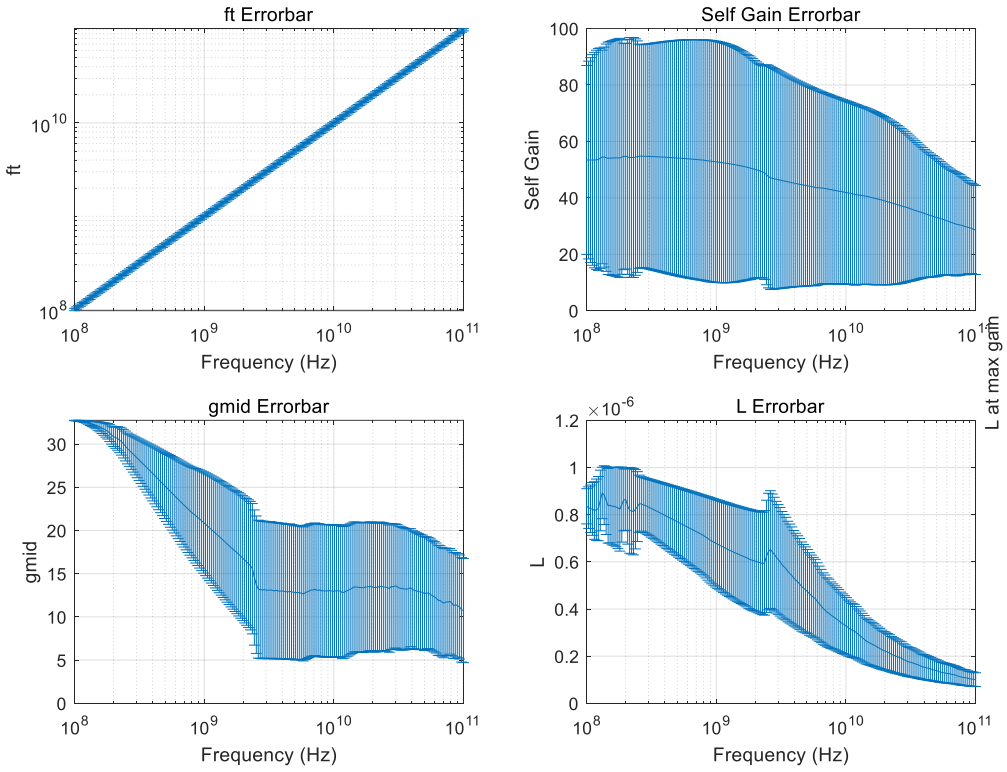
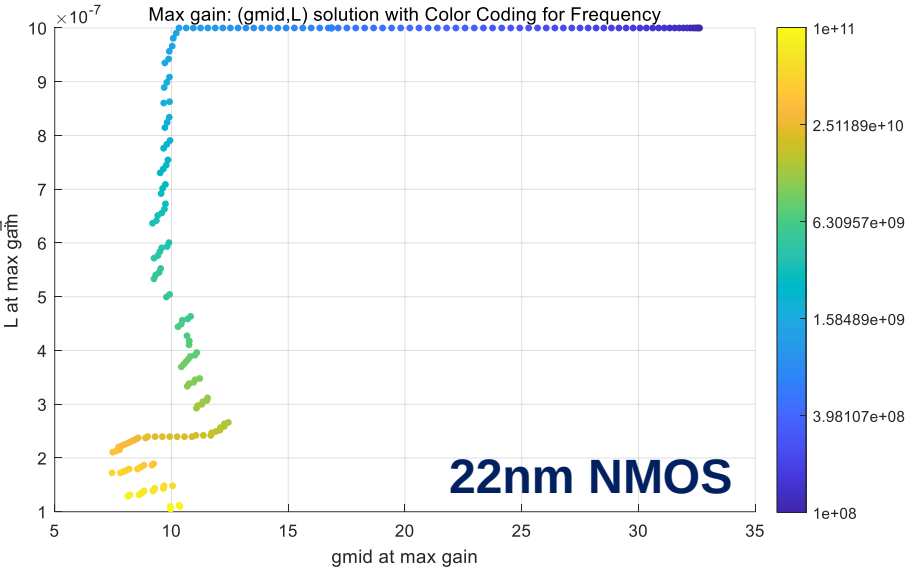
  - 3-Stage Amplifier Transfer
    - Implementation of 102 Cases with Identical Topology
    - Implementation of 300 Cases across Four Topologies
- Conclusions

TBCR F_T Analysis

Without Maxgain Constraints



With Maxgain Constraints



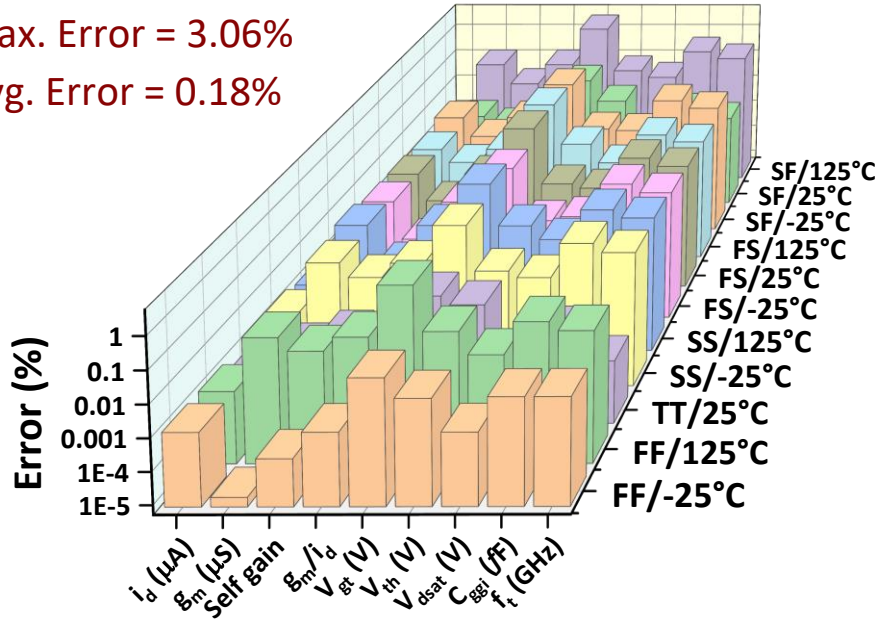
1. Multiple g_m/i_d, L solutions
2. Limited range at f_t extremes
3. ΔV_{gs} variation shown by error bars

1. Specific g_m/i_d, L solution
2. Simplified design at gm/id≈10
3. Conventional methodology alignment

Mapping Accuracy

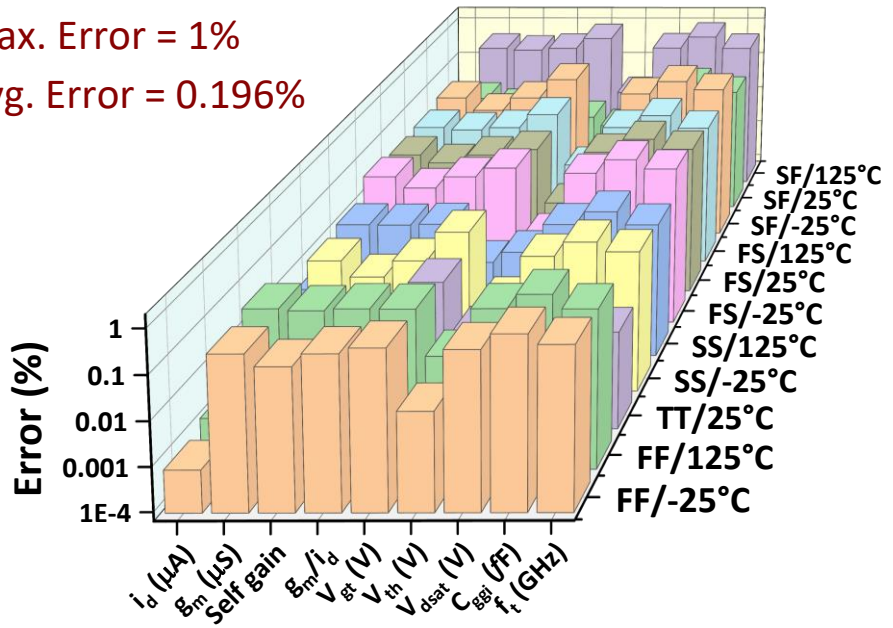
Model vs. Simulation
22*n*m ULVT *n*MOS g_m=1mS f_t=500MHz V_{DS}=0.4V

Max. Error = 3.06%
Avg. Error = 0.18%



Model vs. Simulation
180*n*m SVT *n*MOS g_m=1mS f_t=500MHz V_{DS}=0.9V

Max. Error = 1%
Avg. Error = 0.196%

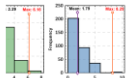


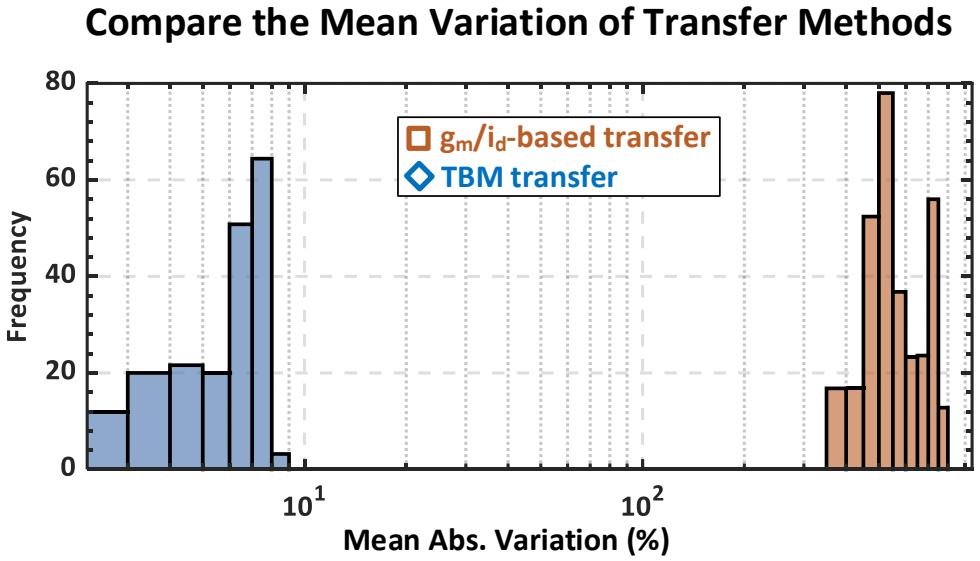
1. Error < 5% vs. SPICE simulation, comparable to MOSFET model KOP(Key output) fitting accuracy
2. Multiple PVTs ability & scalable

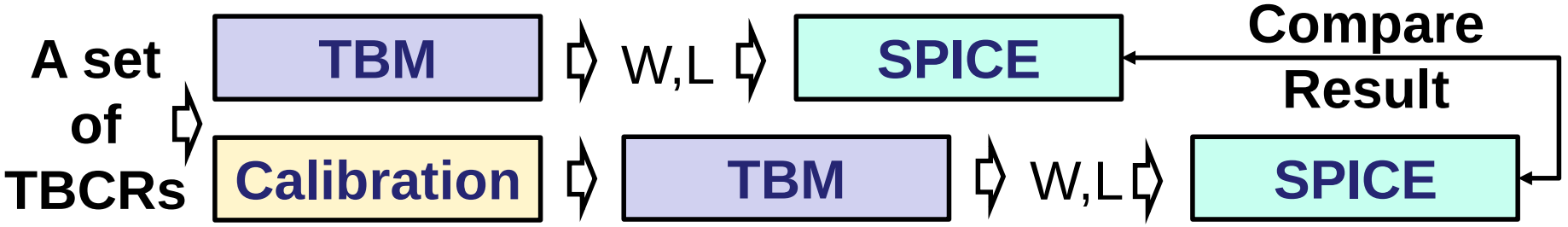
Transfer a n-MOSFET

Transfer Variation

g_m f_t

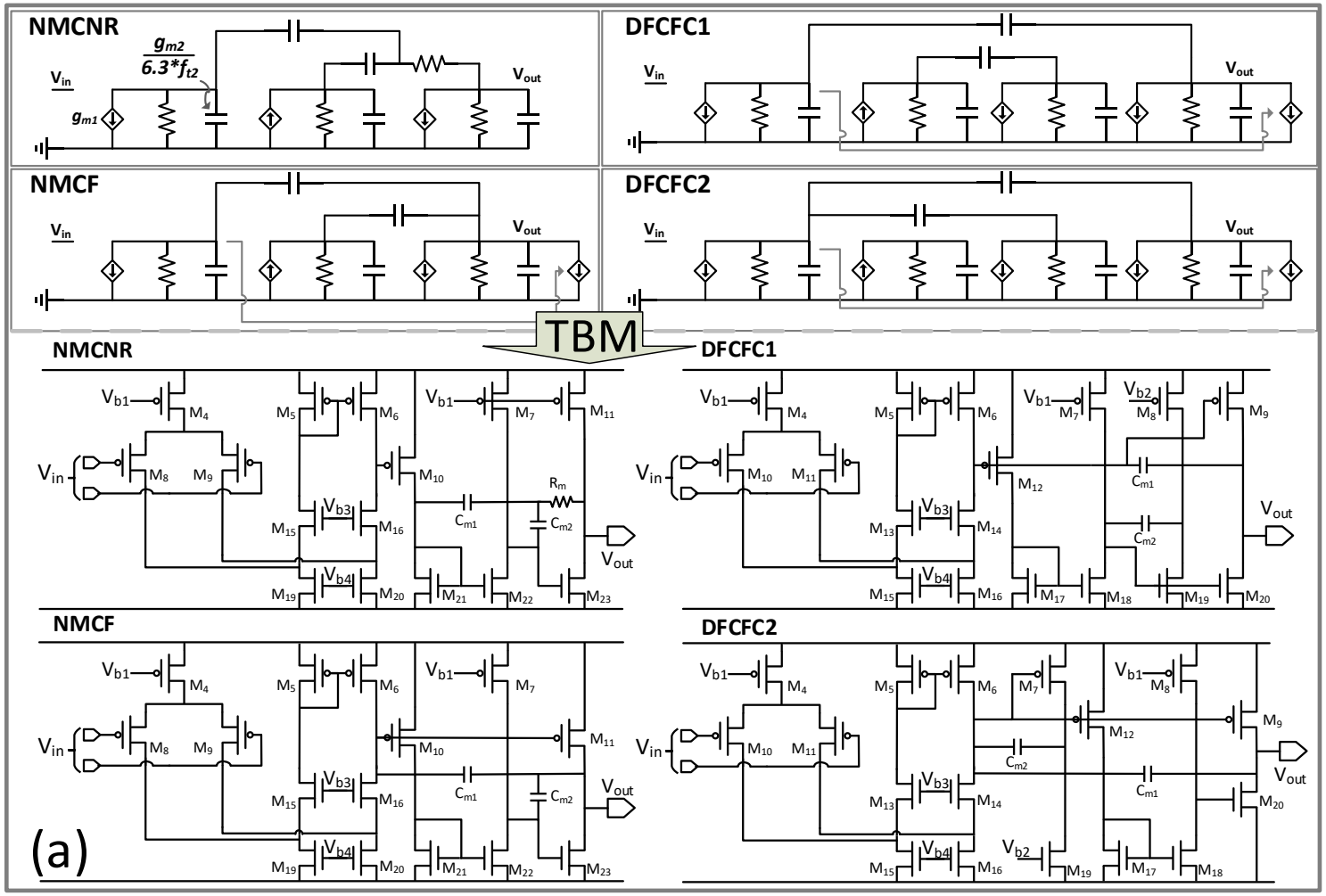






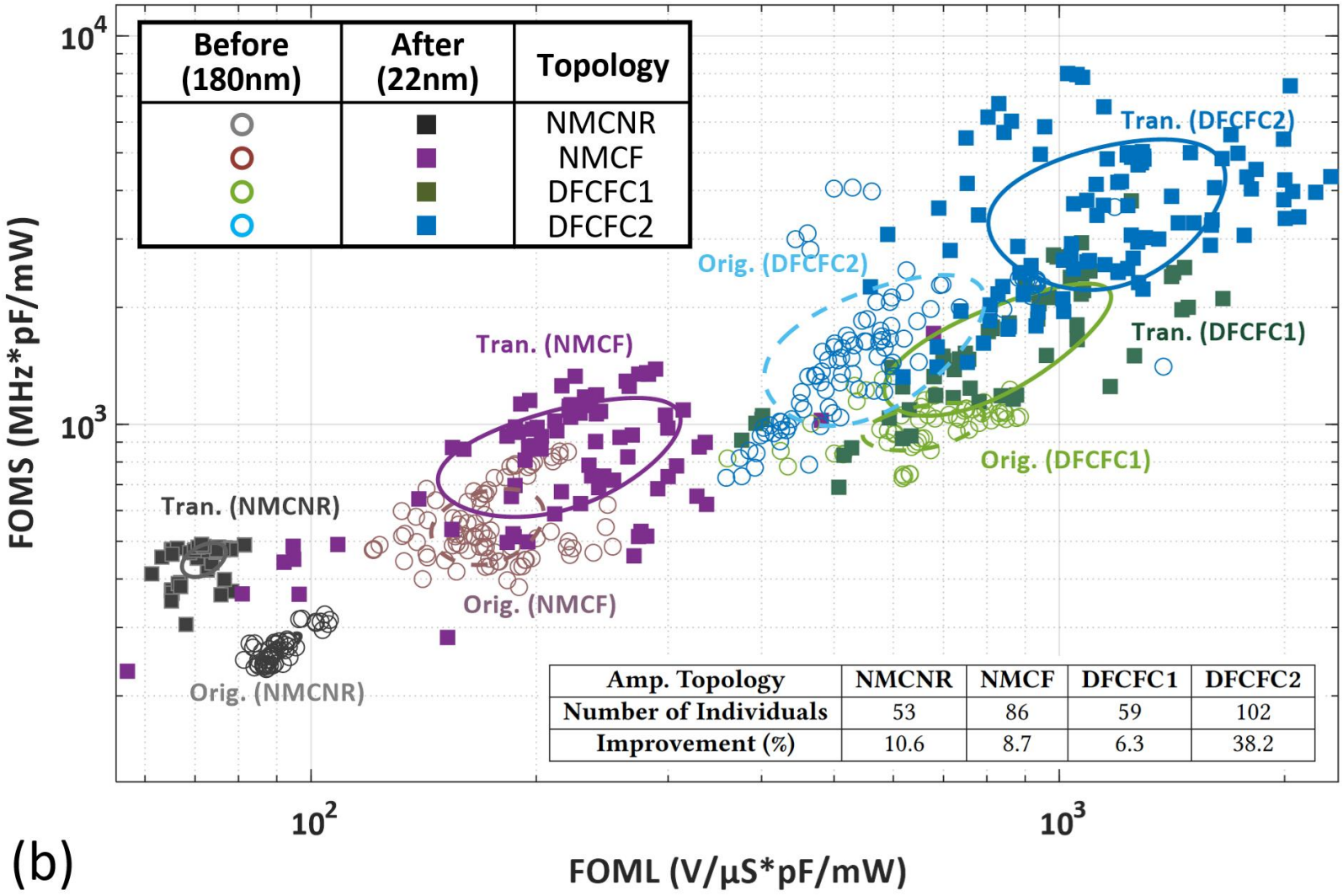
1. Calibration enables <10% variation (180nm→22nm)
2. Error was 96× lower than gm/Id method
3. TBCR shows cross-process ability

Implementation of 300 Cases across Four Distinct Topologies



Begins with small-signal circuit optimization, using TBM to get 300 individuals in different sizing, do it both in 180 and 22nm, then compare the result.

Implementation of 300 Cases across Four Distinct Topologies



Amp. Topology	NMCNR	NMCF	DFCFC1	DFCFC2
Number of Individuals	53	86	59	102
Improvement (%)	10.6	8.7	6.3	38.2

Cross-node scaling benefits: 6.3%-38.2% (VDD-driven)

Conclusion

- Novel Transistor Behavioral Circuit Representation (TBCR)
  - Technology-independent parameters: gm, ft, VDS, ΔVGS
- Enabling Technology Node Transfer
  - Analytical conversion from TBCR to transistor sizing
  - Verified across 180nm → 22nm nodes
- Key Advantages
  - Technology-independent circuit representation
  - Leverages scaling benefits

Thank you

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