



Fast Routing Algorithm for Mask Stitching Region of Ultra Large Wafer Scale Integration

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Outline

- Introduction
- Problem Formulation
- Technical Details
- Experimental Results
- Conclusion



- Ultra large wafer scale integration is promising for ultra-high performance computing applications, such as AI and super-computing.
- The area of interposer is increasing:
 - The interposer area of the TSMC CoWoS with 3.3X-reticle size is about 2700 mm² [1].
 - In the future, the area of interposers can be up to 5000 mm² [2].



[1] https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm.

[2] Hou et al., "Supercarrier Redistribution Layers to Realize Ultra Large 2.5D Wafer Scale Packaging by CoWoS," in ECTC, 2023.

Introduction

• Mask stitching technique is necessary for ultra large silicon interposer manufacturing.



(a) The illustration of ultra large silicon interposer. (b) The illustration of mask stitching technique.

 Mask
 Stitching Region

Introduction

Challenges

- Effectiveness:
 - solve special design rules.
- Efficiency:
 - tackle more than 10 thousands of signal nets.







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Problem Formulation

- Input:
 - Access point set, net set, RDL set.
- Output:
 - Connect two access points of each net by vias, wires, and a stitching wire.
- Objective:
 - Maximize routability and minimize wirelength.
- Design rule constraints:
 - Via location: access point location.
 - Stitching wire location: stitching region.
 - Required routing pattern.
 - Routing angle: 0° , 90° , or 135° .
 - Minimum spacing.



Routing region tuning

• prepare the tuned region for special routing patterns.

Routing algorithm w. conflict elimination

- Routing region initialization:
 - access point sorting.
- Conflict elimination:
 - layer-by-layer procedure.
- Fast legal routing:
 - candidate selection.



Routing region tuning

• prepare the tuned region for special routing patterns.



Figure 5: The illustration of routing region tuning. (a) Calculate the distances from each access point to the four boundaries. (b) Assign each point to corresponding boundaries. (c) Determine the tuned region candidates. (d) The final tuned region.

Routing algorithm w. conflict elimination

• Fast legal routing: candidate selection.



Figure 6: The illustration of the proposed routing algorithm. (a) The initialization before scanning the two access point lists. (b) Update the current stitching wire candidate based on the bounding box of the net (Policy (1)). (c) Generate the routing solution based on the smaller bounding box considering the required pattern (Policy (2)) and update data for the next net (Policy (3)). (d) Generate the routing solution for the second processed net and update data for the next net.

- Time complexity: O(nlogn).
 - For each layer, the time complexity of initialization: O(nlogn).
 - For each layer, the time complexity of candidate selection: O(2n).
 - For each layer, the time complexity of other operations: constant.
 - The number of layers is limited.

Algorithm 1: Mask Stitching Routing Algorithm Input: net set N, access point set AP, layer set L, and design parameters. **Output:** routing solution S. 1 $N_C \leftarrow N$; $2 AP_C \leftarrow AP;$ $3 N_L \leftarrow \emptyset$; 4 for each layer $l_i \in L$ do Generate the sorted stitching wire candidate set SWC ; 5 Generate two sub-set AP_S and AP_E of AP_C ; 6 7 Sort AP_S and AP_E ; Start access point $sp_i \leftarrow sp_1 \in AP_S$; 8 End access point $ep_k \leftarrow ep_1 \in AP_E$; 9 Current stitching wire candidate $swc_0 \leftarrow swc_1 \in SWC$; 10 while $i \leq |AP_S|$ do 11 12 if $k > |AP_E|$ then 13 ++j;14 Continue ; if the corresponding net of $sp_i \in N_L$ then 15 ++j;16 Continue ; 17 if sp_i and ep_k belong to different net then 18 $N_L \leftarrow$ the net corresponding to ep_k ; 19 ++k:20 Continue ; 21 Update swc_o ; 22 Generate the required pattern of the corresponding net of sp_i and 23 ep_k based on swc_0 ; ++ i;24 ++k; 25 ++o; $N_C \leftarrow N_L$; 27 $N_L \leftarrow \emptyset$; Update AP_C based on N_C ;

Experimental Results

- Compared with SOTA RDL routing algorithm [3]:
 - The general RDL routing algorithm is limited to achieve 100% routability due to small access point pitch.
 - The general RDL routing algorithm is limited to optimize wirelength due to the limited search space.
 - The general RDL routing algorithm is too complicated to achieve good efficiency.

Testcase	N	L	Routability (%)		Wirelength (µm)		Runtime (s)	
			Baseline	Ours	Baseline	Ours	Baseline	Ours
T1	110	4	99.00%	100.00%	> 644924.80	418837.31	1795.31	0.26
T2	112	4	98.00%	100.00%	> 561531.69	453781.26	1598.94	0.36
T3	220	4	99.00%	100.00%	> 1380668.07	896232.00	8438.95	0.35
T4	224	4	98.00%	100.00%	> 1388438.63	927169.23	7415.70	0.31
Ratio	-	-	0.99	1.00	-	1.00	14844.86	1.00

[3] Cai et al., "Simultaneous Pre- and Free-assignment Routing for Multiple Redistribution Layers with Irregular Vias," in DAC, 2021.

Experimental Results

• Routing results:



(a) Baseline. (b) The proposed algorithm. Figure 7: The T3 routing solutions of the baseline and the proposed algorithm.





(a) Baseline. (b) The proposed algorithm. Figure 8: The T4 routing solutions of the baseline and the proposed algorithm.



- To the best of our knowledge, this is the first work to solve the routing problem of mask stitching regions of ultra large 2.5D wafer scale packages.
- The proposed algorithm has a conflict elimination scheme to efficiently determine the corresponding layer of each net in the routing process layer by layer.
- Considering the special design rules of mask stitching regions, the proposed algorithm can efficiently generate better routing solutions compared with existing RDL routing algorithms.
- Experimental results show the efficiency and effectiveness of the proposed algorithm compared with the SOTA baseline.

Thanks for Your Attention!