A D-Band CMOS Transceiver Chipset Supporting 640Gb/s Date Rate with 4×4 Line-of-Sight MIMO

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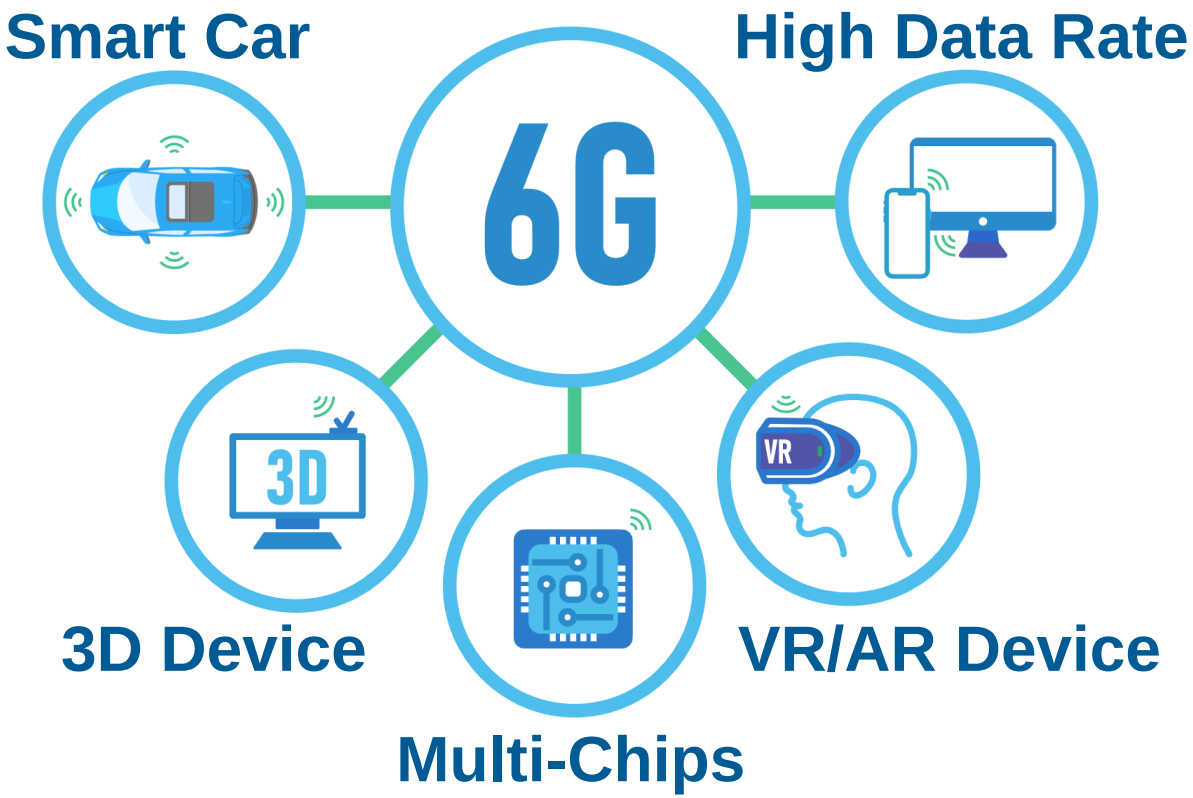
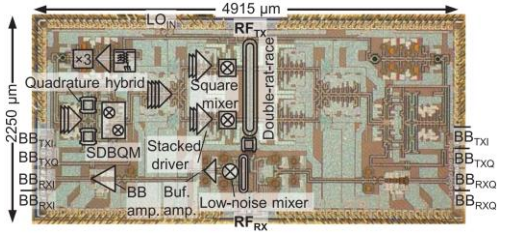
Background and Motivation

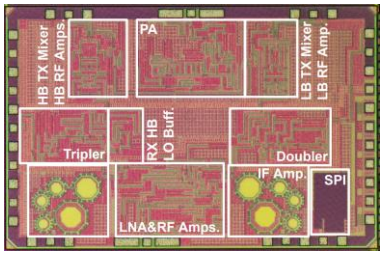


- Frequency Band Over 100GHz
- Data Rate exceeds 100Gb/s
- Ultra-low latency
- Massive Capacity

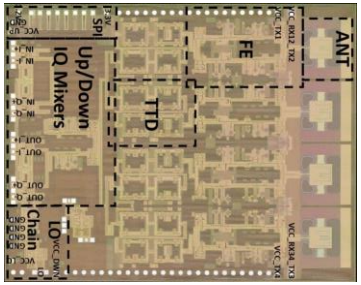
[S. Lee *et al.* JSSC 2019]



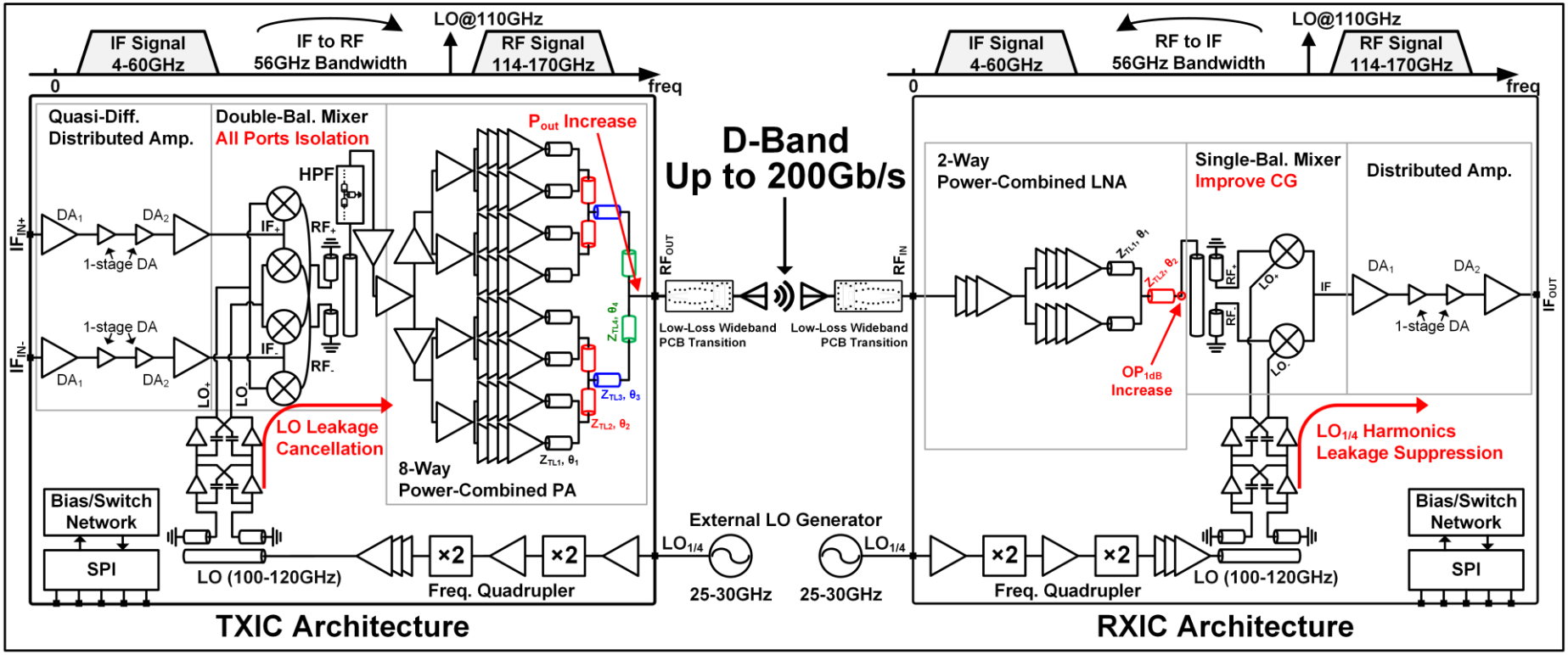
[K. K. Tokgoz *et al.* ISSCC 2018]



[A. Karakuzulu *et al.* JSSC 2023]



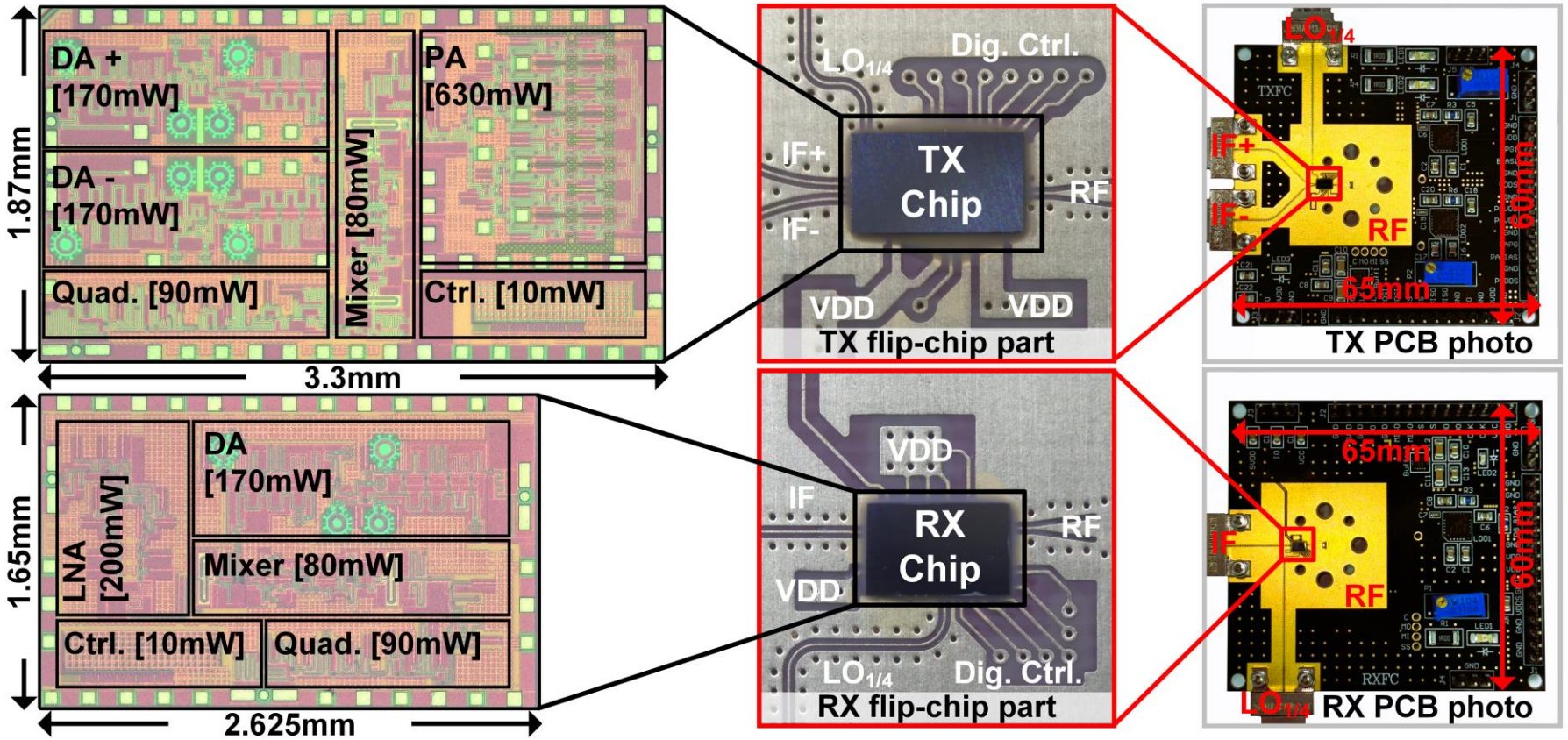
Proposed D-Band CMOS TRX Chipset



Heterodyne Architecture Front-End RF TX/RX Chipset.

External IF / LO signals. Wideband & High-linearity Signal Chain.

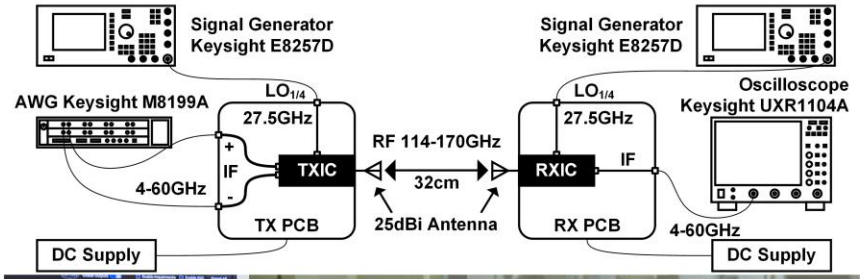
Transceiver Chipset Micrograph and PCB Photo

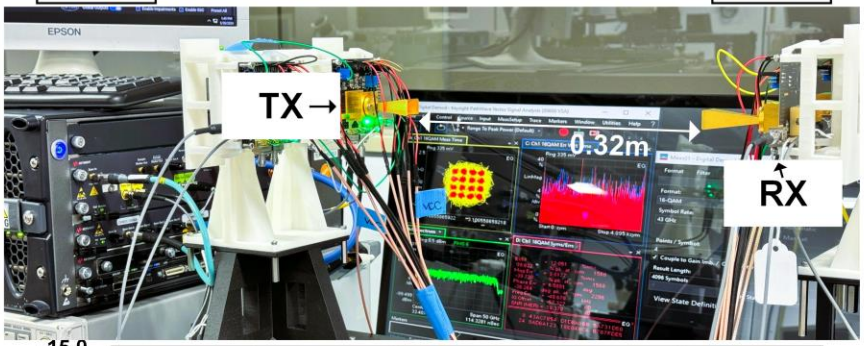


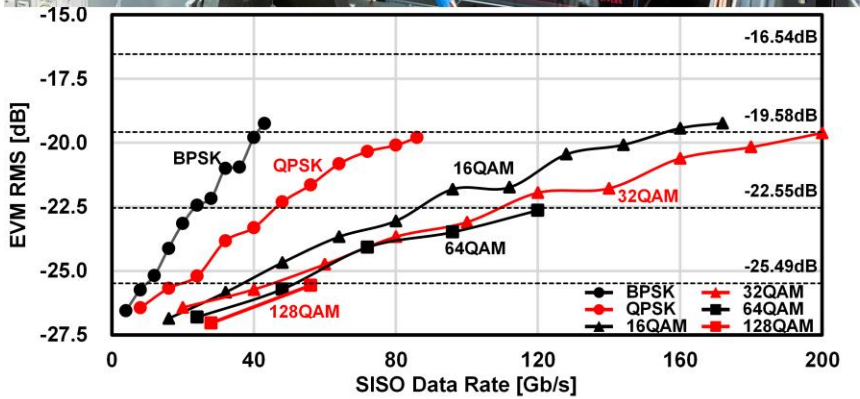
Wideband & Low-Loss PCB IF/LO/RF Interface.

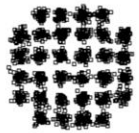
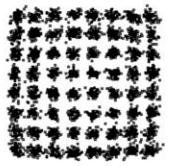
RF port utilizes waveguides to connect horn antenna.

SISO Wireless Measurement

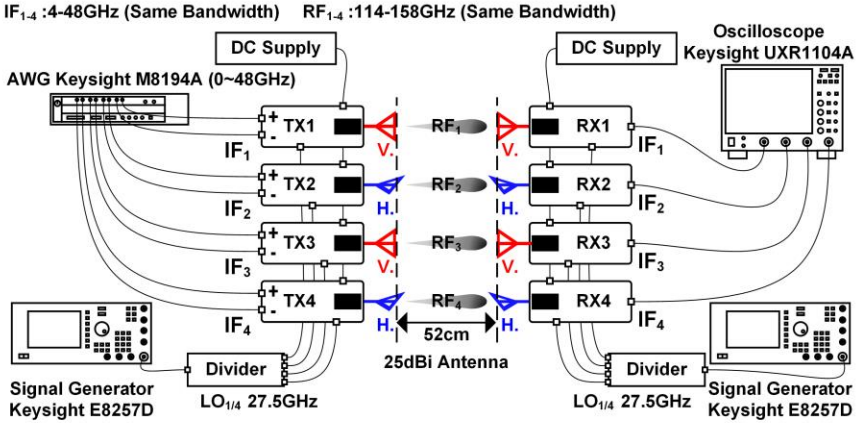


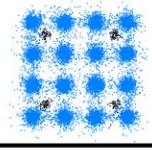
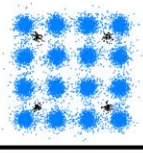
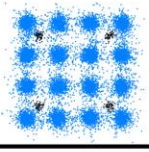
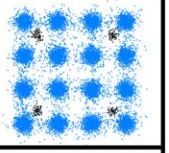


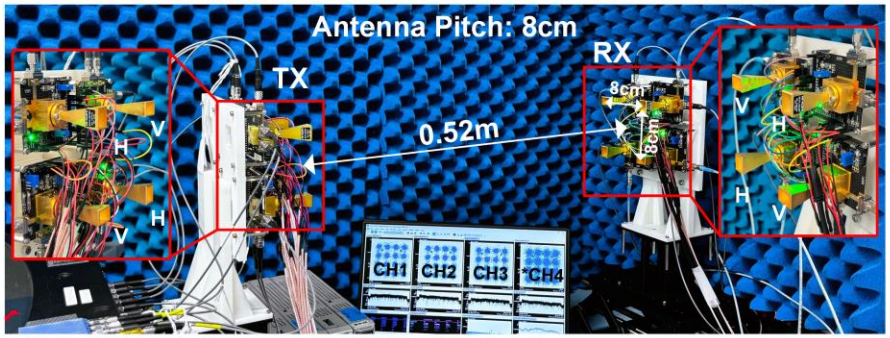


Modulation	BPSK	QPSK	16QAM
Symbol Rate*	43Gbaud	43Gbaud	43Gbaud
Data Rate	43Gb/s	86Gb/s	172Gb/s
EVM_{RMS}	-19.26dB	-19.8dB	-19.23dB
EVM (BER<10^{-3})	EVM < -5.16dB	EVM < -9.80dB	EVM < -16.54dB
Constellation (Equalized) (Single Carrier)			
Modulation	32QAM	64QAM	128QAM
Symbol Rate*	40Gbaud	20Gbaud	8Gbaud
Data Rate	200Gb/s	120Gb/s	56Gb/s
EVM (RMS)	-19.61dB	-22.64dB	-25.57dB
EVM (BER<10^{-3})	EVM < -19.58dB	EVM < -22.55dB	EVM < -25.49dB
Constellation (Equalized) (Single Carrier)			
*roll-off factor: 0.05 (>30Gbaud), 0.1 (<30Gbaud)			

MIMO Wireless Measurement

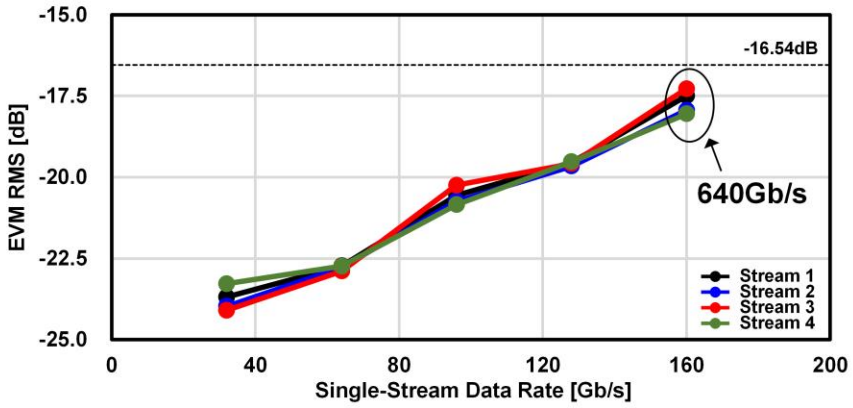


Modulation	16QAM			
Stream*	Stream1 (V)	Stream2 (H)	Stream3 (V)	Stream4 (H)
Bandwidth	40GHz	40GHz	40GHz	40GHz
Data Rate	160Gb/s	160Gb/s	160Gb/s	160Gb/s
EVM (RMS)	-17.50dB	-17.94dB	-17.28dB	-18.05dB
EVM (BER<10^{-3})	EVM < -16.54dB	EVM < -16.54dB	EVM < -16.54dB	EVM < -16.54dB
Constellation (Equalized)				
* OFDM signal with 1024 carriers.				



*UXR's CH4 is weak. It causes worse EVM than other channels.

Channel	CH1	CH2	CH3	CH4
Power Level*	0dBc	-49dBc	-24.8dBc	-46.4dBc
*Signal in channel 1 is turned on.				



Performance Comparison

	ISSCC 2018 [23]	JSSC 2019 [21]	TMTT 2020 [25]	IMS 2020 [47]	JSSC 2020 [24]	JSSC 2023 [27]	ISSCC 2024 [20]	JSSC 2024 [29]	This work			
Technology	65nm CMOS	40nm CMOS	130nm SiGe	130nm SiGe	80nm InP-HEMT	130nm SiGe	28nm CMOS	65nm CMOS	65nm CMOS			
RF Freq. [GHz]	70 - 105	252 - 279	225 - 255	222.5 - 257.5	275 - 305	110 - 170	90 - 180	88 - 136	114 - 170			
TRX Integration	TRX	TRX	TX & RX	TX & RX	Integrated PA	TRX	TX & RX	TRX	TX & RX			
Modulation*	16QAM	16QAM	QPSK	QPSK / 16QAM	16QAM	BPSK / QPSK 16QAM / 32QAM	OOK	16QAM	16QAM	32QAM	64QAM	128QAM
SISO TX-to-RX Data Rate** [Gb/s]	120	80	55	60 / N/A[#]	120	60 / 120 120 / N/A[##]	16 / 20	112	172	200	120	56
SISO EVM_{RMS} [dB]	-17	-18.42	-9.94	-14.52 / -14.61	-16.7	-11.15 / -9.9 -17.2 / -17.6	N/A	-16.6	-19.23	-19.61	-22.64	-25.57
MIMO TX-to-RX Data Rate** [Gb/s]	N/A	N/A	110	N/A	N/A	N/A	N/A	N/A	640	N/A	N/A	N/A
MIMO EVM_{RMS} [dB]	N/A	N/A	-9.94	N/A	N/A	N/A	N/A	N/A	-17.69	N/A	N/A	N/A
TX P_{sat} [dBm]	-1.9	-1.6	7.5	12	11	-8	15-18	0	12 - 15			
RX SSB NF [dB]	N/A	22.9	17	18.5	10 - 17[+]	10.08[▲]	6.2 - 8.5[▲]	15	12			
TX/RX P_{DC} [mW]	120/160	890/897	2850 (TRX)	1237 / 850	4500 / 4500	2500 / 1950	750 / 160	200 / 120	1150 / 550 (1V) 1468 / 700 (1.2V)			
Antenna Gain [dBi]	23	24	25	21	50	4.8	15	15	25		43	
Communication Distance [m]	0.2	0.03	1 / 2	0.8	9.8	0.15	1 / 0.5	0.02	0.32 / 0.52		15 / 90	
RF Interface	Flip-Chip Implementation	Probing	On-Chip Antenna (Lens)	On-Chip Antenna (Lens)	Individual module	On-Chip Antenna (Lens)	Wire Bonding	Flip-Chip Implementation	Wideband Flip-Chip Implementation & PCB-to-Waveguide Transition			
TX/RX Area [mm^2]	6 (TRX)	11.06 (TRX)	4.02/3.36	7 / 5.1	N/A	27.2 (TRX)	0.69 / 0.77	5.7 (TRX)	6.17 / 4.33			

*This work can also support BPSK & QPSK.
**Data rate for BER < 10^{-3}.
[#]Data rate of 100Gb/s is also reported with BER > 10^{-3}.
[##]Data rate of 200Gb/s is also reported with BER > 10^{-3}.
[+]NF of the RF PA.
[▲]Simulation result.

Thank You

Reference

- [1] S. Lee et al., "An 80-Gb/s 300-GHz-Band Single-Chip CMOS Transceiver," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3577-3588, Dec. 2019.
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