

A High-Density Hybrid Buck Converter with a Charge Converging Phase Reducing Inductor Current for 12V Power Supply Systems

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AUTOMATION
CONFERENCE

Motivation



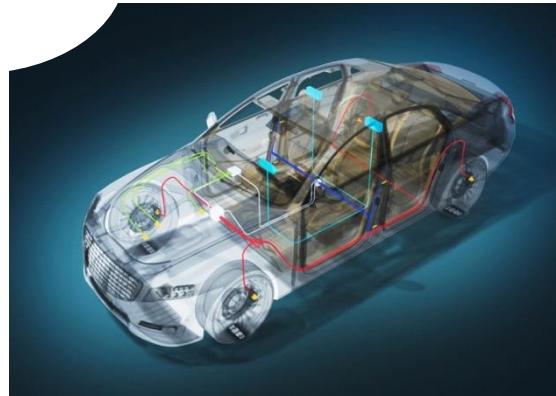
Data Center



Portable Devices



Industrial Automation

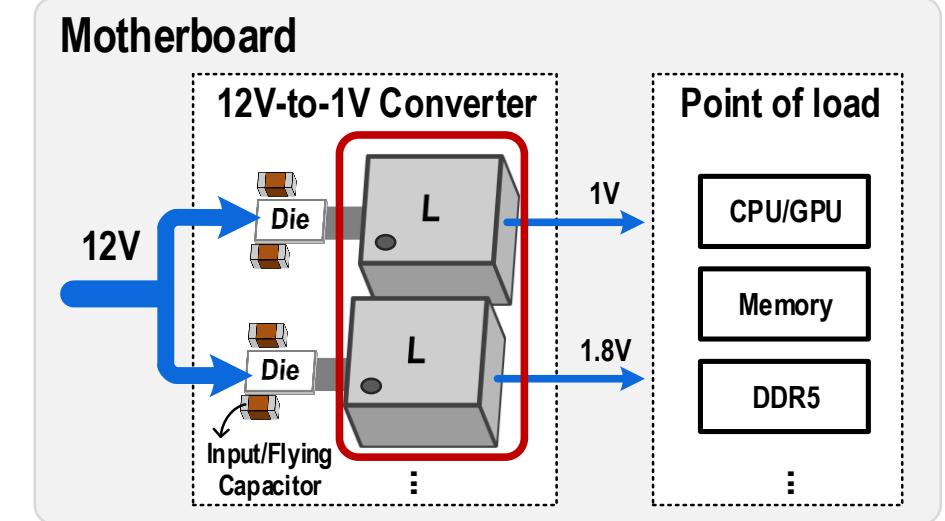


Automotive Electronics
[Images from Internet]

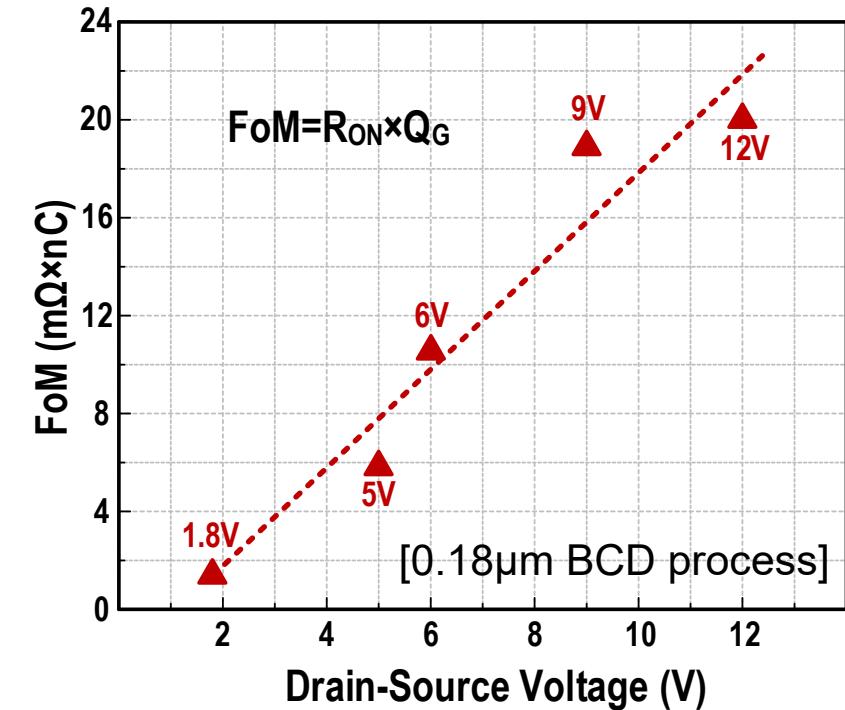
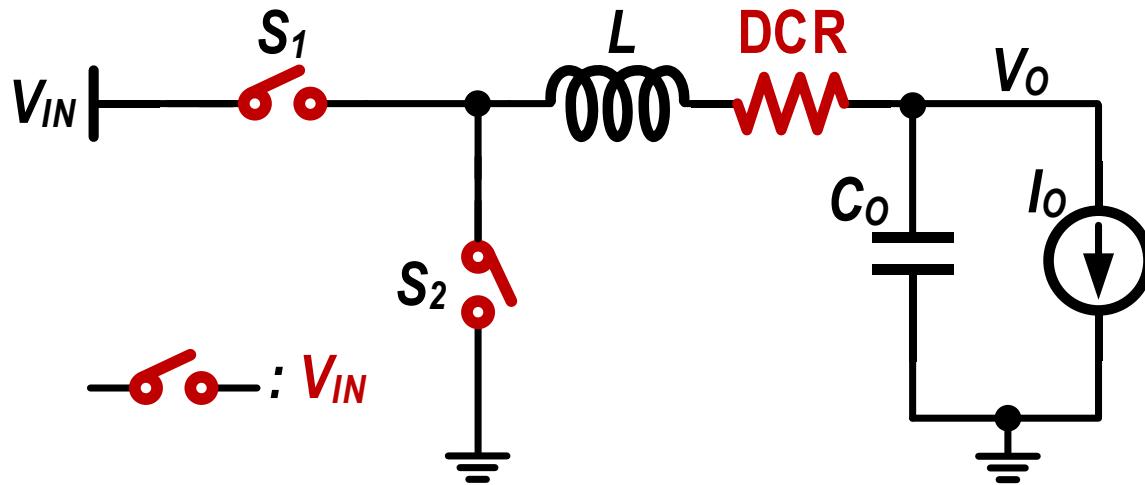
- 12V system is widely used in industrial and automotive applications
- Inductors occupy the most area, leading to **low current density**

□ Requirements:

- High voltage conversion ratio
- High efficiency
- High current density



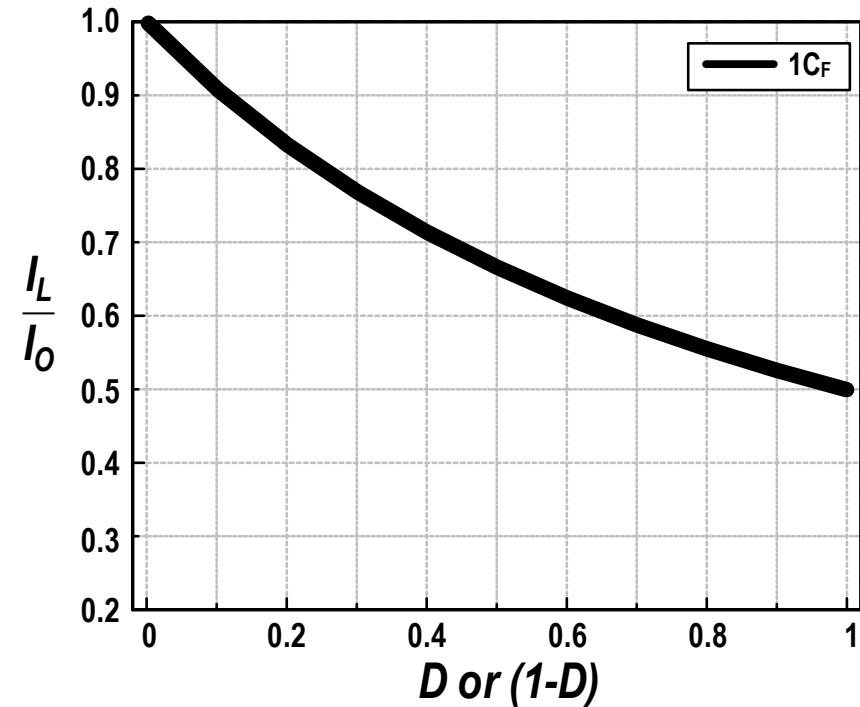
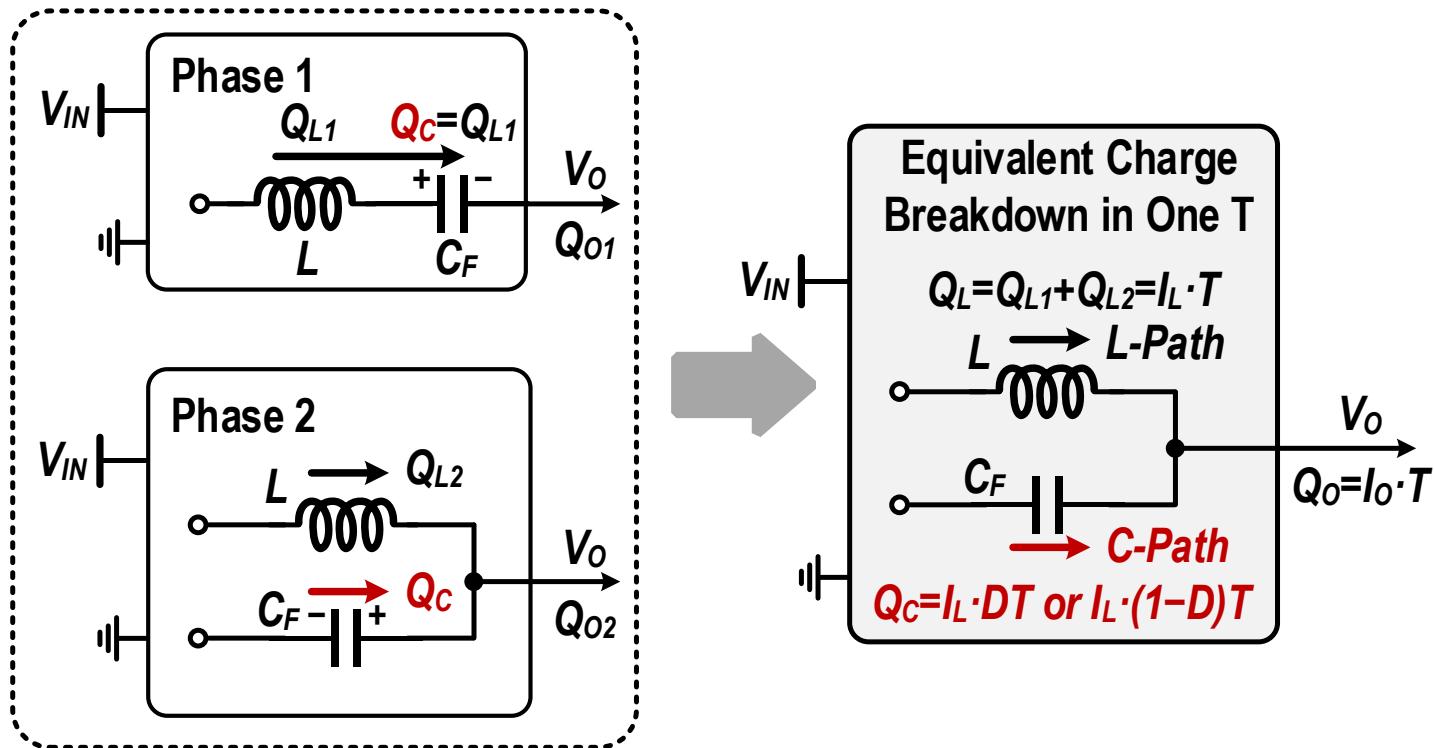
Conventional Buck Converter



- ✗ High-voltage device (high FoM) and high power loss
- ✗ High inductor current and large DCR conduction loss

Dual-Path Buck Converters

- Phase 1: C_F along with V_O is soft charged by L with a Q_C of $I_L DT$ or $I_L(1-D)T$
- Phase 2: Q_C is transferred to the output in parallel with L **realizing I_L reduction**

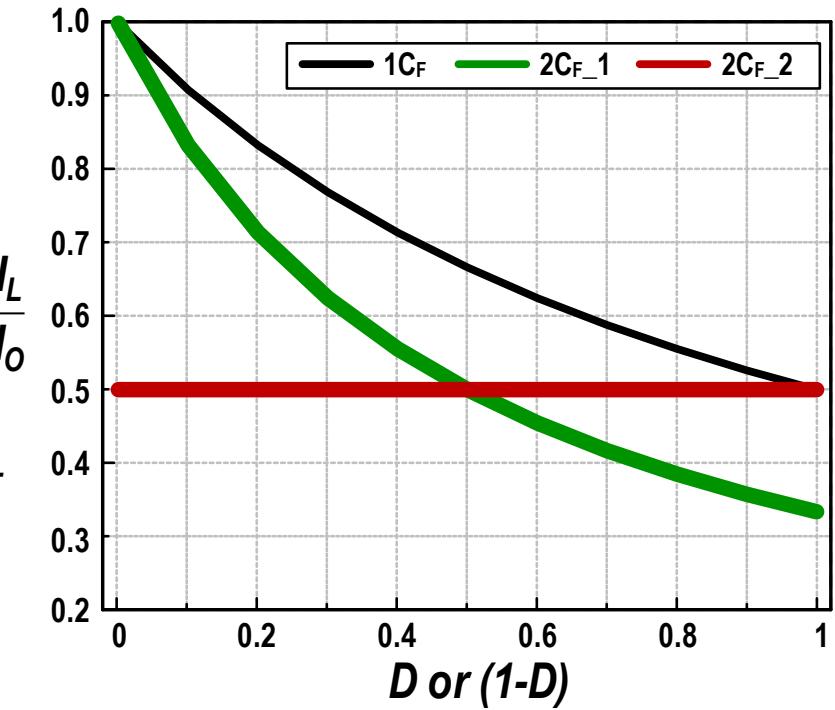
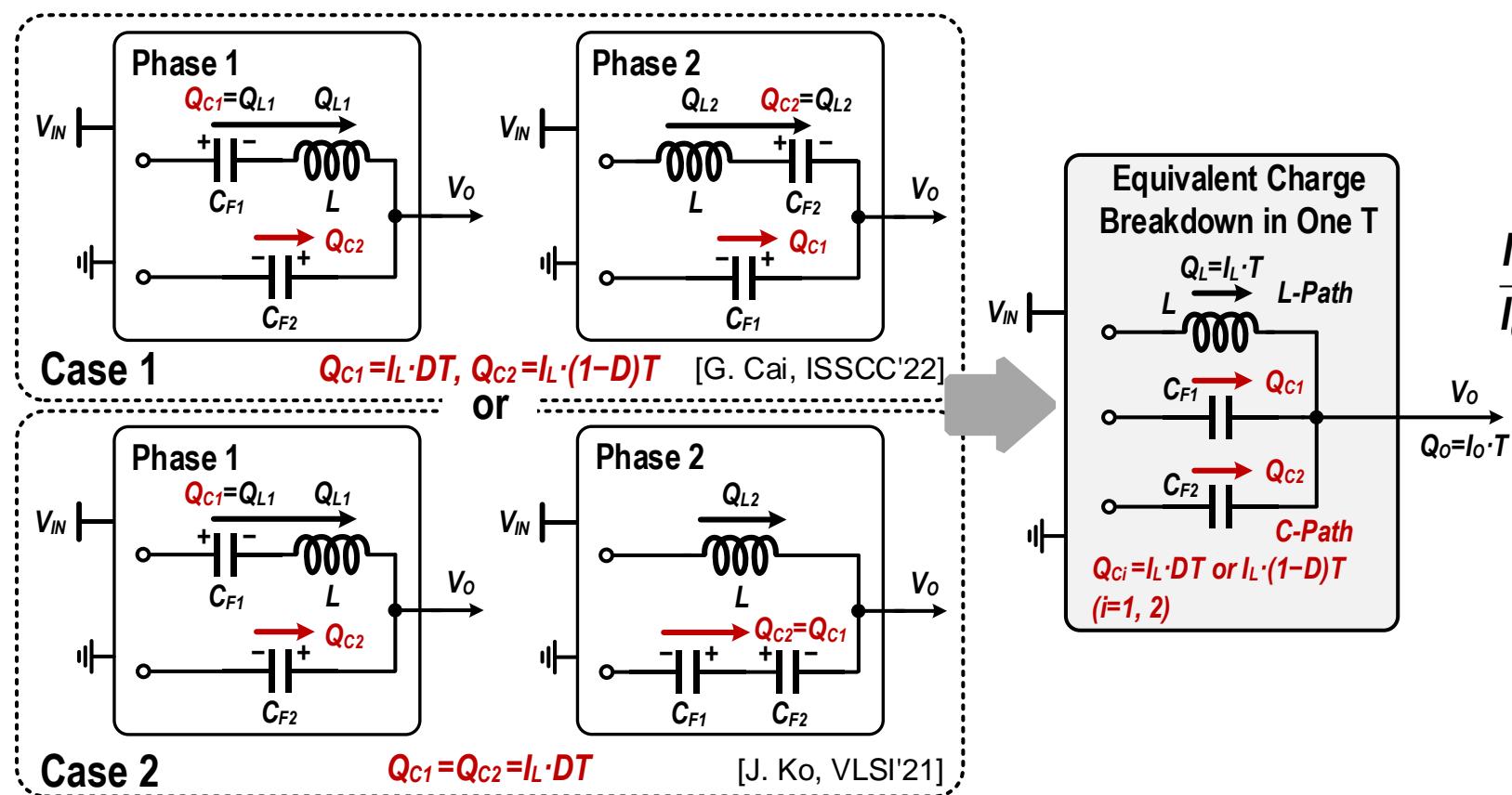


➤ Q_C dependent on D and modest I_L reduction

$$\frac{I_L}{I_0} = \frac{Q_L}{Q_O} = \frac{Q_L}{Q_L + Q_C} = \frac{1}{1+D} \text{ or } \frac{1}{2-D}$$

Dual-Path Buck Converters

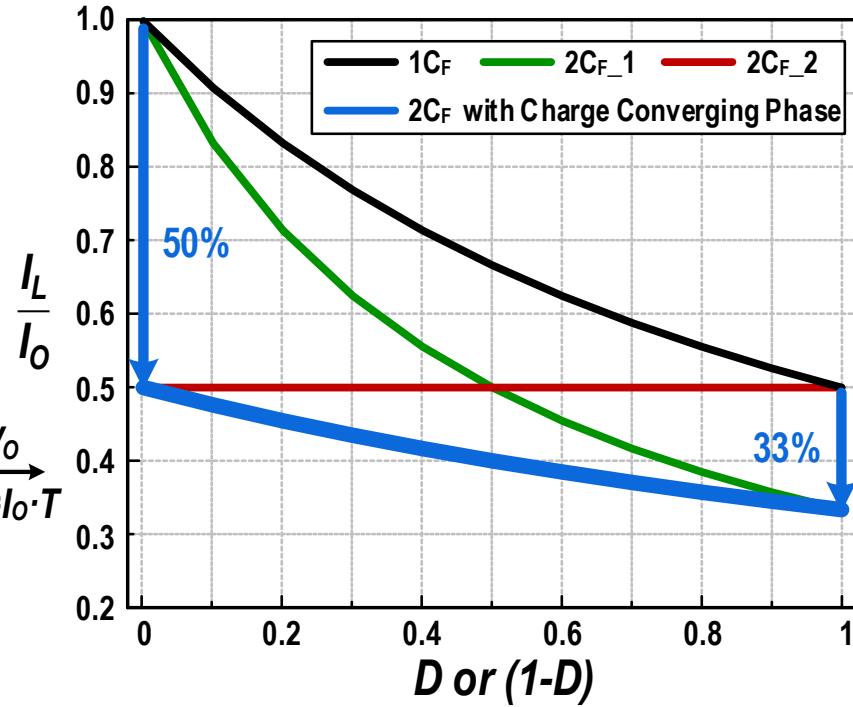
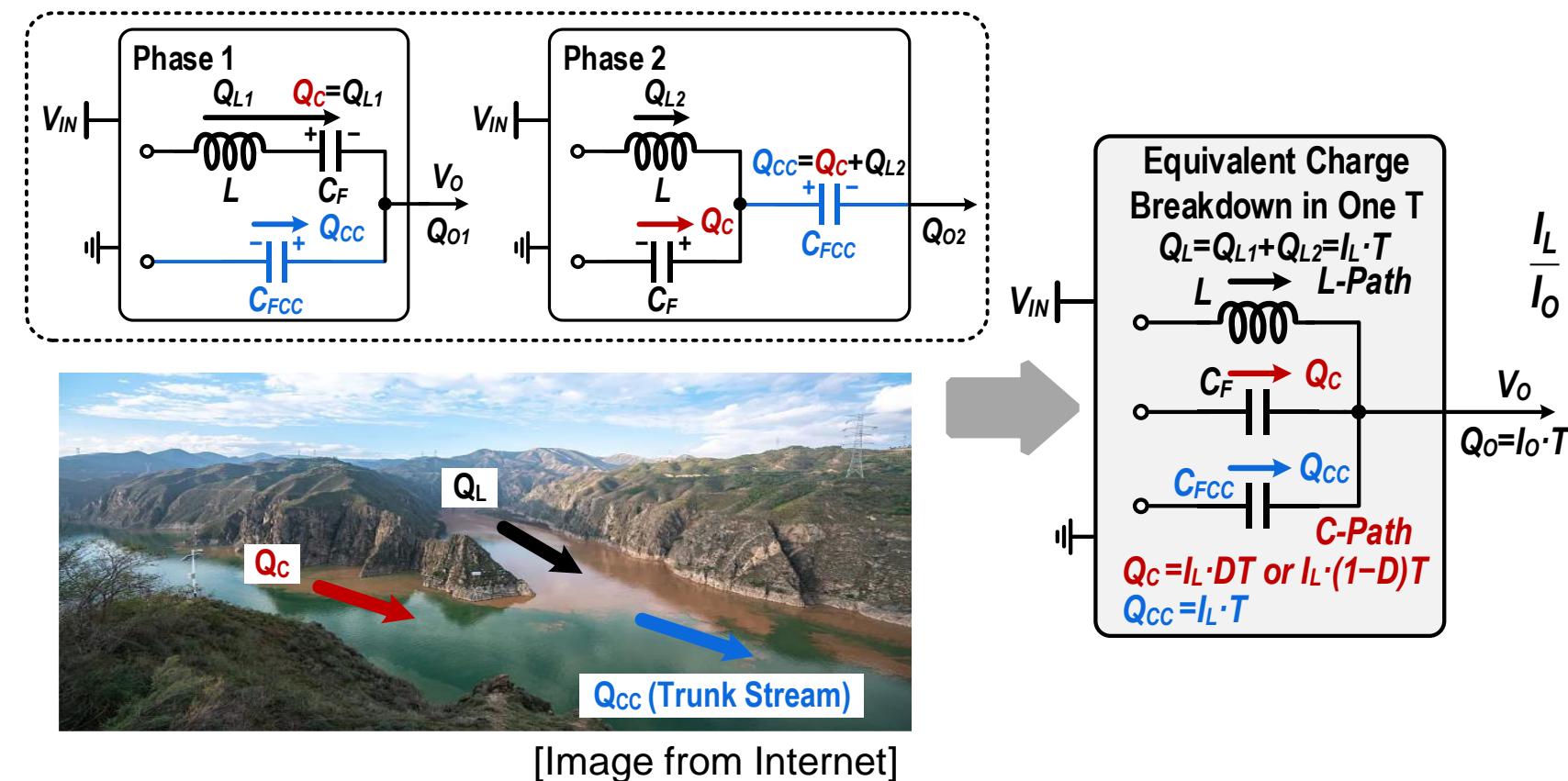
- By applying 2 C_F s, I_L is further reduced. Each Q_C is dependent on D and still limited to $I_L \cdot DT$ or $I_L \cdot (1-D)T$



$$\frac{I_L}{I_0} = \frac{Q_L}{Q_L + Q_{C1} + Q_{C2}} = \frac{1}{1+2D} \text{ or } \frac{1}{3-2D} \text{ or } \frac{1}{2}$$

Proposed Charge Converging Phase

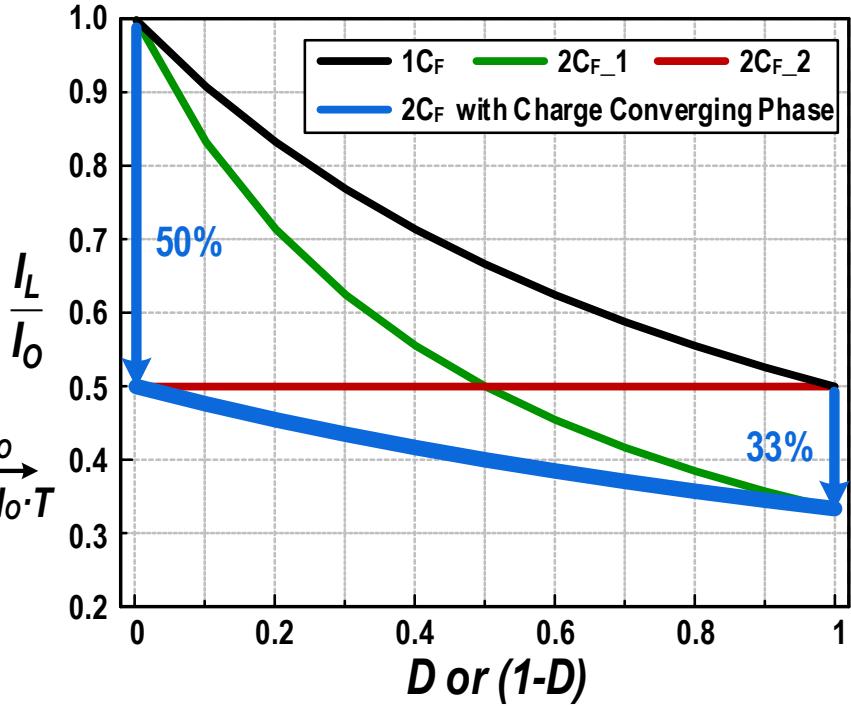
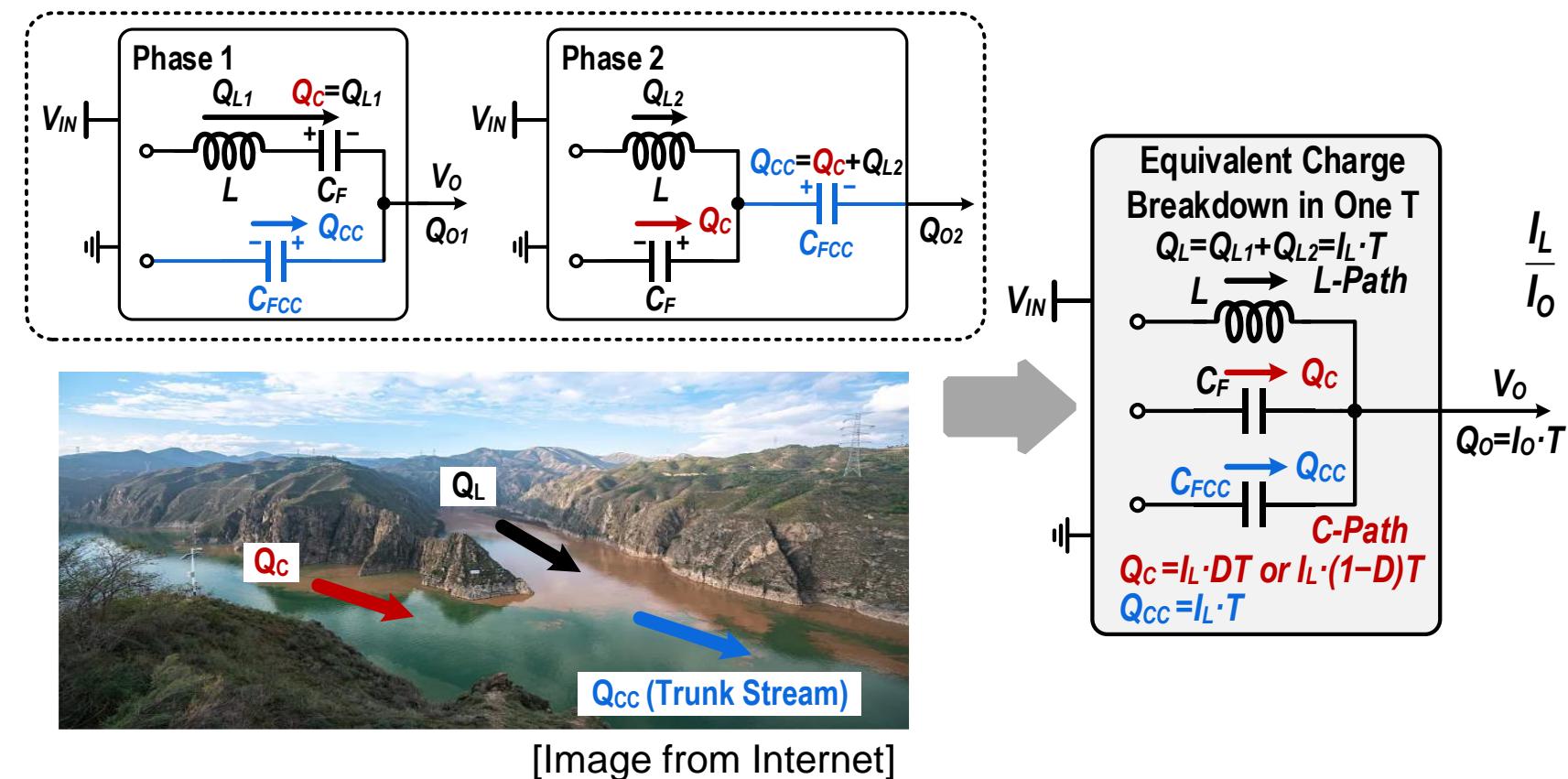
- Phase 1: C_F and V_O are charged by L while Q_{CC} gets transferred to V_O
- Phase 2: By reusing Q_C , C_{FCC} and V_O are charged simultaneously by L and C_F



$$\frac{I_L}{I_0} = \frac{Q_L}{Q_L + Q_C + Q_{CC}} = \frac{1}{2+D} \text{ or } \frac{1}{3-D}$$

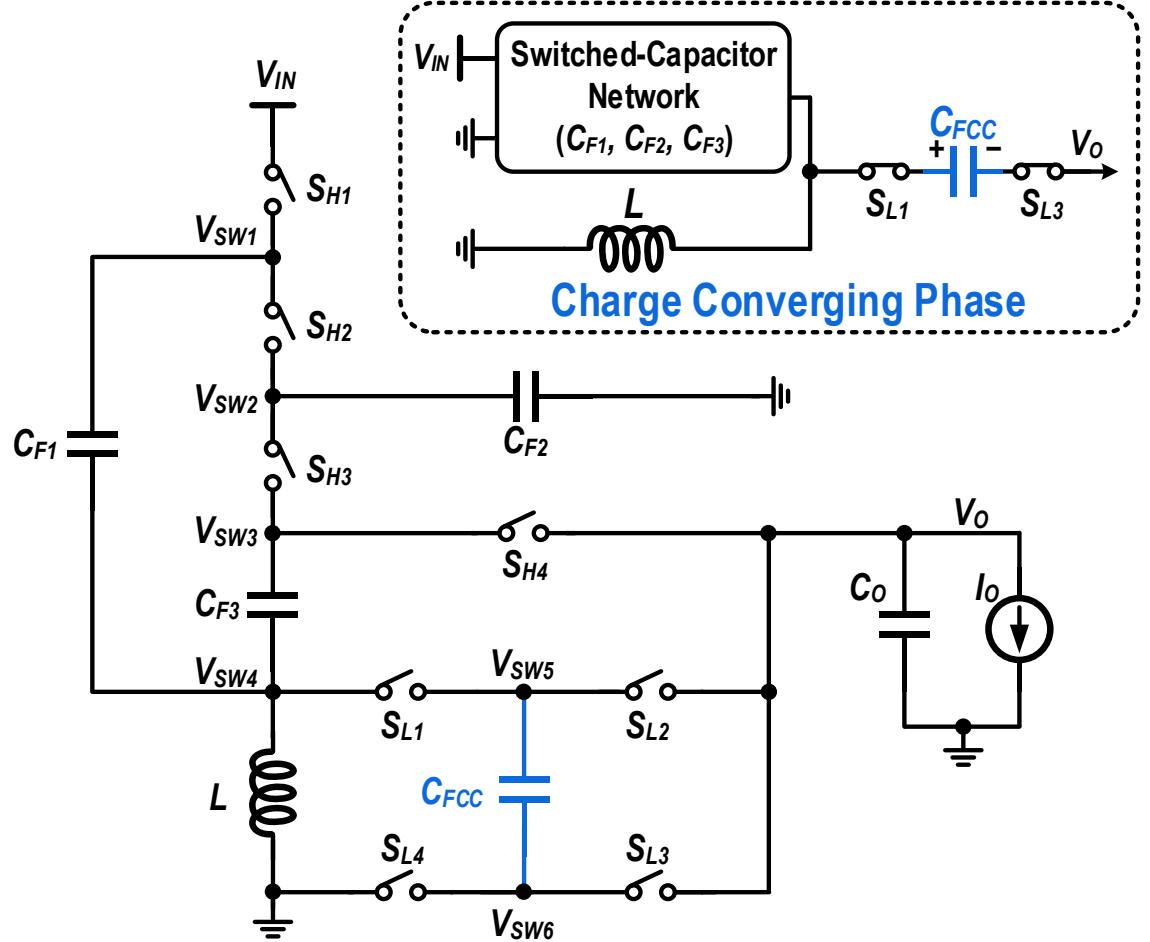
Proposed Charge Converging Phase

- The charge from C_{FCC} (Q_{CC}) is increased to $I_L T$ and **is independent on D**
- **I_L is reduced to always $< 0.5 \times I_O$ across D range**



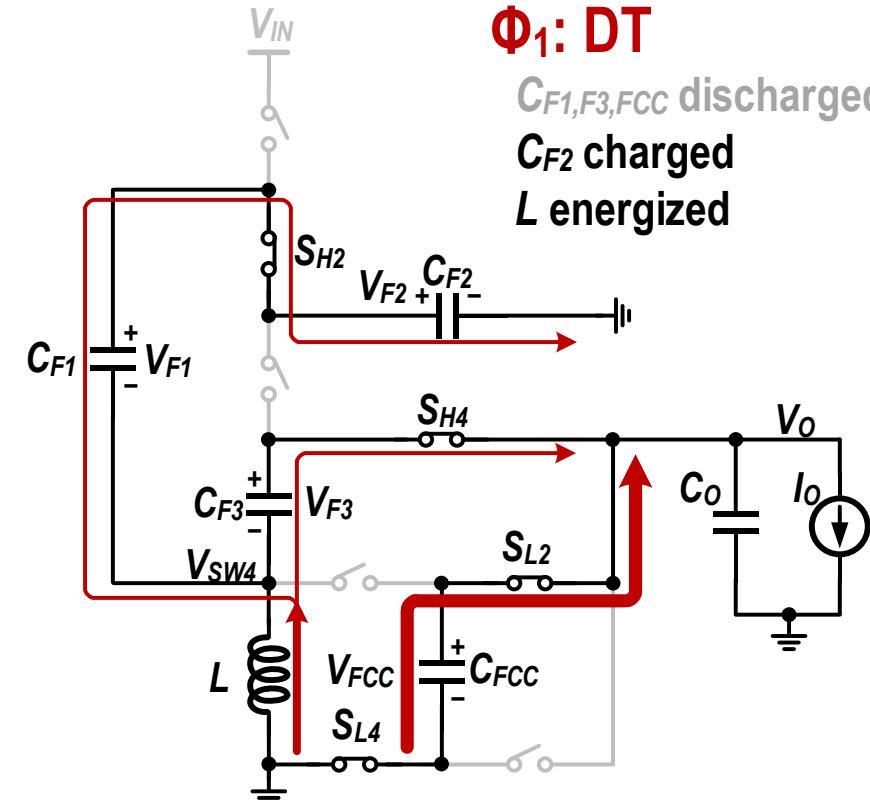
$$\frac{I_L}{I_O} = \frac{Q_L}{Q_L + Q_C + Q_{CC}} = \frac{1}{2+D} \text{ or } \frac{1}{3-D}$$

Proposed Hybrid Buck Converter



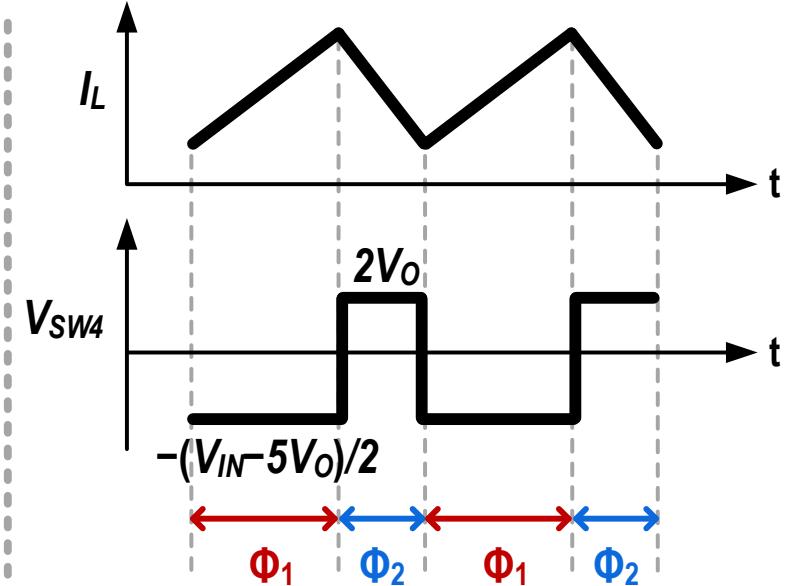
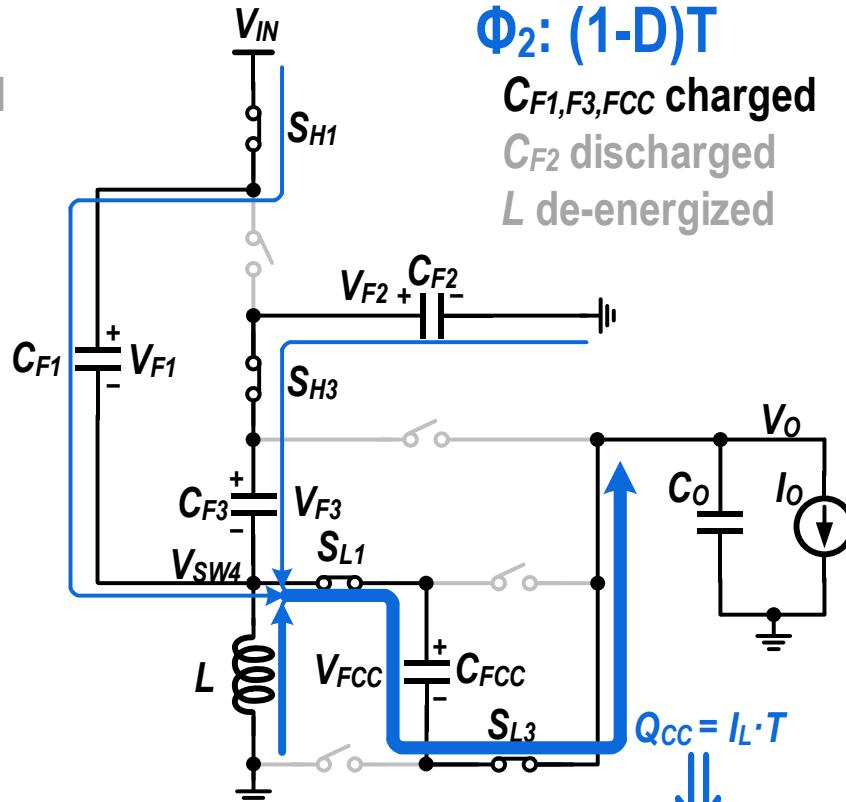
- 1 inductor, 4 flying capacitors & 8 switches
 - C_{F1} , C_{F2} and C_{F3} are stacked
 - Reducing voltage stress of switches
 - All switches implemented by 5V/1.8V devices
 - L , C_{F3} , C_{FCC} form charge converging phase
 - Average inductor current always $< 0.5I_O$
 - Reducing DCR Conduction Loss
 - Relieving reliance on a bulky inductor
- ➡ ☺ **Higher efficiency**
- ☺ **Higher current density**

Working Principle



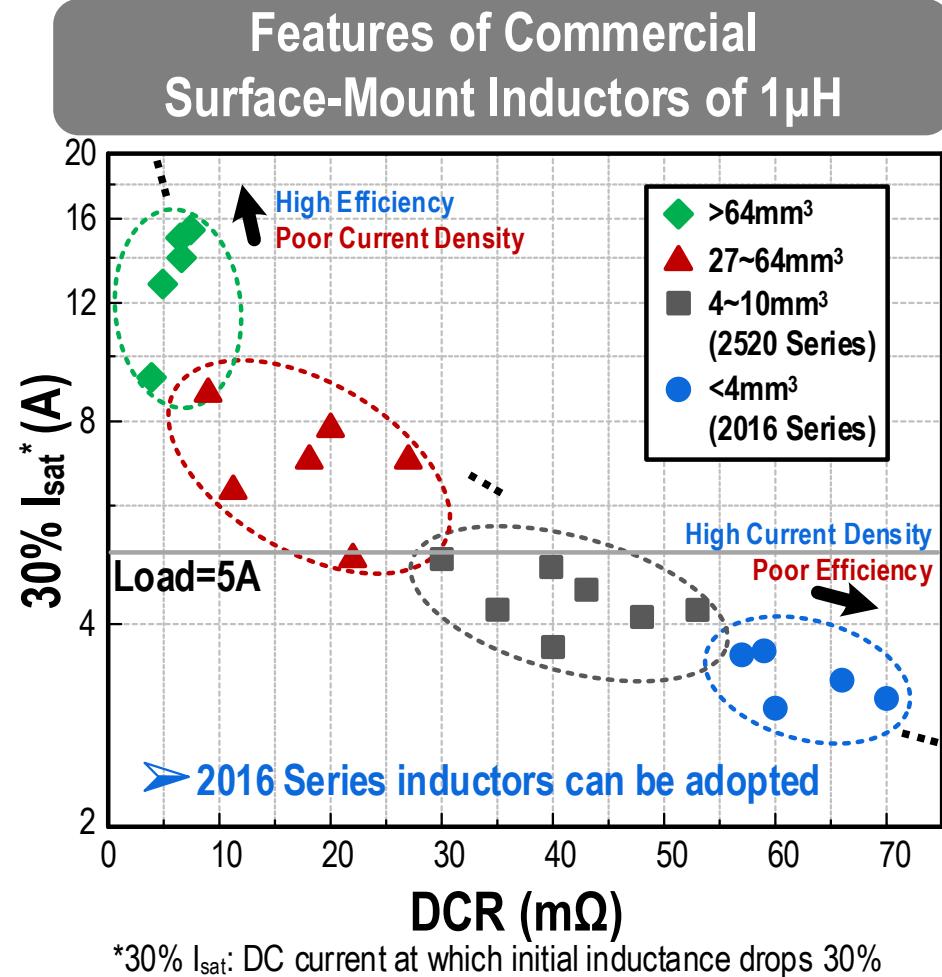
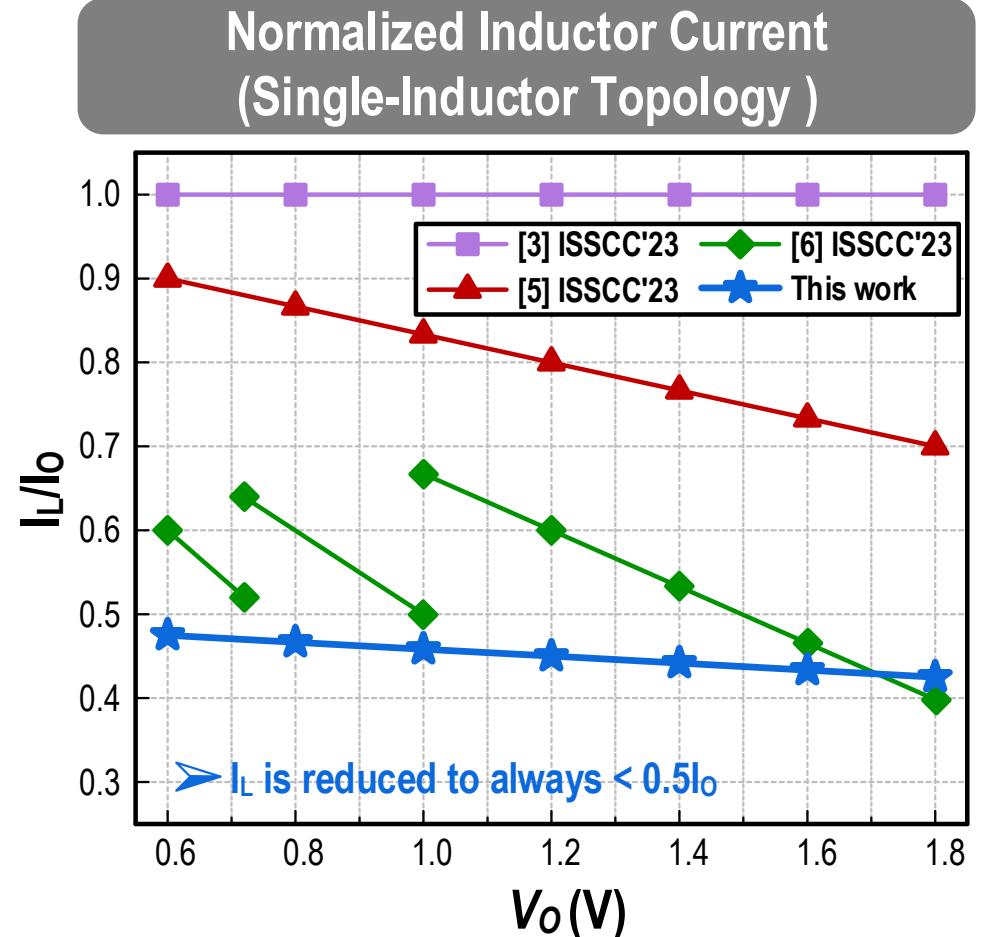
$$\frac{V_O}{V_{IN}} = \frac{D}{4+D}$$

$$\frac{I_L}{I_O} = \frac{2}{4+D}$$



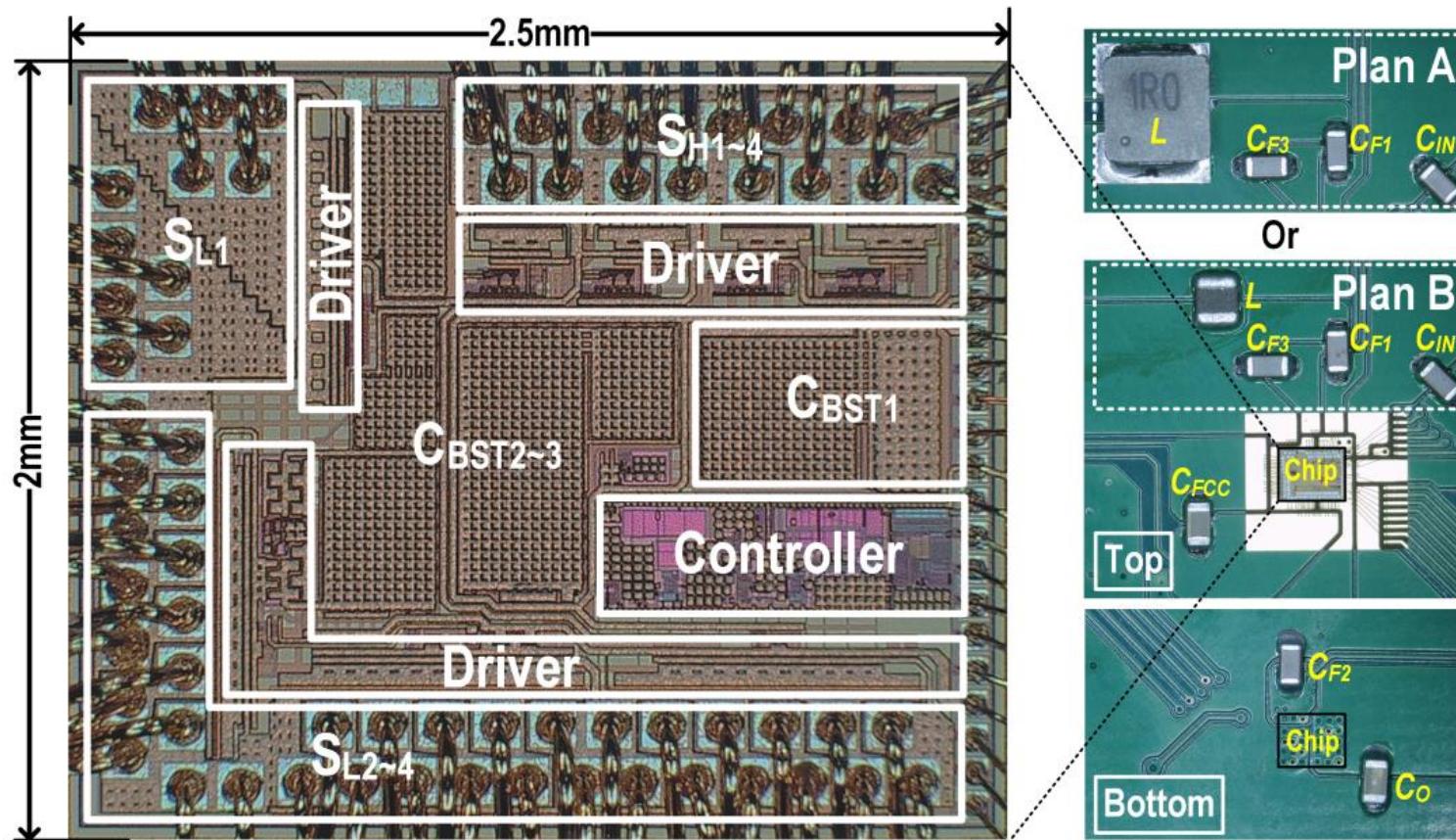
V_{F1}	V_{F2}	V_{F3}	V_{FCC}
$V_{IN}-2V_O$	$\frac{V_{IN}+V_O}{2}$	$\frac{V_{IN}-3V_O}{2}$	V_O

Topology Comparison



- The average inductor current is **consistently reduced to $< 0.5I_O$**
- For 5A load capacity, **2016-series inductors** ($30\% I_{sat} \sim 3\text{A}$) can be adopted

Chip Micrograph and PCB Photo



- 0.18 μ m BCD process
- Chip area: 2.5mm \times 2mm
- F_{SW} : 1MHz
- V_{IN} : 12V
- V_O : 1V-1.8V
- Two testing plans
(Bulky & compact inductors)

Selection of Capacitors

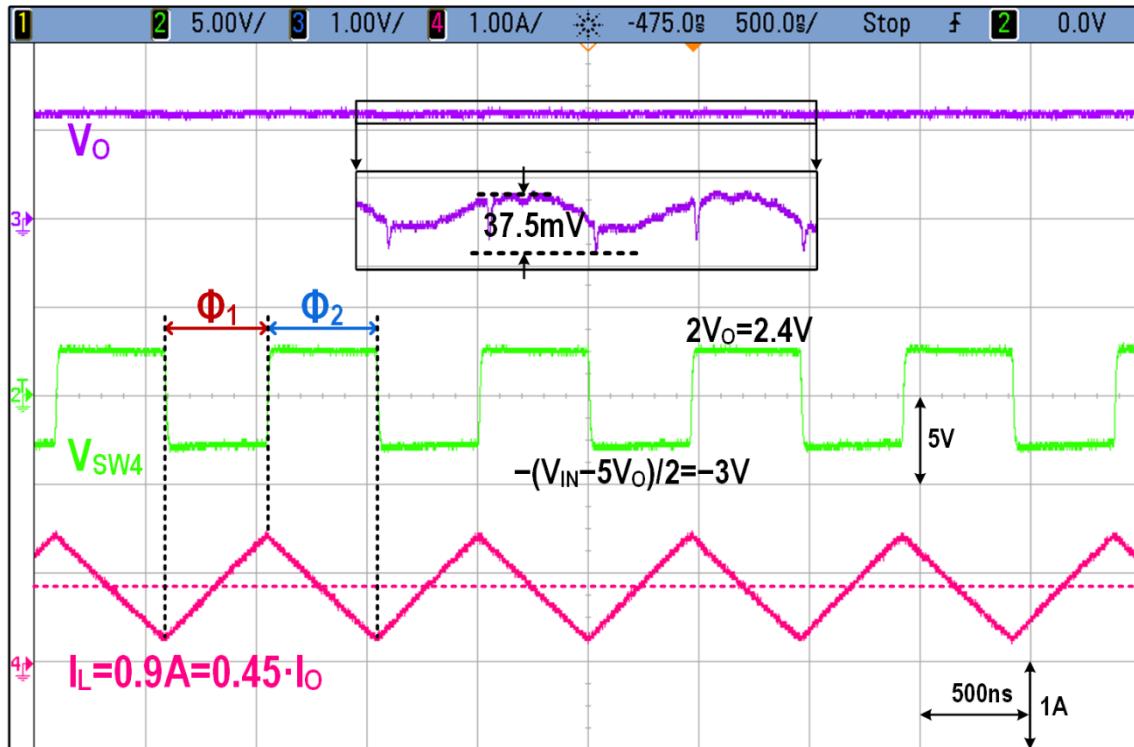
Component	Nominal Value	Footprint (Size)
$C_{IN}, C_{F1}, C_{F2}, C_{F3}$	10 μ F	0603
C_{FCC}, C_O	22 μ F	(1.6 \times 0.8 \times 0.8mm 3)

Selection of Inductors

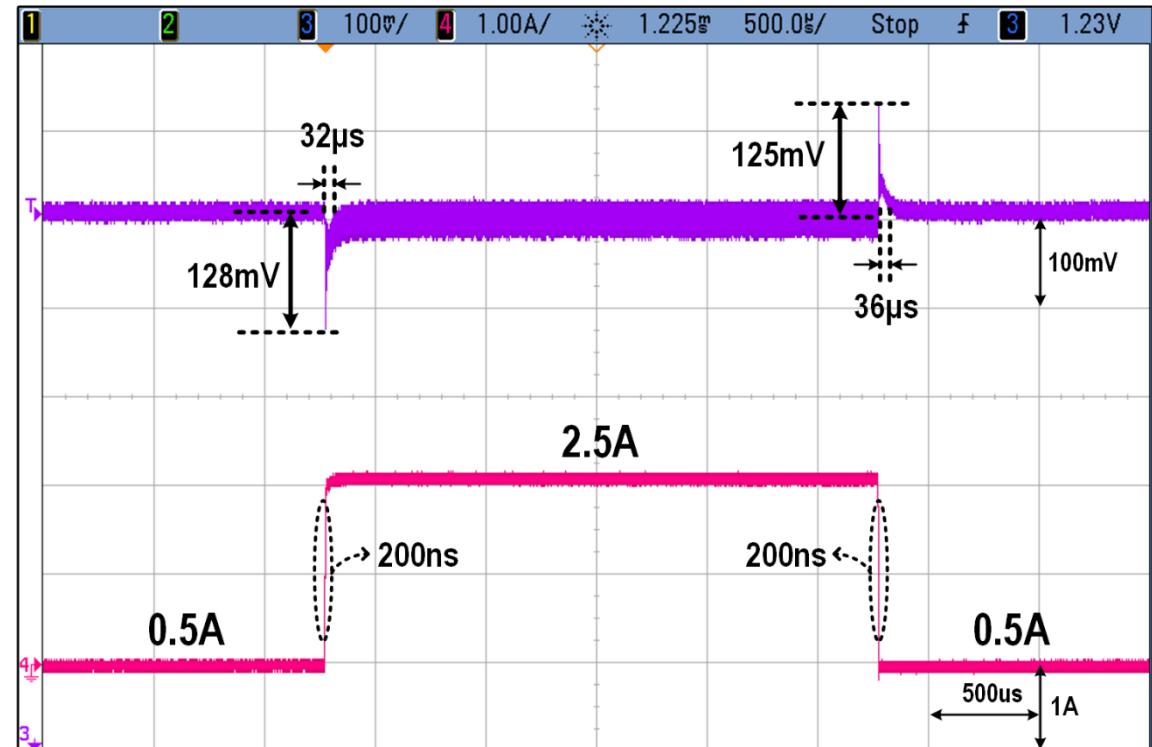
Component	Inductance (DCR)	I _{sat} (30%)	Size
L (<i>Plan A</i>)	1 μ H (10.5m Ω)	6.7A	4.2 \times 4 \times 2.1mm 3
L (<i>Plan B</i>)	1 μ H (57m Ω)	3.6A	2 \times 1.6 \times 1mm 3

Measurement Results

Steady State: $V_O=1.2V$, $I_O=2A$

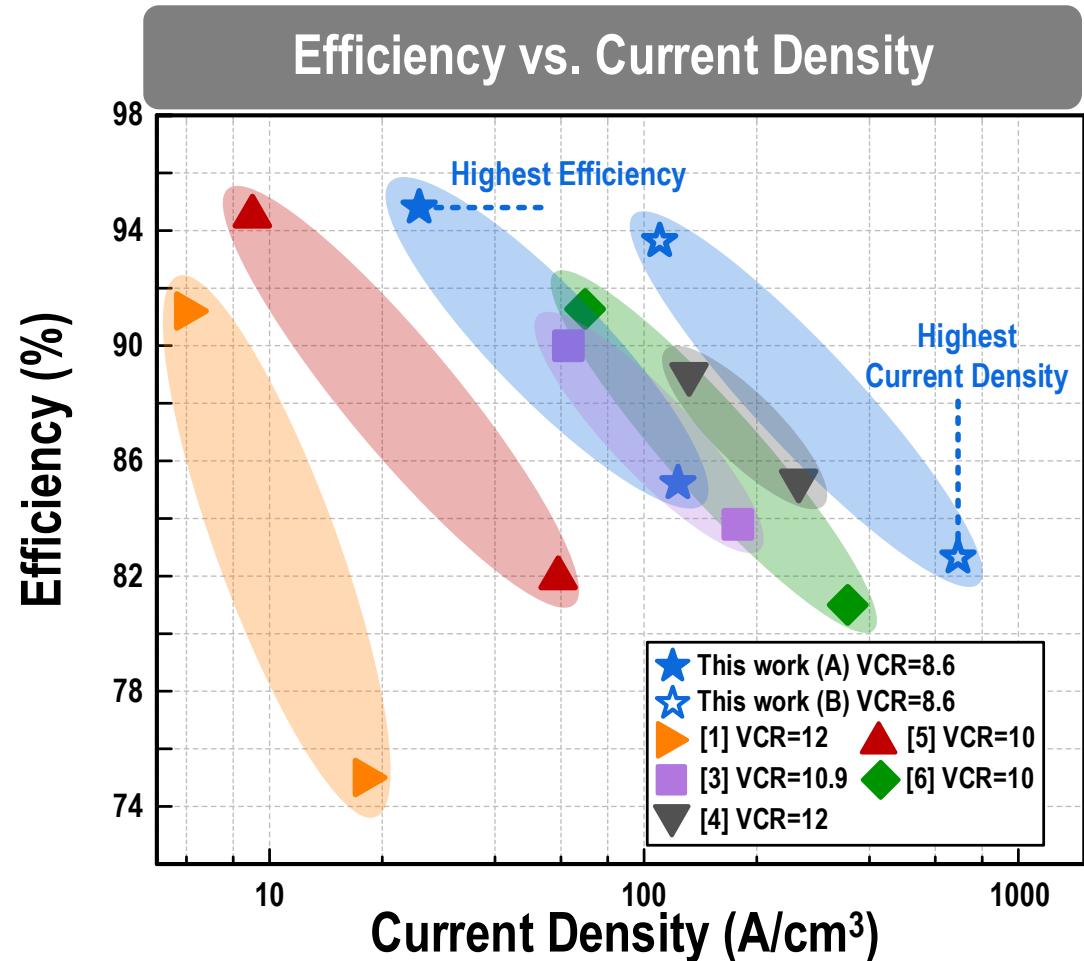
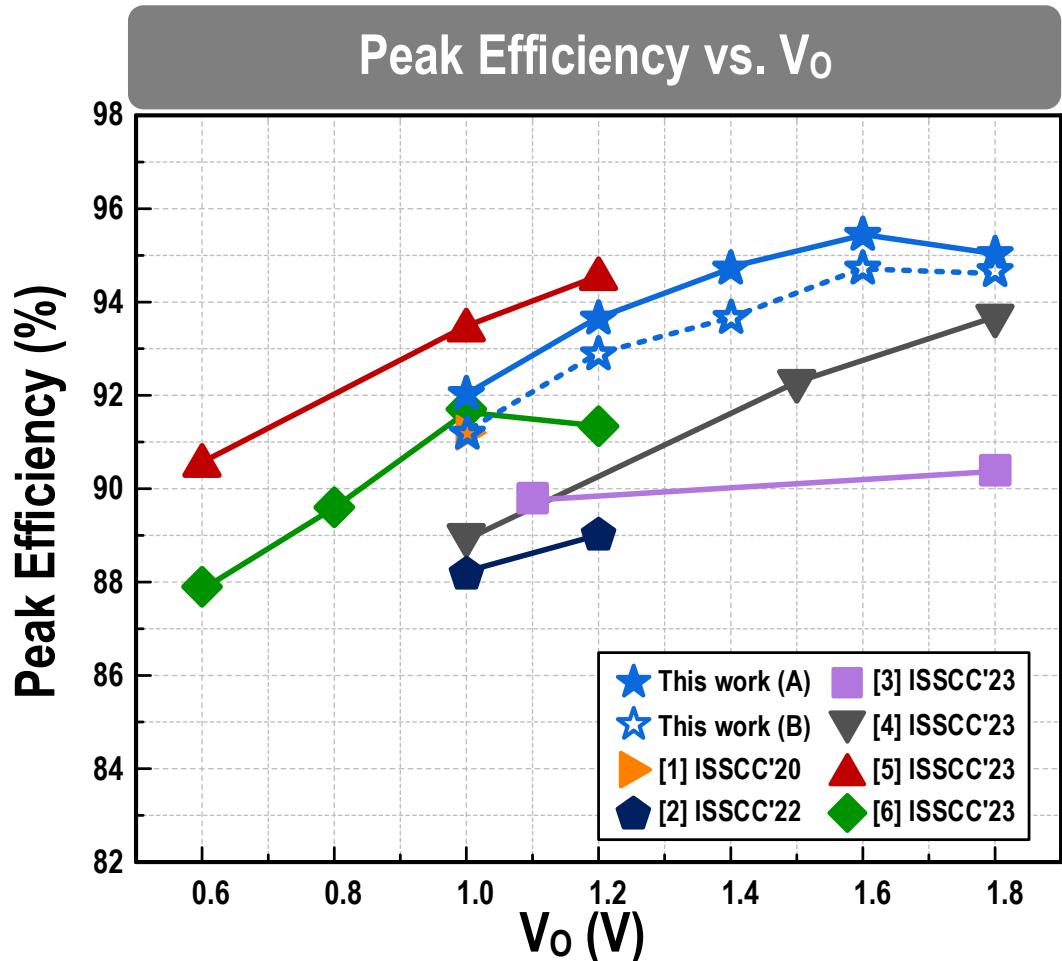


Load Transient: $V_O=1.2V$, $I_O=0.5A-2.5A-0.5A$



- Steady state: the average I_L showing **a reduction of 55%**
- Load transient (2A/200ns): verifying the stability of the converter

Measurement Results



- High peak efficiency across a wide V_O range
- **Highest efficiency or highest current density** with an appropriate inductor

Summary and Comparison

	Bulky Inductor Adopted					Compact Inductor Adopted		
Publication	ISSCC 2020[1]	ISSCC 2022[2]	ISSCC 2023[3]	ISSCC2023[5]	This work (A)	ISSCC 2023[4]	ISSCC 2023[6]	This work (B)
Technology	0.18µm BCD	0.18µm BCD	0.18µm BCD	0.18µm BCD	0.18µm BCD	0.18µm BCD	0.18µm BCD	0.18µm BCD
Topology	Tri-State DSD	DSD	SC Buck	DPSC	CCP-HB	2L4PHB	ReSC-PL	CCP-HB
Nominal $V_{IN} - V_O$	12V/24V – 1V	12V/24V – 1V	12V – 1.1V	9-16V – 0.6-1.6V	12V – 1-1.8V	12V – 1-1.8V	12V – 0.6-1.2V	12V – 1-1.8V
Max. Load Current	3A	4A	4A	5A	5A	4A	5A	5A
Components ^(a)	2L 2C 7S	2L 1C 4S	1L 4C 6S	1L 4C 8S	1L 4C 8S	2L 3C 8S	1L 4C 12S	1L 4C 8S
Inductor	$2 \times 0.56\mu H$	$2 \times 1.8\mu H$	$0.22\mu H$	$0.68\mu H$	$1\mu H$	$2 \times 1\mu H$	$1\mu H$	$1\mu H$
I_L Reduction ^(b) @ VCR=10	0%	0%	0%	20%	55%	20%	40%	55%
Inductor Size (DCR)	$6.6 \times 6.4 \times N.A.^{(c)}$ mm ³ (N.A.)	N.A.	$3.2 \times 2.5 \times 1.2$ mm ³ (6mΩ)	$6.6 \times 6.4 \times N.A.^{(c)}$ mm ³ (N.A.)	$4.2 \times 4 \times 2.1\text{mm}^3$ (10.5mΩ)	$2.5 \times 2 \times 1\text{mm}^3$ (48mΩ)	$2.5 \times 2 \times 1.2\text{mm}^3$ (N.A.)	$2 \times 1.6 \times 1\text{mm}^3$ (57mΩ)
Peak Efficiency @ V_O ($V_{IN}=12V$)	91.2%@1V	89%@1.2V ^(c)	90%@1.1V	94.5%@1.2V	95.4%@1.6V 93.7%@1.2V	93.7%@1.8V 89%@1V	91.8%@1V 91.3%@1.2V ^(c)	94.7%@1.6V 92.9%@1.2V
Efficiency @ I_{O_max}	75%@1V,3A ^(c)	87%@1.2V,4A ^(c)	83.8%@1.1V,4A	82%@1.2V,5A	84.8%@1.2V,5A	85.3%@1V,4A	81%@1.2V,5A ^(c)	82.1%@1.2V,5A
Total Passive Volume ^(d)	168.96mm ³ ^(e)	N.A.	22.1mm ³	84.48mm ³ ^(e)	39.38mm ³	15.17mm ³	14.3mm ³	7.3mm ³
Current Density	18A/cm ³	N.A.	181A/cm ³	59A/cm ³	127A/cm ³	264A/cm ³	350A/cm ³	685A/cm ³

(a) Number of inductors (L), flying capacitors (C), switches (S) adopted in the topology. (b) I_L Reduction = $(I_O/N - I_O)/(I_O/N)$, where N is the number of inductors.

(c) Estimated from graph. (d) Counts flying capacitors and inductors. (e) Counts inductors only, and the height is assumed to be 2mm.

Thank you!