

A 500-MS/s 8-bit SAR ADC Generated from an Automated Layout Generation Framework in 14-nm FinFET Technology



ASP-DAC 2025

University Design Contest



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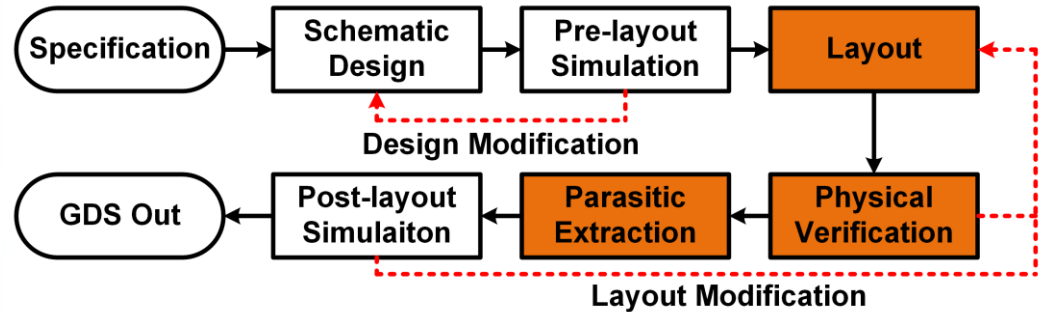
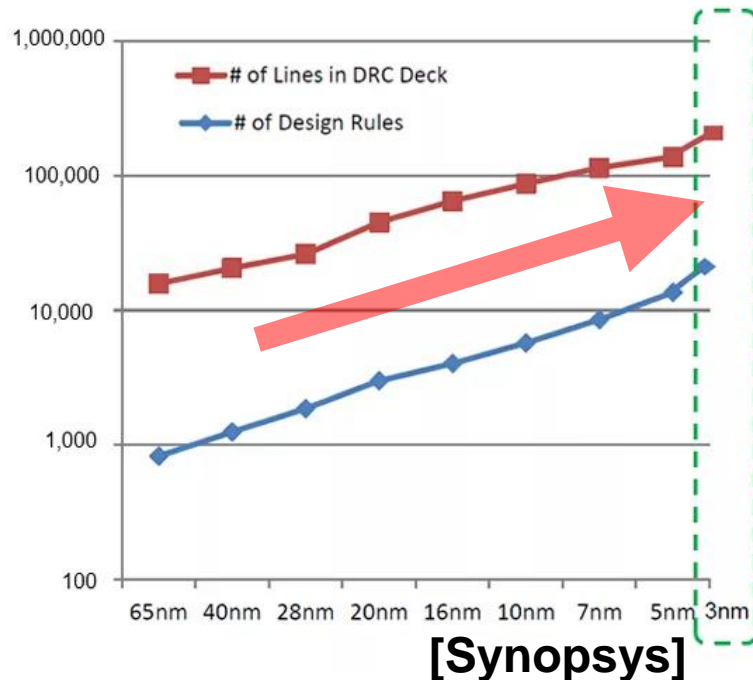
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Motivation

- **Advanced technology nodes**
 - Increased design rule & sign-off flow complexity
 - High human & time resources requirement
 - High cost in custom layout design process

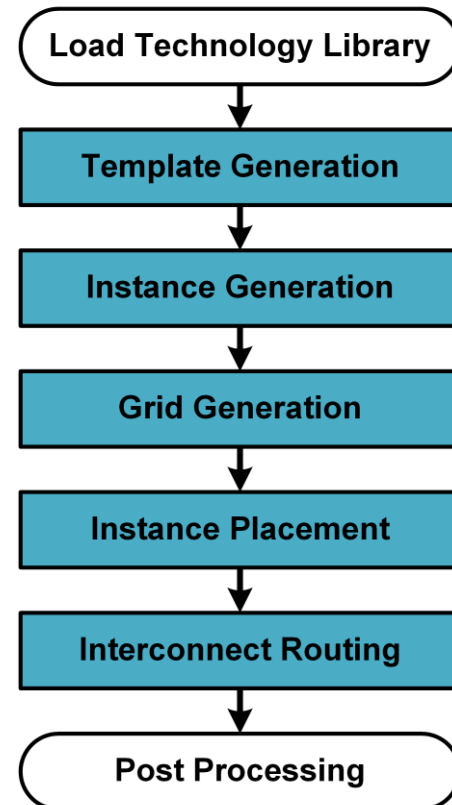
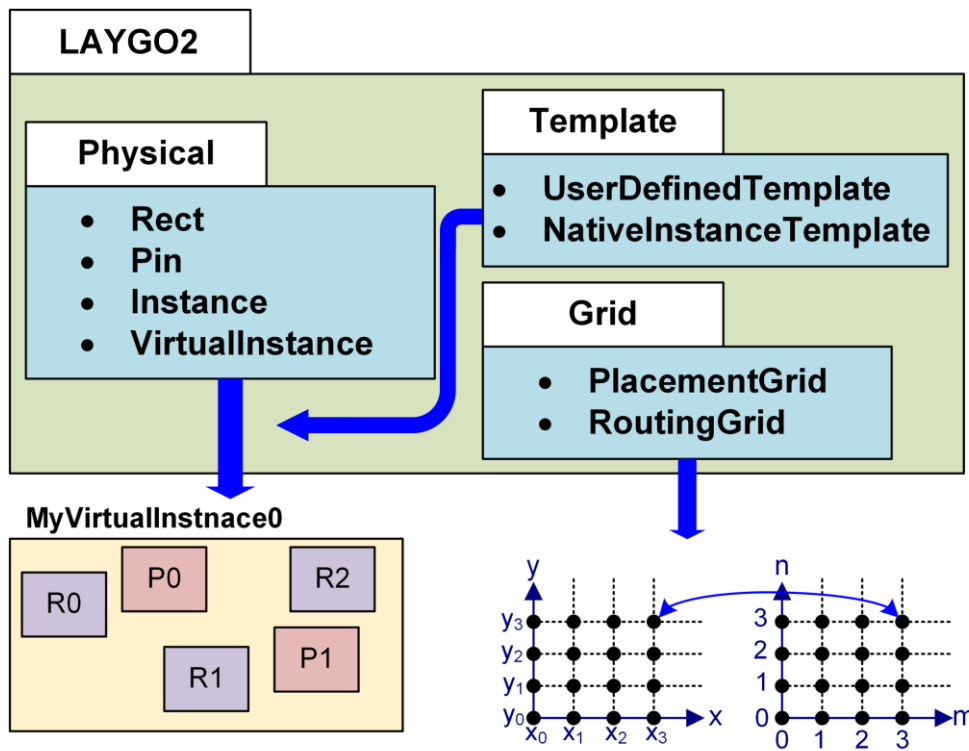
⇒ **Need automated layout generation !**



Automated Layout Generation Framework

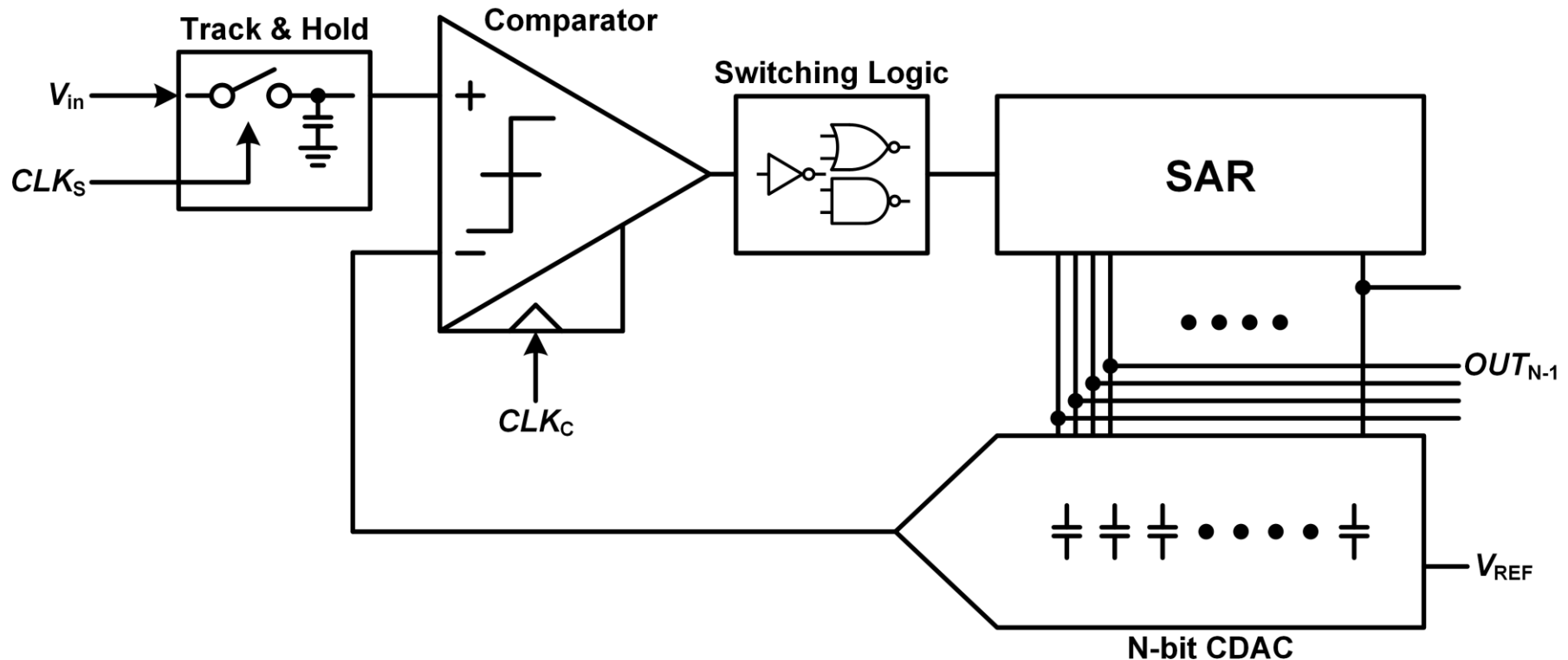
■ LAYGO2

■ Gridded object-based layout generation framework



SAR ADC Building Blocks

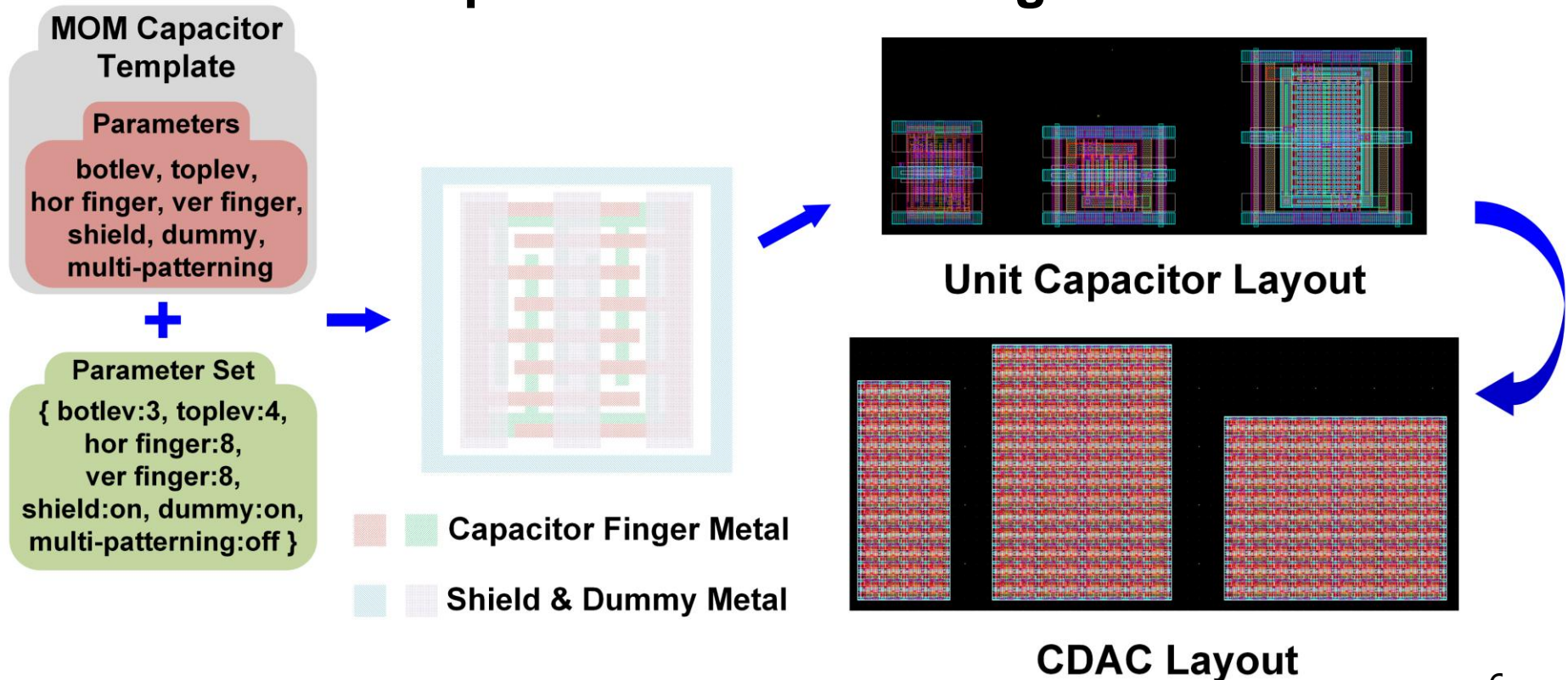
- SAR ADC architecture
 - CDAC, comparator, track & hold, and switching logic



Layout Generation (1/3)

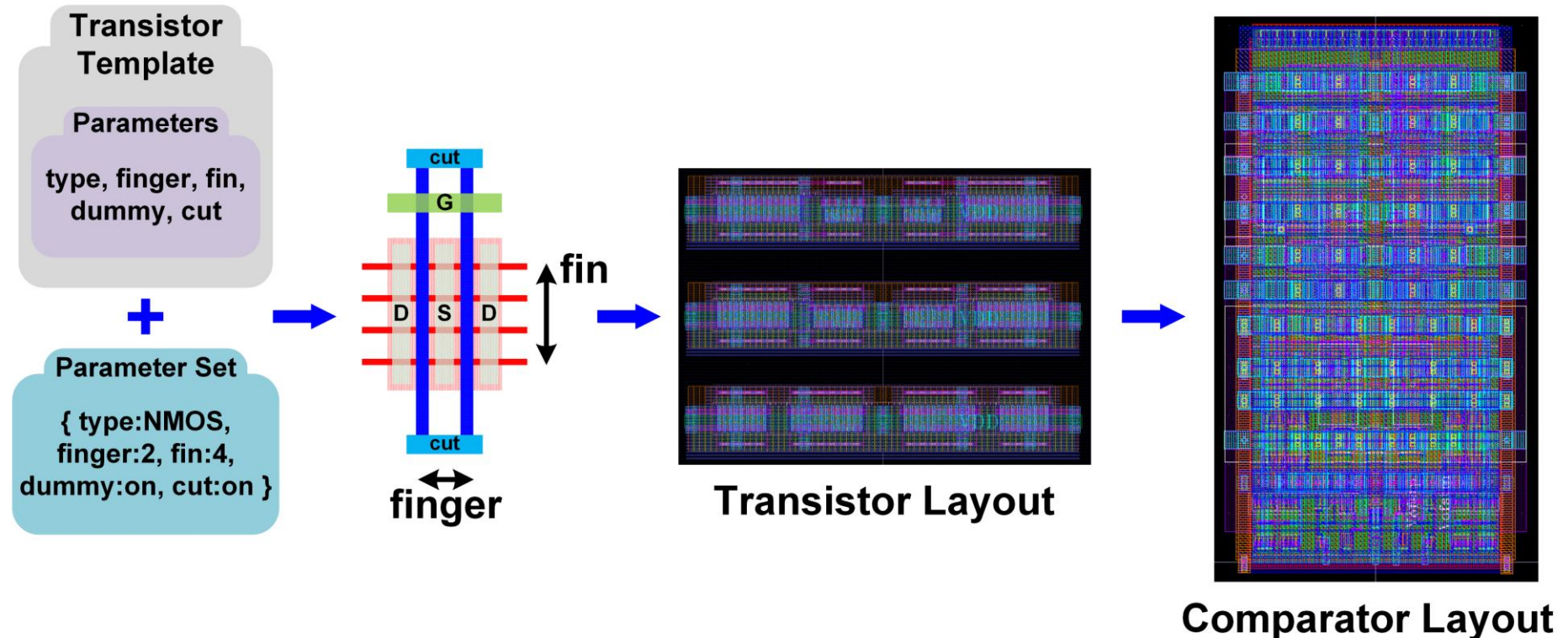
■ CDAC layout

- **Software-Defined Template** (*UserDefinedTemplate*) for MOM capacitor
- **Grid-based placement and routing**



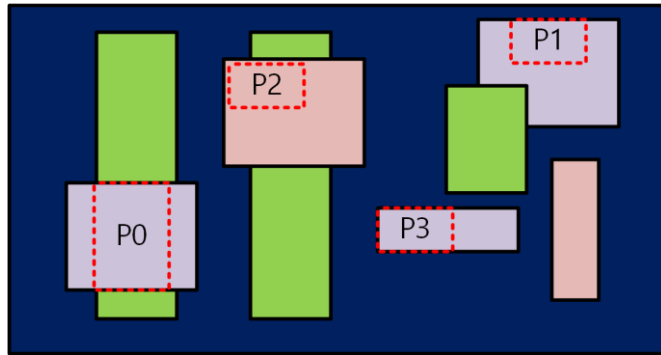
Layout Generation (2/3)

- **Comparator layout**
 - **Software-Defined Template** (*UserDefinedTemplate*) for transistors
 - **Grid-based placement and routing**

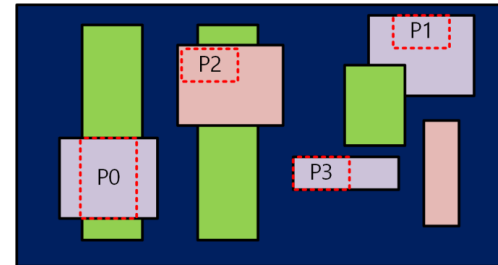


Layout Generation (3/3)

- Track & hold, switching logic layout
 - **Wrapper Template** (*NativeInstanceTemplate*) for manual structures
 - Efficient area with hand-crafted layout



Hand-crafted Layout

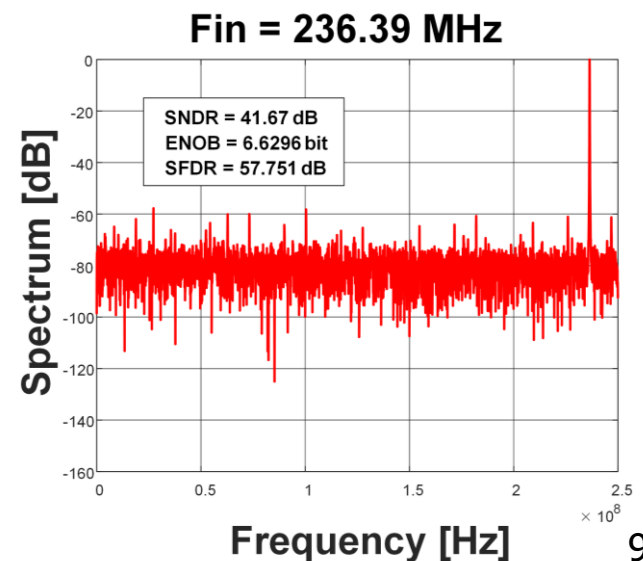
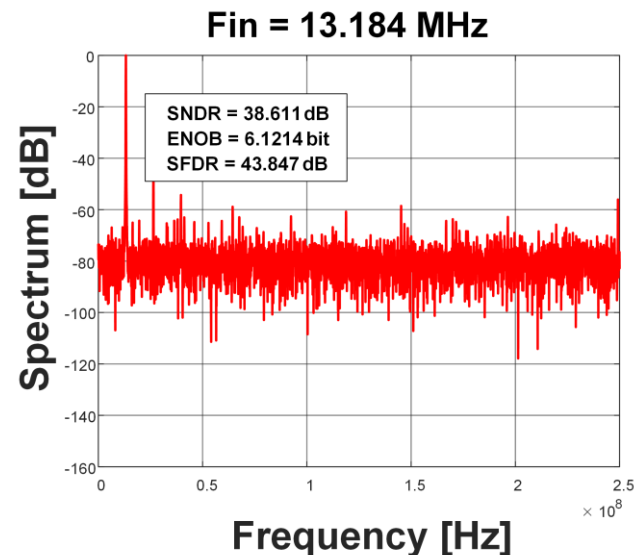
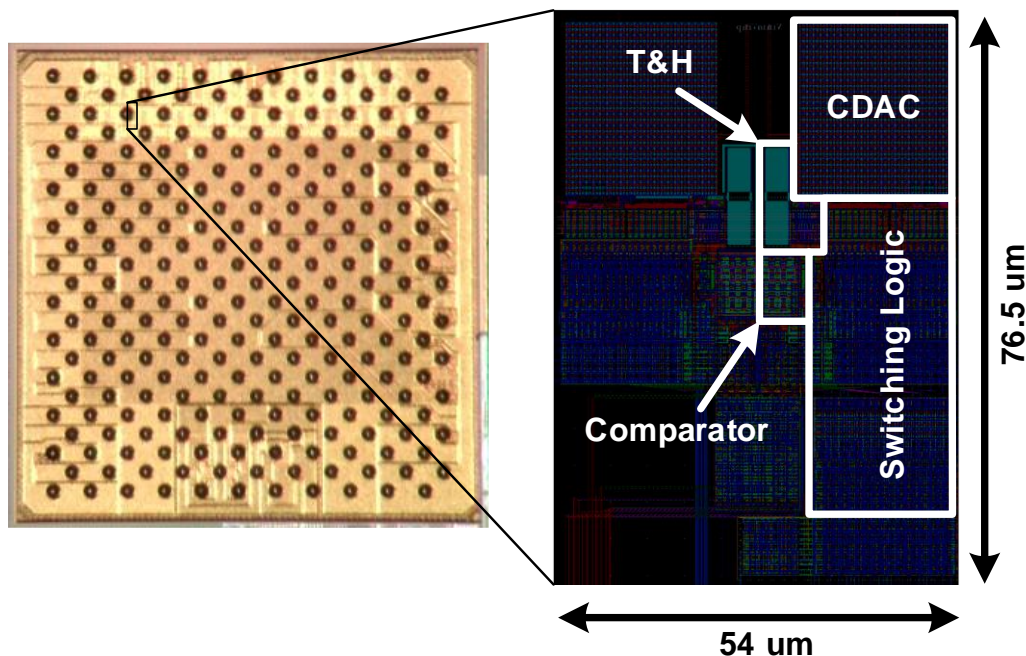


Physical Information

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Measurement Results

- **Generated SAR ADC**
 - Fabricated in 14-nm FinFET
 - Occupies 4,131 μm^2
 - 500 MS/s with 8-bit resolution



Conclusion

- **Automated layout generation in advanced technology nodes**
 - Essential for addressing increasing complexity in custom designs
 - **SAR ADC layout generation with LAYGO2**
 - Grid-based placement and routing
 - Customizable template for each building block
- ⇒ **Foundation for enhanced design efficiency**
- Layout mismatch mitigation
& Layout productivity improvement**