UC San Diego

Standard Cell Layout Generation: Review, Challenges, and Future Works

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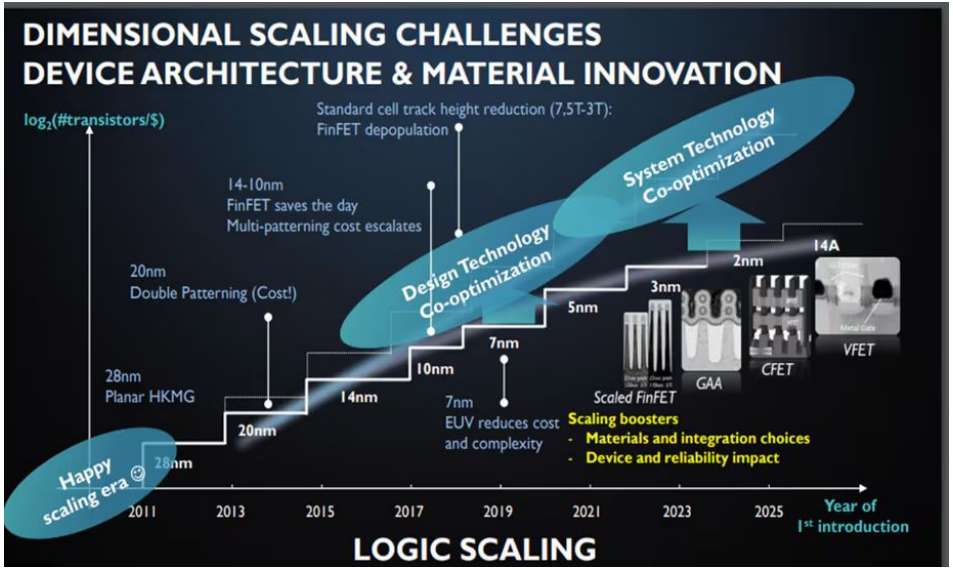
Outlines

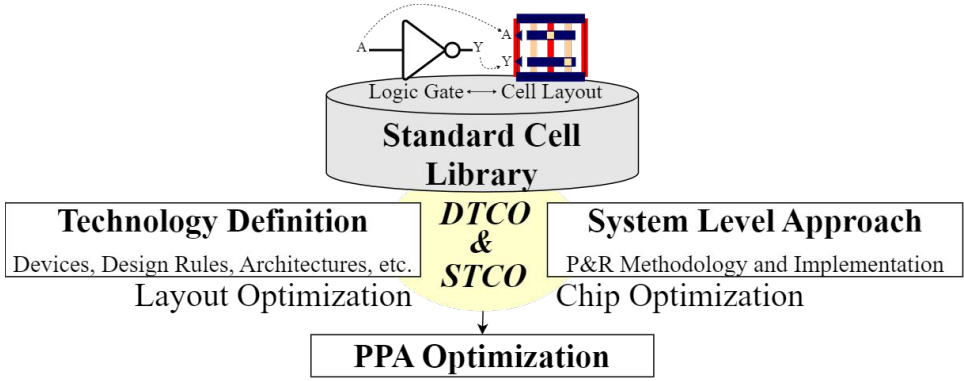
1. Motivation
2. Review : Placement and Routing with Tool Sets
3. Challenges : Complexity and Optimality
4. Future Works : Optimization and New Devices
5. Conclusion

Motivation: Relentless Demand for Scaling

- **Standard cells are one pivotal brick for chip power, performance, and area (PPA) scaling**

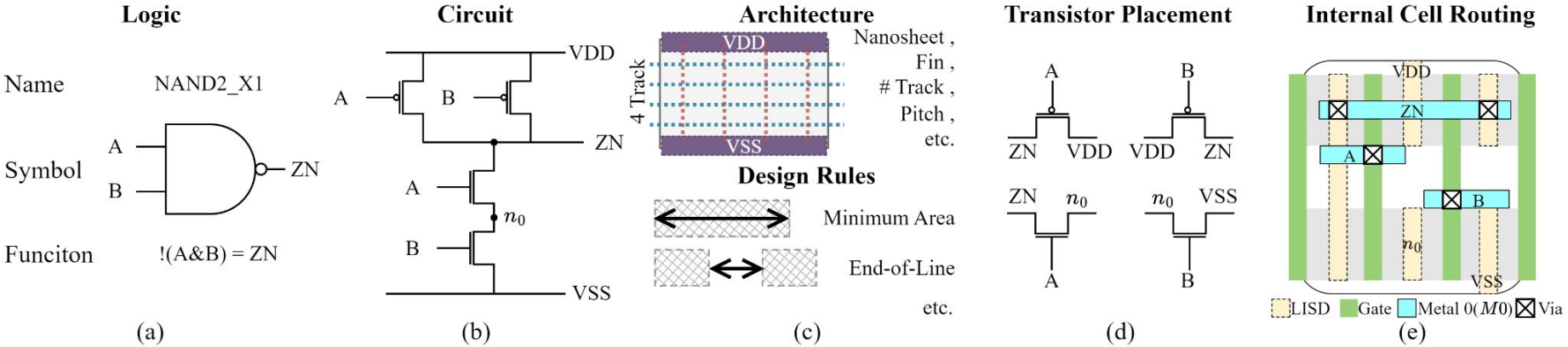


IMEC logic scaling loadmap



Motivation: Standard Cell Design Flow

- **NP-complete with limited problem sizes**



Review : Cell Layout Automation

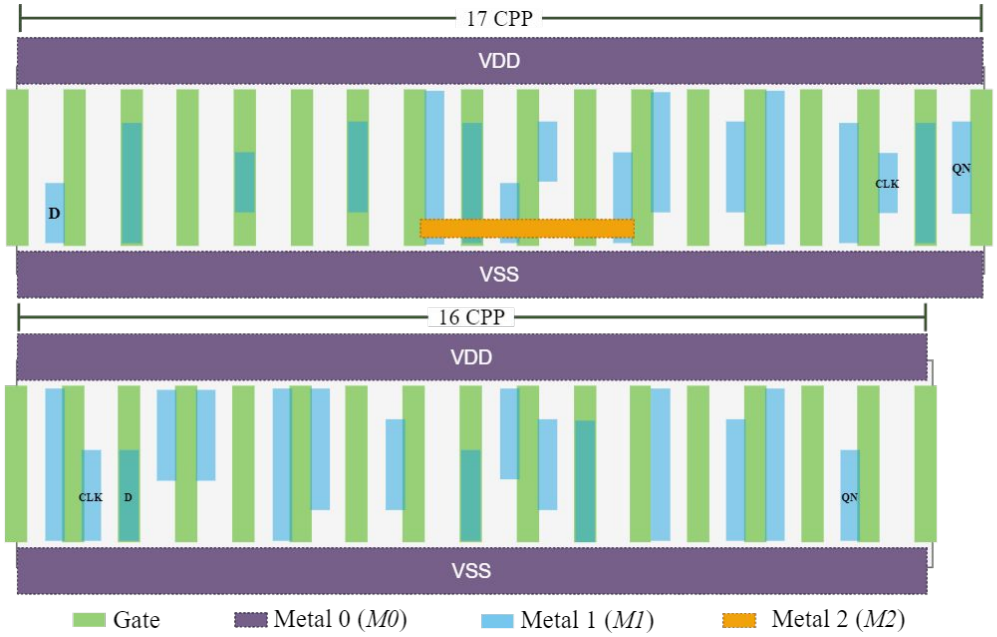
- **Cell generators for sub-10nm node covering placement and routing**

	Algorithms		Optimality (✓: meets criteria, —: bounded by constraints)					Support	
Tool	Placement	Routing	wo pre T.pair	wo T.part	T.P w rp	I.C.R w pa	runtime	DRs	Metal
NCTUCell [15]	DP	ILP	—	✓	✓	—	<90sec.(FF)	7nm [8]	bi
BonnCell [27]	S-Tree	MIP	✓	✓	✓	✓	<8hr.(FF)	7nm	uni
SP&R [12]	SMT	SMT	✓	—	✓	✓	<1hr.(FF)	7nm	uni
MCell [14]	A*	MAX-SAT	—	—	✓	—	<81min.(4BFF)	7nm	bi
NVCell [22]	SA, RL	GA, RL	✓	—	✓	✓	N/P	~5nm	uni
*i*tplace [13]	S-Tree, CNN	ILP [15]	✓	—	✓	—	N/P	7nm	bi
CSyn-fp [3]	S-Tree	SMT [12]	—	—	✓	✓	<18min.(FF)	7nm	bi
SMTCell [6]	SMT	SMT	✓	—	✓	✓	<94min.(LHQ)	3nm [24]	uni

Table 1: Comparison of cell layout generation tools based on their algorithms and optimality criteria. Abbreviations are as follows: wo pre T.pair: without pre-transistor pairing, wo T.part: without transistor partitioning, T.P w rp: transistor placement with routing prediction, I.C.R w pa: internal cell routing with pin accessibility metric, DRs: supporting design rules, Metal: lowest metal's routing direction, N/P: Not Provided.

Challenges : Complexity & Optimality

- **Transistor Partitioning**
  - **Reduces the search space**
  - **Misses the best solution**



(a)

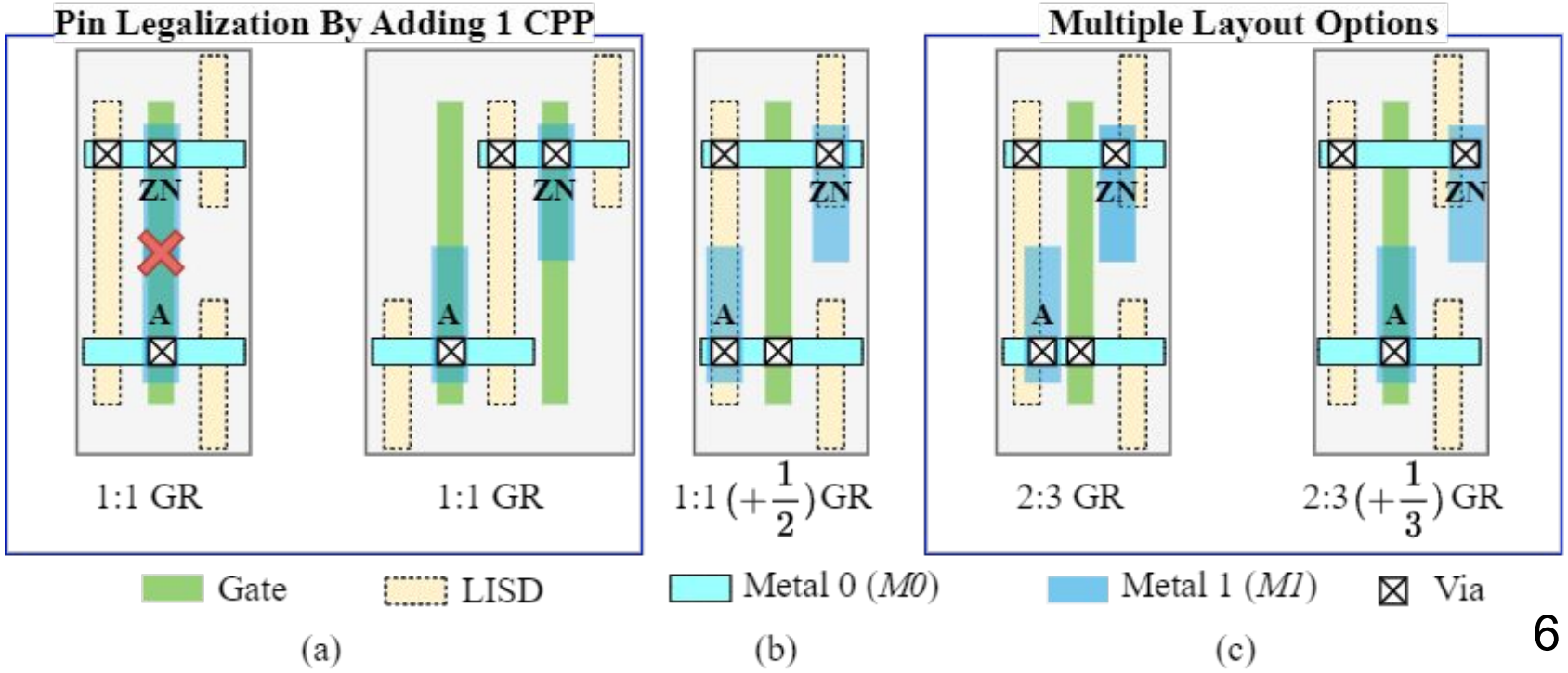
Design hierarchy based partitioning
Fast / Not optimal

(b)

Exhaustive search
Slow / Optimal

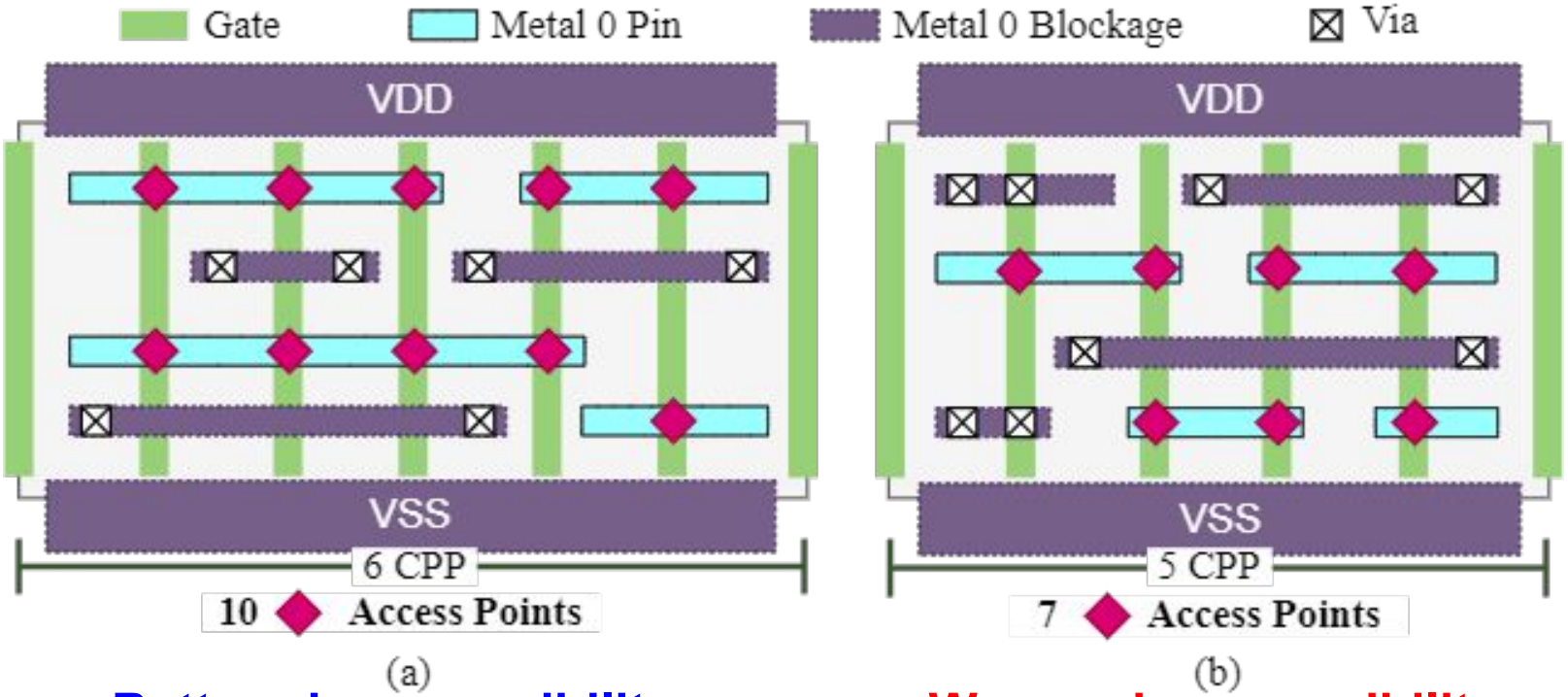
Challenges : Complexity & Optimality

- **Gear Ratio & Offset**
  - **More routing resources with added complexity**
  - **E.g. 2:3 GR spans a non-uniform grid**



Challenges : Complexity & Optimality

- **Design Trade-offs**
  - **Cell Area vs Pin accessibility**

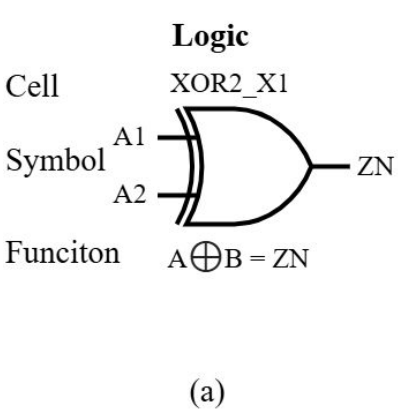


Better pin accessibility
Bigger area

Worse pin accessibility
Smaller area

Future Works: Optimization & New Devices

- **Logic Optimization**
  - **Expand search space for optimality**
  - **Produce multiple design possibilities**



Truth Table & Boolean Equations

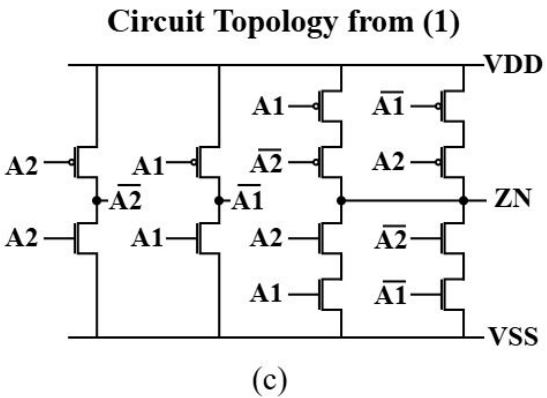
A1	A2	ZN
0	0	0
0	1	1
1	0	1
1	1	0

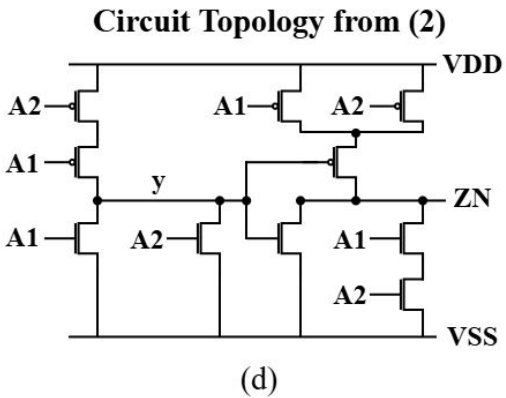
$ZN = \overline{A1} \cdot A2 + A1 \cdot \overline{A2}$ (1)

$ZN = \overline{(y + A1 \cdot A2)}$ (2)

$y = \overline{(A1 + A2)}$

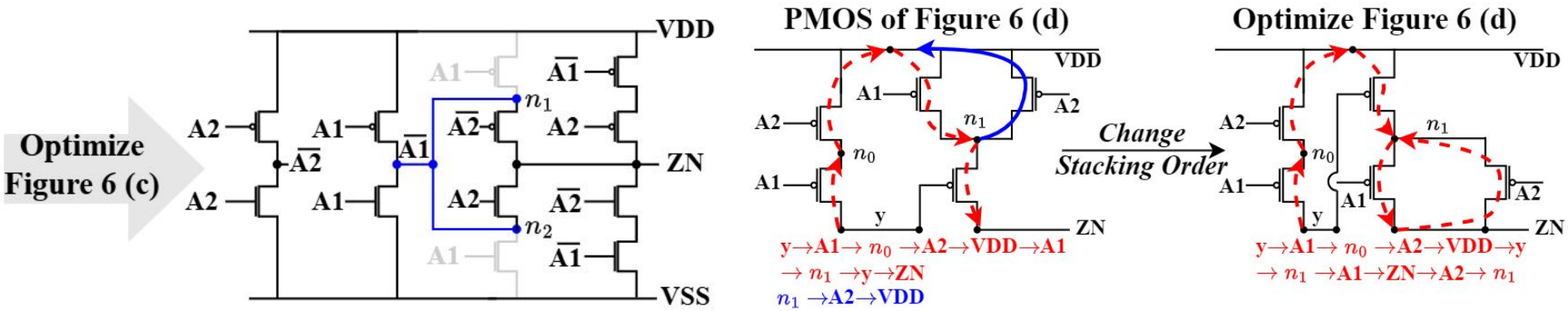
(b)





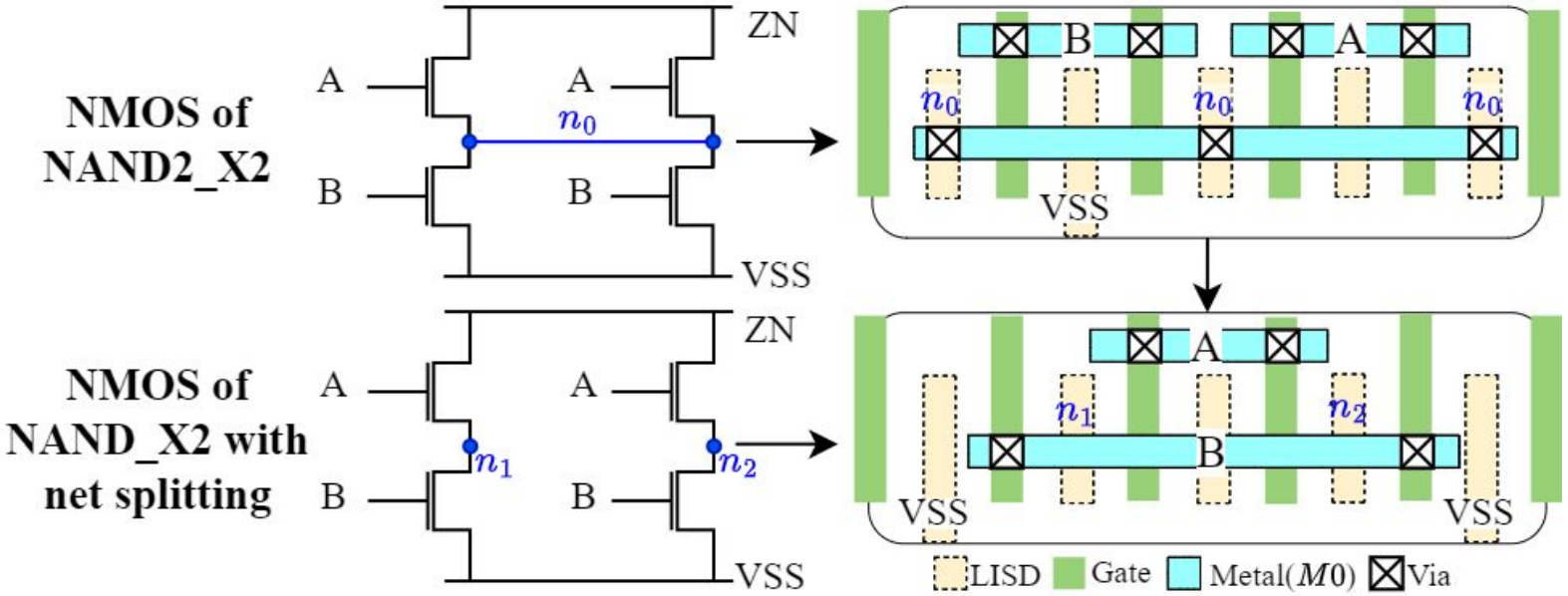
Future Works: Optimization & New Devices

- **Topology optimization - 1**
  - Internal net state verification for transistor removal
  - Changing stack order for better Euler path



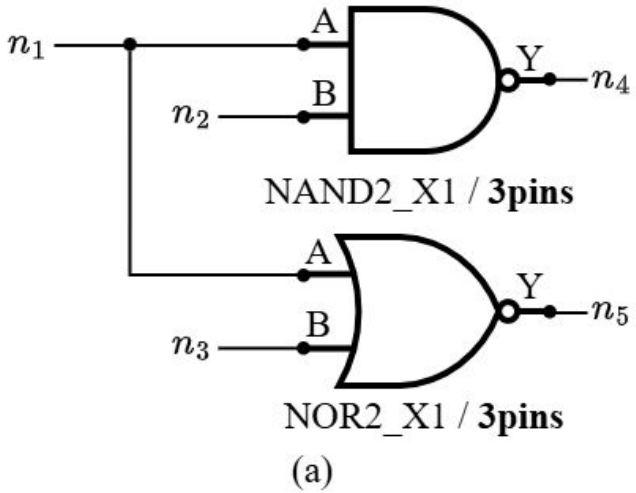
Future Works: Optimization & New Devices

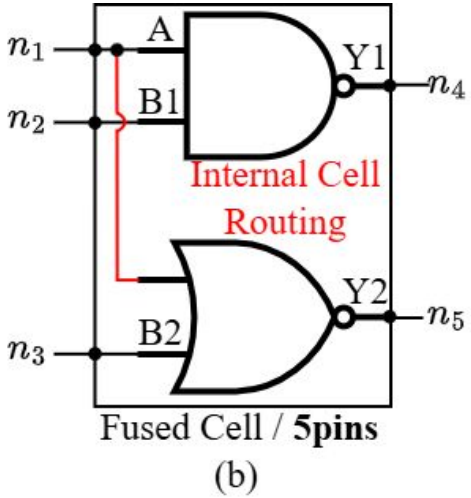
- **Topology optimization - 2**
  - **Increasing the drive strength of cell differently**
  - **Net splitting can improve circuit performance**

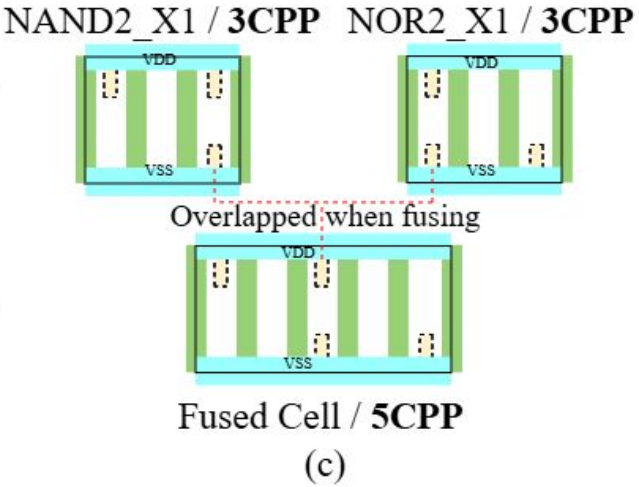


Future Works: Optimization & New Devices

- **Standard cell fusion**
  - **Pin density wall**
  - **Fused cell can reduce pin count and cell area**

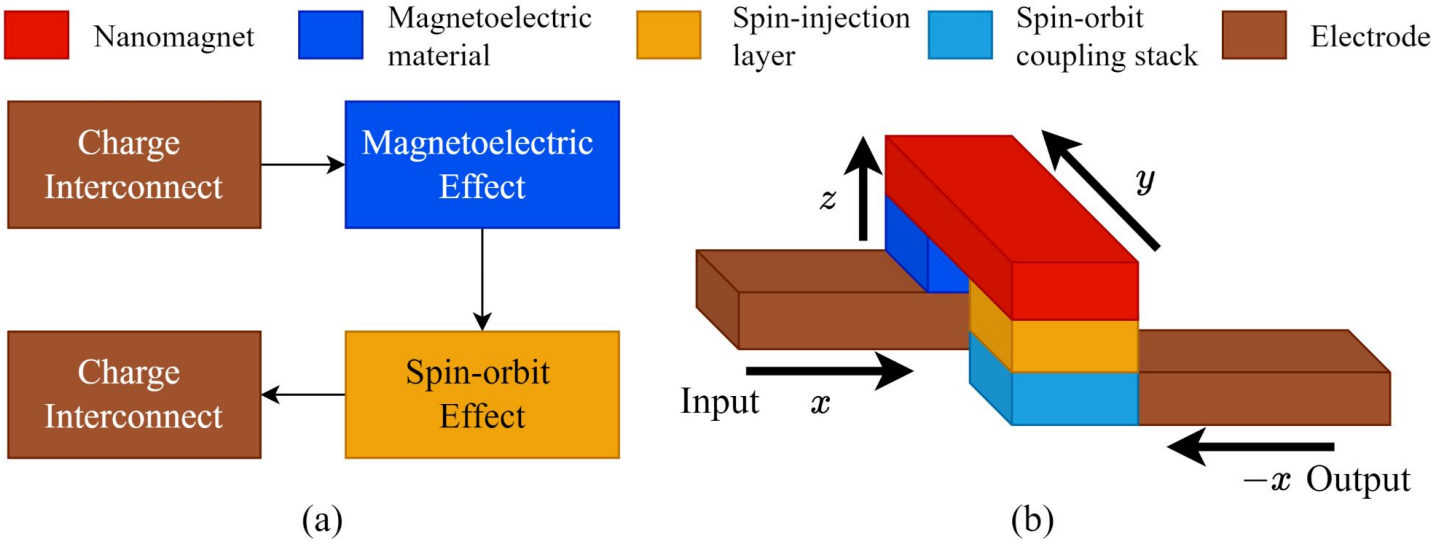






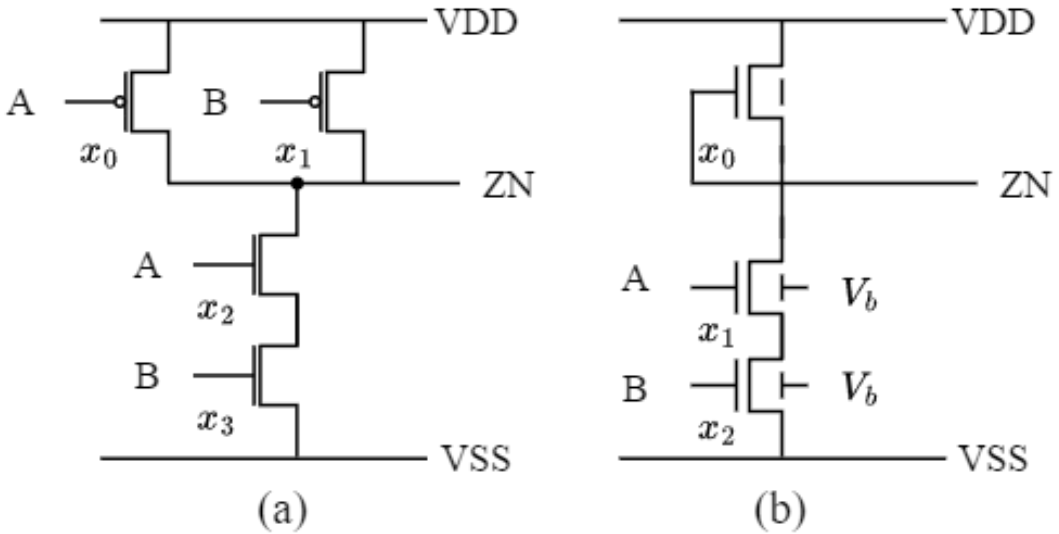
Future Works: Optimization & New Devices

- **Magnetoelectric Spin–Orbit (MESO) Device**
  - **Address the limitations of traditional CMOS scaling**
  - **Use the majority function and has a compatible process with current VLSI technology**



Future Works: Optimization & New Devices

- **Thin Film Transistors (TFT)**
  - **Widely adopted in digital displays and is being researched for low-cost logic circuit applications and low temperatures**
  - **Only operate with n-channel logic**



Conclusion

- NP-complete with limited problem sizes
- Payoff for PPA improvement
- DTCO/STCO + engineering R&D
- Larger scopes for further improvement

Thank you!