SI-Aware Wire Timing Prediction at Pre-Routing Stage with Multi-Corner Consideration

Yushan Wang[1], **Xu He**[1], Renjun Zhao[1], Yao Wang[2], Chang Liu[2], Yang Guo[2]

[1]Hunan University, [2]National University of Defense Technology

Changsha, China

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Outline

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03 Overview

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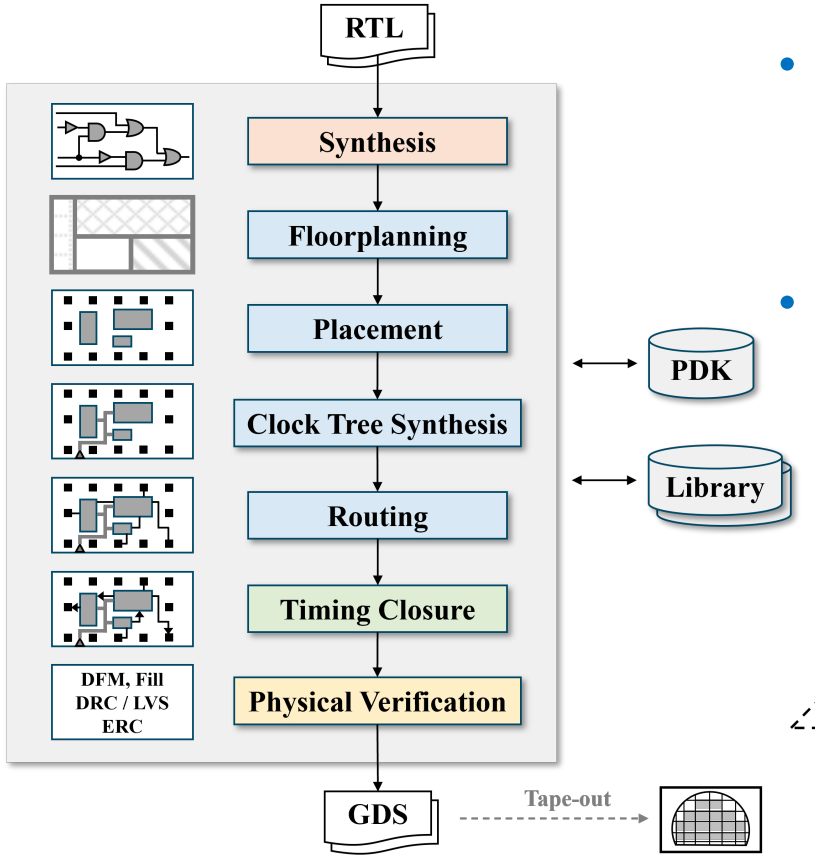
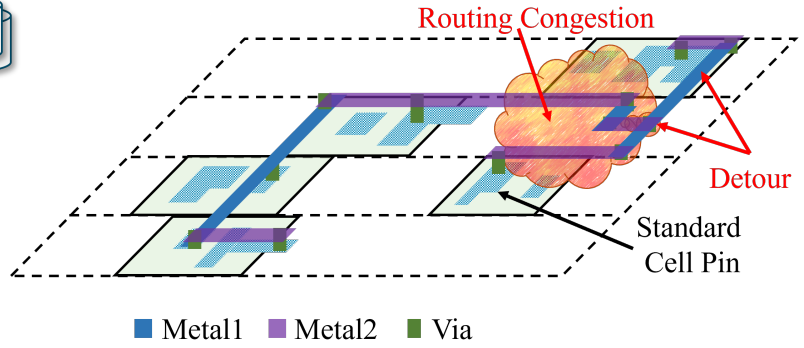
Motivation

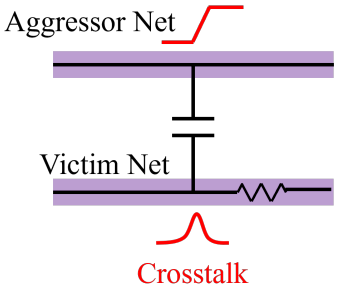
- Timing analyze throughout entire design flow
- Earlier the intervention stage, greater the room for optimization



- Signal Integrity (SI) Effect
  - Crosstalk and noise propagation
  - SI analyze typically in post-routing, electrical and logical

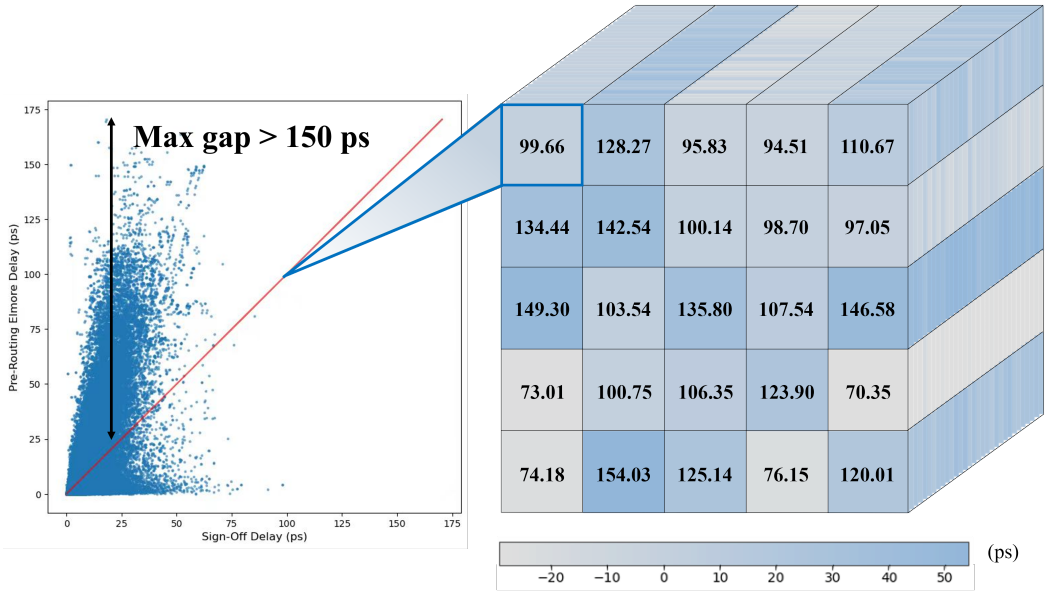
- Challenges in Pre-Routing Timing
  - Absence essential physical info, i.e., routing, congestion





Motivation

- Pre-routing wire timing challenges:
  - Lack of routing info
  - Model oversimplification
  - Elmore vs. Sign-Off, gap >150 ps
  - Even worse in multi-corner variations
- Solution
  - Develop SI-aware prediction model
  - Multi-corner consideration



(a) (b)

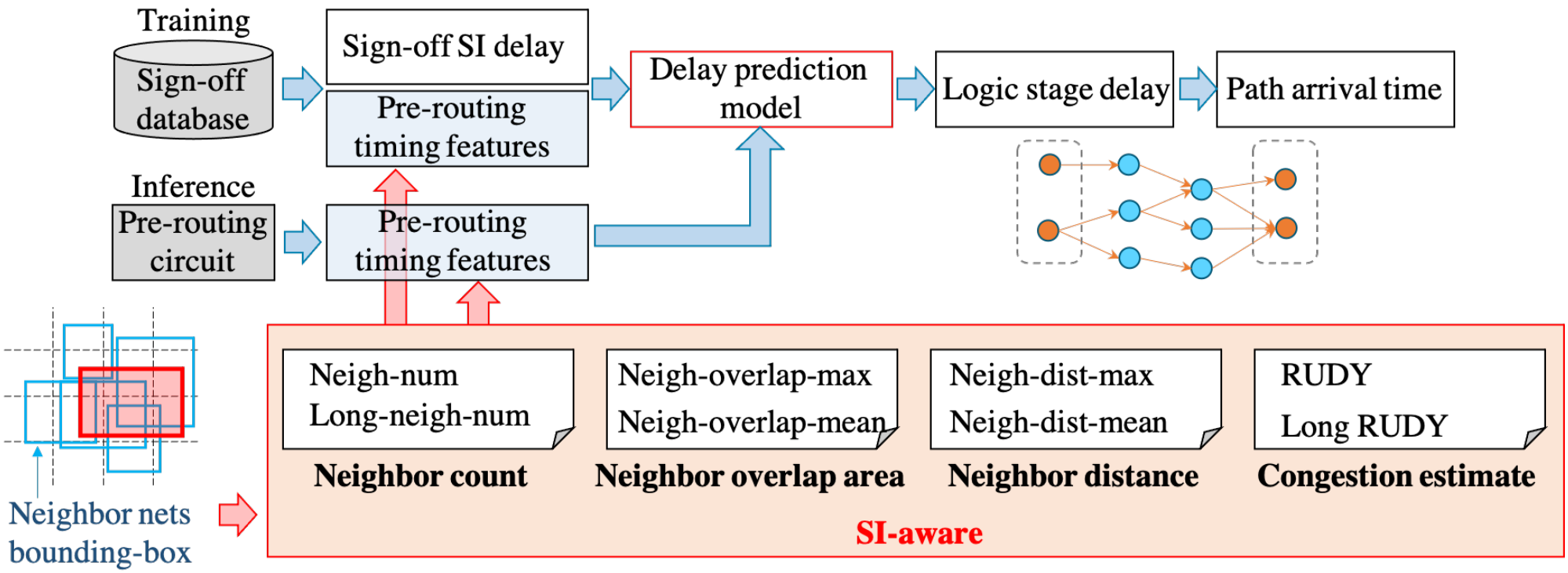
(a) Difference between Elmore and sign-off at typical corner
(b) Path delay among different PVT corners.

SI-Timing Prediction Formulation

- Prior Machine Learning Predictions:
  - Trade-off between accuracy and computationally expensive
  - Pre-placement stage
  - Placement stage
  - Post-routing and sign-off stage

- Problem Formulation:
  - Input: layout, cell library
  - Golden timing reports in SI mode under multi-corners (For training and evaluation)
  - Output: Wire delay, corresponding path AT, and critical path
  - Objective: Minimizes the discrepancy between prediction and the golden timing.

Overview

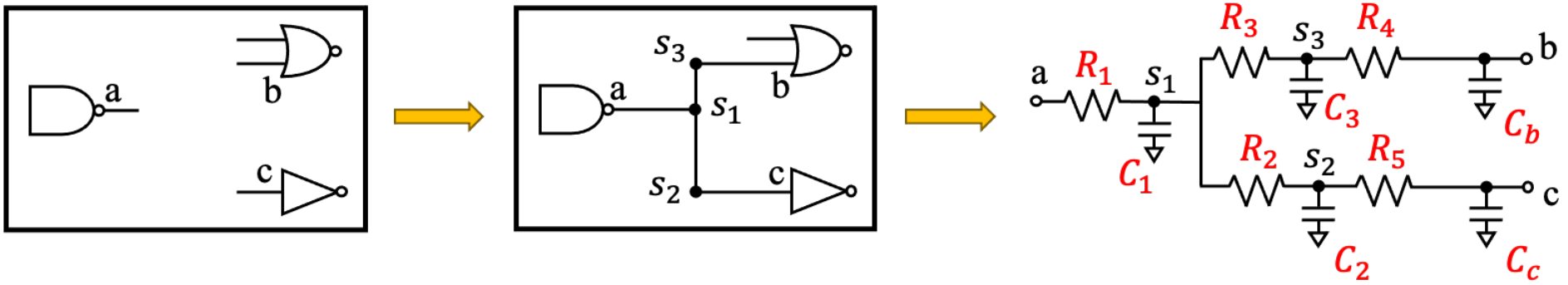


Framework of our method

Key Techniques: Feature Selection & Extraction Method

- Feature selection is critical, three kinds factors:
  - Net-itself feature: Basic RC info
  - Neighboring nets related feature: SI-Aware
  - PVT corner: Multi-corner consideration

- Routing info unavailable at pre-routing
- Lookahead RC Network: based on Steiner tree-based trial routing



Location Fast Trial Routing Lookahead RC Tree

Key Techniques: Feature Selection & Extraction Method

- Net-itself features (driver output pin to a target sink input pin)

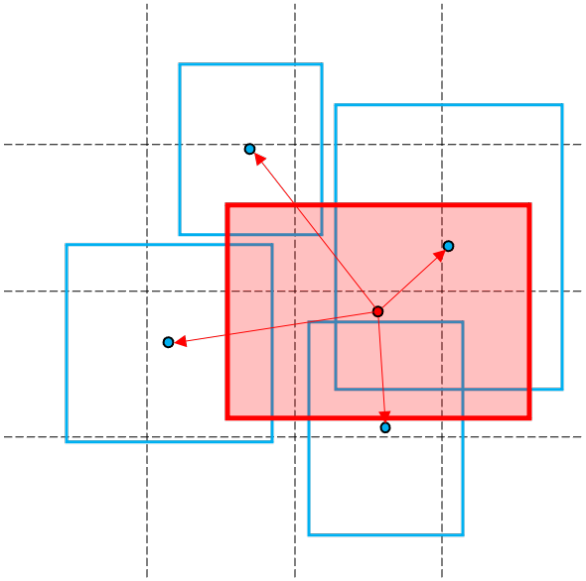
Type	Feature	Reference
Net-Itself	Sink-slew	Lookahead RC tree/predict
	Driver-slew	Lookahead RC tree & lib
	Sink-cap	Lookahead RC tree
	Driver-cap	
	Elmore	
	Context-Elmore	
	D2M	
	Driver-strength	Netlist
	Fanout-num	
	Distance	Steiner-Tree
	Steiner-demand	
	Max-dist	Placement input

- Driver-related
- Sink-related
- Connection info

Lookahead trial routing

Key Techniques: Feature Selection & Extraction Method

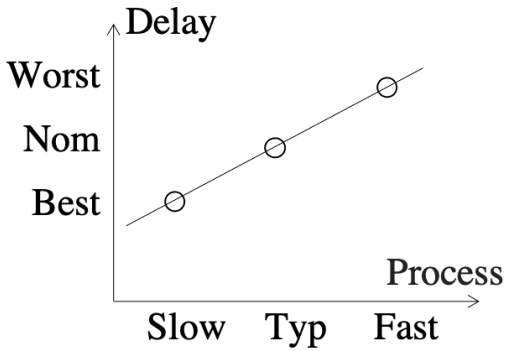
- Neighbor-net (SI-aware) features
  - Routing congestion
  - Detouring probability for long-range
  - Crosstalk from adjacent nets



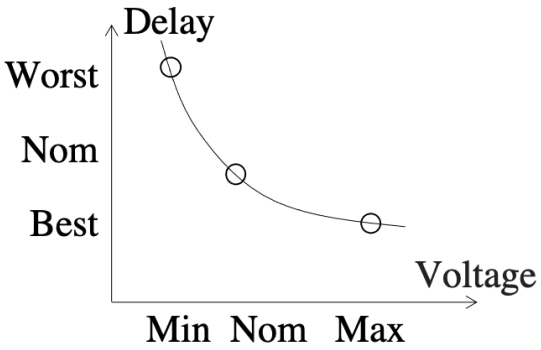
Type	Feature	Reference
Neighbor-Net	Neigh-num	Placement input
	Long-neigh-num	
	Neigh-overlap-max/mean	
	Neigh-dist-max/mean	
	RUDY	
	Long-RUDY	

Key Techniques: Feature Selection & Extraction Method

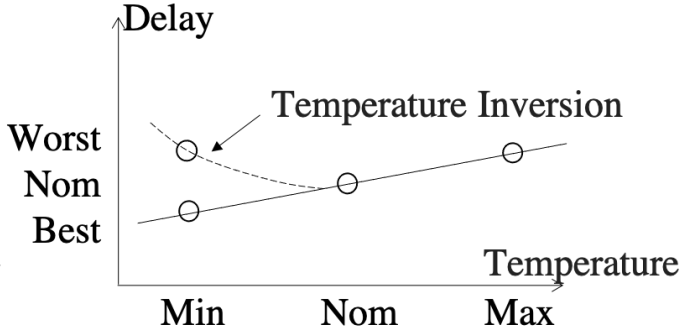
- PVT Corner features
  - Temperature (i.e., $-40°C, 0°C$, $25°C$ and $125°C$)
  - Voltage (i.e., 0.81V, 0.9V, and 0.99V)
  - RC (i.e., RC-best, RC-worst, C-best, C-worst, and etc.)



(a) Process vs. Delay



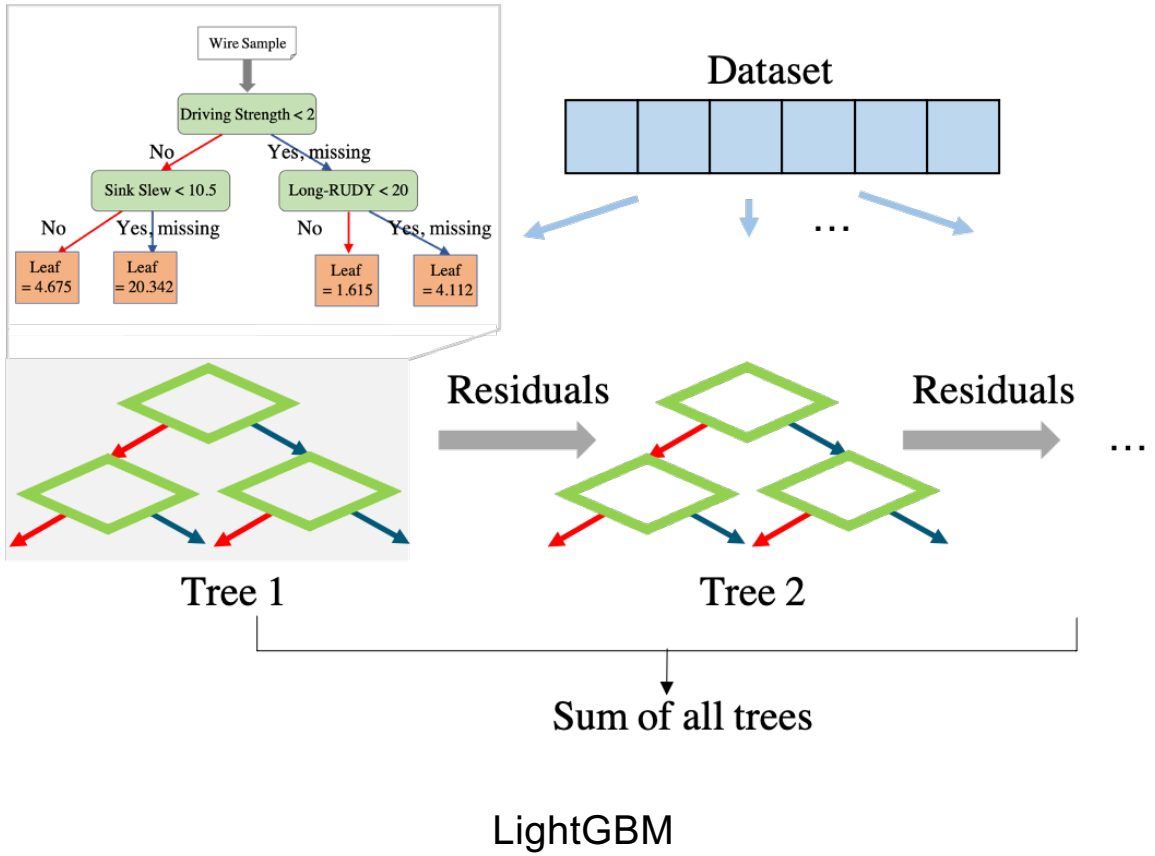
(b) Voltage vs. Delay



(c) Temperature vs. Delay

Key Techniques: Machine Learning Algorithm & Timing Inference

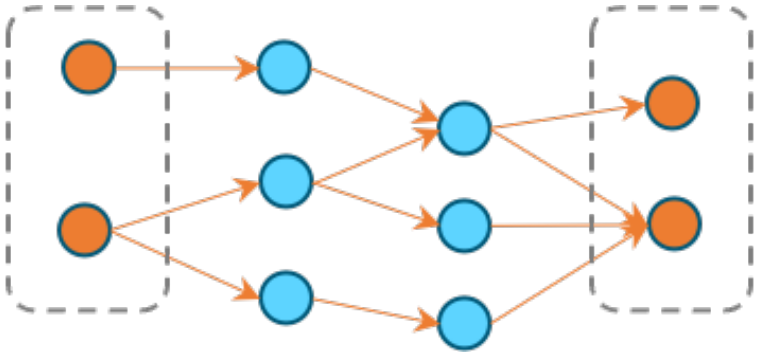
- ML-based timing prediction model:
  - Decision tree models
    - RF
    - XGBoost
    - LightGBM (3 × faster in training)
  - GNNs
  - Traditional models
- Advantages of LightGBM:
  - Histogram-based feature discretization
  - Leaf-wise growth strategy
  - Parallel acceleration



LightGBM

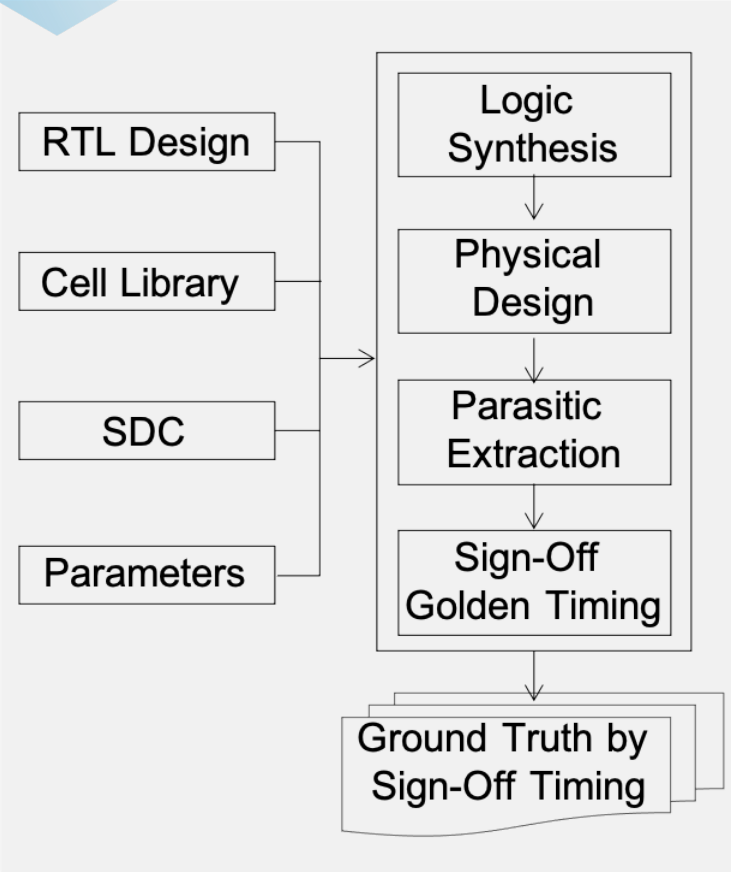
Key Techniques: Machine Learning Algorithm & Timing Inference

- Path Timing:
  - Delay from timing prediction
  - Traverse netlist as Directed Acyclic Graph (DAG) in topology order
  - Endpoint arrival time, slack



- Implementation
  - Delay prediction
  - Integrated into OpenTimer tool

Experimental Result: Dataset Preparation



Dataset Preparation

Benchmark Suite Information

Circuit	#Cells/Corner	#Nets/Corner	#FFs/Corner	#Samples
b11	3,000	3,120	132	9,794
b12	5,644	6,100	476	19,426
b13	1,124	1,272	180	3,288
b14	41,304	42,108	1,024	122,710
b20	106,248	108,304	2,068	313,920
b21	87,968	90,056	2,104	275,848
b17	104,172	110,124	6,084	371,510
b22	92,800	95,980	3,120	316,698
CV32	120,537	129,804	8055	477,048
CVA6	194,702	197,240	23,195	4,814,028

The circuit data is the total number of all implementations.

~7 Million

- ITC'99, Risc-V benchmarks circuits
- 28-nm industry process
- SI-mode timing reports across multiple PVT corners

Experimental Result: Typical Corner Timing Prediction Analysis

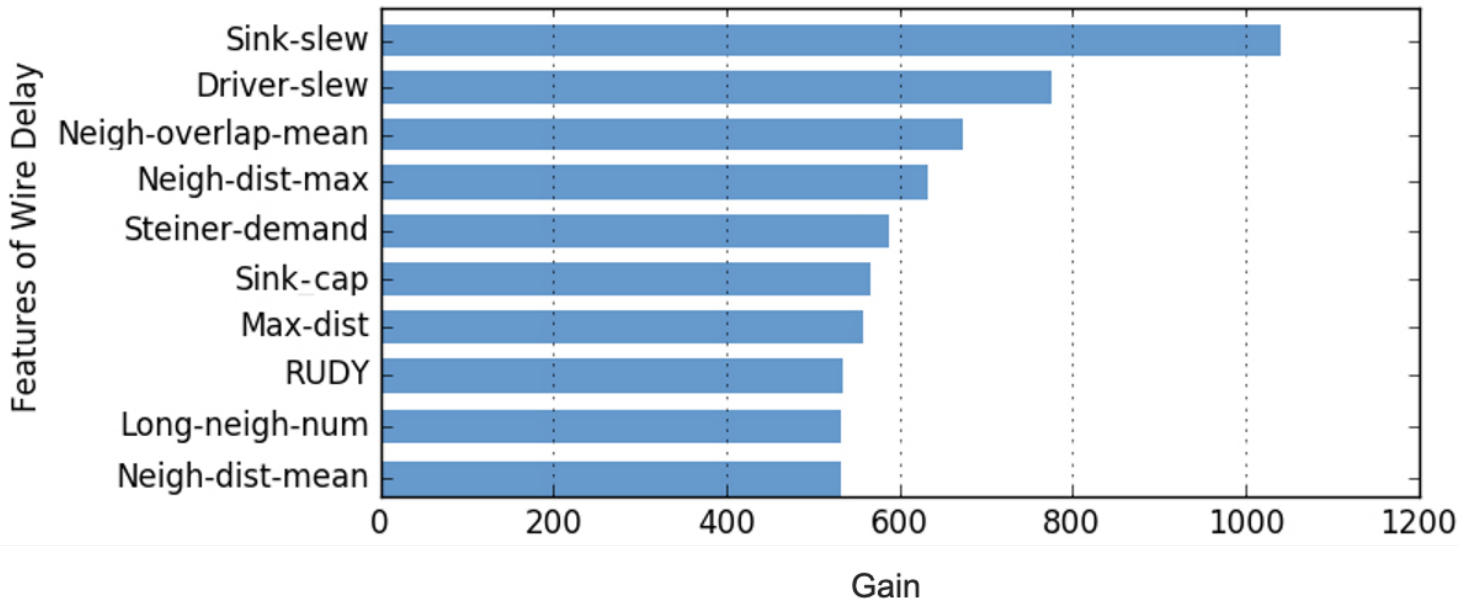
Analysis on Wire Delay Prediction under Typical Corner

Circuit	DAC'20 [4]				MLCAD'22 [5]				Ours			
	SCorr / TCorr	SMax / TMax	SMean / TMean	SCPU / TCPU	SCorr / TCorr	SMax / TMax	SMean / TMean	SCPU / TCPU	SCorr / TCorr	SMax / TMax	SMean / TMean	SCPU / TCPU
b11	0.632 / 0.824	46.66 / 46.66	10.44 / 3.54	0.001 / 0.003	0.601 / 0.801	43.27 / 43.27	12.25 / 4.78	0.001 / 0.003	**0.806** / **0.902**	45.80 / 45.80	9.64 / 3.74	0.002 / 0.008
b12	0.717 / 0.872	42.65 / 49.36	11.37 / 4.02	0.002 / 0.010	0.661 / 0.846	42.54 / 44.58	13.31 / 5.42	0.002 / 0.007	**0.793** / **0.906**	52.75 / 53.20	11.38 / 4.57	0.015 / 0.015
b13	0.496 / 0.758	48.59 / 48.59	12.81 / 7.10	0.001 / 0.002	0.417 / 0.724	46.67 / 46.67	14.23 / 9.31	0.001 / 0.002	**0.668** / **0.836**	46.53 / 46.53	13.79 / 8.54	0.001 / 0.004
b14	0.673 / 0.839	65.63 / 65.63	10.06 / 5.82	0.016 / 0.032	0.681 / 0.854	62.08 / 62.08	12.77 / 7.76	0.015 / 0.030	**0.736** / **0.878**	74.28 / 74.28	8.50 / 5.21	0.026 / 0.060
b17	0.697 / 0.817	83.11 / 83.11	6.89 / 4.14	0.047 / 0.091	0.700 / 0.825	71.18 / 71.18	7.66 / 4.78	0.045 / 0.088	**0.779** / **0.874**	67.80 / 67.80	5.45 / 3.41	0.075 / 0.179
b20	0.668 / 0.821	78.84 / 78.84	6.71 / 3.68	0.036 / 0.075	0.691 / 0.843	70.05 / 70.05	8.31 / 4.79	0.035 / 0.075	**0.731** / **0.866**	56.36 / 56.36	4.96 / 2.89	0.057 / 0.122
b21	0.655 / 0.810	77.93 / 77.93	7.12 / 4.08	0.033 / 0.068	0.656 / 0.820	81.71 / 81.71	8.61 / 5.16	0.031 / 0.071	**0.721** / **0.858**	71.98 / 71.98	5.30 / 3.20	0.055 / 0.113
b22	0.710 / 0.839	62.22 / 62.22	6.71 / 3.60	0.034 / 0.076	0.694 / 0.836	54.20 / 54.20	8.04 / 4.51	0.033 / 0.078	**0.784** / **0.890**	57.58 / 57.58	5.23 / 2.95	0.056 / 0.159
CV32	0.788 / 0.879	57.24 / 57.24	5.13 / 2.39	0.043 / 0.115	0.736 / 0.847	54.68 / 54.68	6.18 / 3.04	0.041 / 0.114	**0.881** / **0.934**	61.95 / 61.95	4.84 / 2.33	0.062 / 0.189
Avg.	0.671 / 0.829	62.54 / 63.29	8.58 / 4.26	0.024 / 0.053	0.649 / 0.822	58.49 / 58.71	10.15 / 5.51	0.023 / 0.052	**0.767** / **0.883**	59.45 / 59.50	7.68 / 4.09	0.039 / 0.094

- SI-sensitive: Fanout number ≥ 8 or delay ≥ 5ps
- S/Tmean, S/TMax, and S/TCorr are the mean and maximum error (ps), and correlation of SI-sensitive/Total dataset

- Typical Corner:
  - Comparison with DAC'20 and MLCAD'22 in SI mode, using our RC network and their features
  - Achieve highest correlation for both Scorr and TCorr
  - SI-sensitive dataset, our model outperforms SCorr about 10%

Experimental Result: Dataset Preparation



Contribution rank of Top-10 features in wire delay

- Sink-slew is the most crucial feature
- Other SI-associated features from neighboring nets also rank in top-10

Experimental Result: Multi-Corner Timing Prediction Analysis

- Training dataset: $ml - rcworst$ & $wcl - rcworst$
- Testing dataset: $bc - rcworst$, $tc - rcworst$, $wc - rcworst$, and $wcz - rcworst$

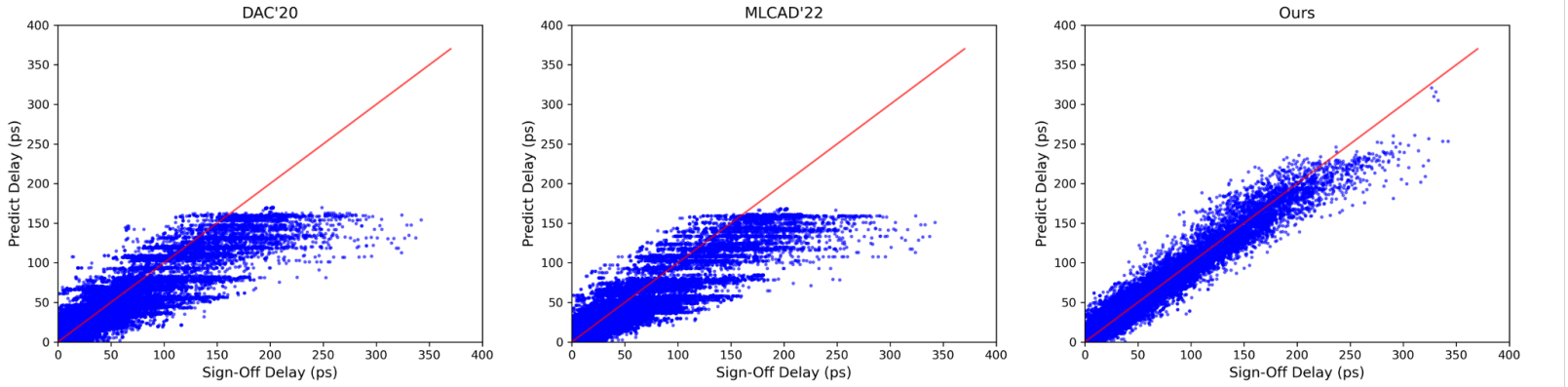
Wire Delay Prediction Analysis of Circuit **CVA6** under Multi-Corner

Circuit	DAC'20 [4]			
	SCorr / TCorr	SMax / TMax	SMean / TMean	SCPU / TCPU
$bc - rcworst$	0.928 / 0.943	129.20 / 129.20	3.84 / 2.07	0.092 / 0.202
$tc - rcworst$	0.930 / 0.944	200.73 / 200.73	5.08 / 2.69	0.101 / 0.207
$wc - rcworst$	0.927 / 0.941	210.62 / 210.62	4.98 / 2.86	0.098 / 0.203
$wcz - rcworst$	0.922 / 0.938	155.46 / 155.46	4.20 / 2.27	0.111 / 0.208
Avg.	0.927 / 0.942	174.00 / 174.00	4.53 / 2.47	0.100 / 0.205
Circuit	MLCAD'22 [5]			
	SCorr / TCorr	SMax / TMax	SMean / TMean	SCPU / TCPU
$bc - rcworst$	0.926 / 0.941	130.35 / 130.35	4.19 / 2.38	0.086 / 0.197
$tc - rcworst$	0.929 / 0.943	201.41 / 201.41	5.37 / 2.98	0.091 / 0.194
$wc - rcworst$	0.925 / 0.939	210.53 / 210.53	5.44 / 3.00	0.091 / 0.191
$wcz - rcworst$	0.921 / 0.936	156.67 / 156.67	4.65 / 2.65	0.090 / 0.194
Avg.	0.925 / 0.940	174.74 / 174.74	4.91 / 2.75	0.089 / 0.194
Circuit	Ours			
	SCorr / TCorr	SMax / TMax	SMean / TMean	SCPU / TCPU
$bc - rcworst$	**0.977 / 0.981**	96.00 / 96.00	2.82 / 1.58	0.088 / 0.301
$tc - rcworst$	**0.981 / 0.984**	88.49 / 88.49	2.82 / 1.60	0.106 / 0.282
$wc - rcworst$	**0.978 / 0.981**	99.03 / 99.03	3.25 / 1.87	0.114 / 0.376
$wcz - rcworst$	**0.979 / 0.982**	101.81 / 101.81	3.08 / 1.81	0.097 / 0.279
Avg.	**0.979 / 0.982**	96.33 / 96.33	2.99 / 1.72	0.101 / 0.310

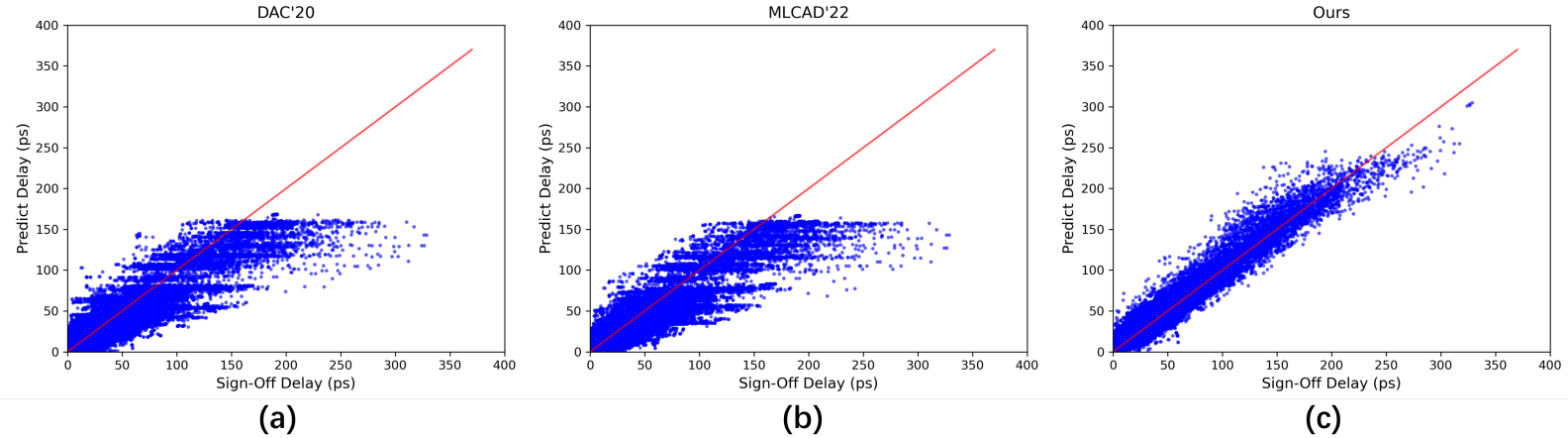
- Multi-Corner:
  - Ours achieves 0.98 correlation
  - Compared to MLCAD'22, reducing "SMax" and "SMean" by 81% and 64%

Experimental Result: Multi-Corner Timing Prediction Analysis

Wire delay prediction distribution under $wc - rcworst$ corner



Wire delay prediction of SI-sensitive distribution under $tc - rcworst$ corner



Experimental Result: Path Timing under Typical Corner

Path AT under Typical Corner

Corner	DAC'20 [4]			MLCAD'22 [5]			Ours		
	Corr	Max(ps)	Mean(ps)	Corr	Max(ps)	Mean(ps)	Corr	Max(ps)	Mean(ps)
b11	0.917	89.085	38.170	0.888	109.499	51.320	**0.947**	66.335	38.073
b12	0.861	95.251	31.901	0.847	120.914	46.965	**0.879**	78.026	37.274
b13	0.812	82.843	29.009	0.820	102.189	42.037	**0.842**	80.921	37.615
b14	0.984	230.087	142.020	0.973	316.732	200.127	**0.985**	190.163	120.066
b17	0.972	179.296	56.488	0.965	246.181	97.602	**0.980**	128.105	43.712
b20	0.971	153.476	63.592	0.961	230.480	113.060	**0.978**	119.584	53.524
b21	0.967	181.662	75.909	0.957	252.989	118.909	**0.978**	127.107	55.784
b22	0.978	201.364	88.965	0.971	259.817	130.011	**0.986**	142.347	69.576
CV32	0.998	140.681	59.179	0.998	156.617	71.702	**0.999**	101.618	54.036
Avg.	0.940	150.416	65.026	0.931	199.491	96.859	**0.953**	114.912	56.629

- Gives best correlation
- Achieves the lowest average absolute error

Experimental Result: Path Timing under Multi-Corner

Path AT of Circuit **CVA6** under Multi-Corner

Corner	DAC'20 [4]			MLCAD'22 [5]			Ours		
	Corr	Max(ps)	Mean(ps)	Corr	Max(ps)	Mean(ps)	Corr	Max(ps)	Mean(ps)
$bc - rcworst$	0.955	43.320	28.032	0.968	36.190	24.054	**0.982**	20.360	3.657
$tc - rcworst$	0.955	43.140	27.882	0.966	52.260	37.397	**0.982**	26.810	9.742
$wc - rcworst$	0.953	52.810	28.506	0.967	35.290	9.350	**0.977**	33.010	11.264
$wcz - rcworst$	0.958	26.980	12.503	0.968	36.190	24.009	**0.984**	36.250	20.491
Avg.	0.955	41.563	24.231	0.967	39.982	23.702	**0.981**	29.108	11.289

- Our correlation is the highest
- "Mean" error is 12ps smaller on average

- Path Slack:
  - SI-sensitive paths contribute 80% to critical paths
  - Since maximum error in our AT computation < 30ps, both TPR and TNR are 100%

Conclusion

- Pre-routing wire timing prediction:
  - Extract net-self RC info, neighboring nets and PVT corner
  - Sophisticated model, avoiding pessimistic simplifications.
  - Integrated with design-flow tool for path analysis
  - Achieves > 0.98 correlation with sign-off under 28nm industry process

Reference

1. [n. d.]. CV32E40P:PULP-Platform 32-bit 4-stage RISC-V CPU Core. https://github. com/openhwgroup/cv32e40p.
2. [n. d.]. CVA6 RISC-V CPU. https://github.com/openhwgroup/cva6.
3. Erick Carvajal Barboza and et al. 2019. Machine Learning-Based Pre-Routing Timing Prediction with Reduced Pessimism. In DAC. 1–6.
4. Hsien-Han Cheng, Iris Hui-Ru Jiang, and Oscar Ou. 2020. Fast and Accurate Wire Timing Estimation on Tree and Non-Tree Net Structures. In DAC. 1–6.
5. Vidya A. Chhabria, Wenjing. Jiang, Andrew B. Kahng, and Sachin S. Sapatnekar. 2022. From Global Route to Detailed Route: ML for Fast and Accurate Wire Parasitics and Timing Prediction. In MLCAD. 7–14.
6. D. G. Chinnery and K. Keutzer. 2000. Closing the Gap between ASIC and Custom: An ASIC Perspective. In DAC. 637–642.
7. C. Chu. 2004. FLUTE: fast lookup table based wirelength estimation technique. In ICCAD. 696–701.
8. S. Davidson. 1999. Characteristics of the ITC'99 Benchmark Circuits. In IEEE International Test Synthesis Workshop.
9. Luis Guerra E Silva, L Miguel Silveira, and Joel R Phillips. 2007. Efficient computation of the worst-delay corner. In Design, Automation &Test in Europe Conference & Exhibition. IEEE, 1–6.
10. Z. Guo, M. Liu, J. Gu, and et al. 2022. A timing engine inspired graph neural network model for pre-routing slack prediction. In DAC. 1207–1212.
11. S. S Han, A. B. Kahng, S. Nath, and et al. 2014. A deep learning methodology to proliferate golden signoff timing. In DATE. IEEE, 1–6.
12. Xu He, Zhiyong Fu, and et al. 2022. Accurate timing prediction at placement stage with look-ahead RC network. In DAC. 1213–1218.
13. Tsung-Wei Huang and Martin D. F. Wong. 2015. OpenTimer: A high-performance timing analysis tool. In ICCAD. 895–902.
14. D. Hyun, Y. Fan, and Y. Shin. 2019. Accurate wirelength prediction for placementaware synthesis through machine learning. In DATE. IEEE, 324–327.
15. Andrew B Kahng, Mulong Luo, and Siddhartha Nath. 2015. SI for free: machine learning of interconnect coupling delay and transition effects. In SLIP. IEEE, 1–8.

Thanks!

Q & A

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