Device-Aware Test for Anomalous Charge Trapping in FeFETs

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Motivation

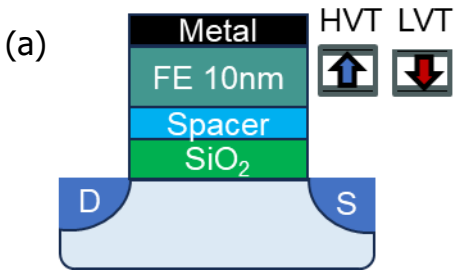
- FeFET emerges aspromising Non-Volatile Memory device [Dünkel, Stefan *et. al*., IEDM, 2017]
  - Test solutions required for manufacturing
- Testing FeFET is still in its early stages [C. Wang *et. al*., ITC, 2024]
  - Conventional defects: transistor defects, interconnect & contact defects => Traditional approach
- Challenge in testing [D. Thapar *et. al*., ITC, 2023]
  - FeFET specific working mechanism => Unique defects in FeFETs
  - Traditional approach detecting unique defects result in **high escapes**
- Solution [L. Wu *et. al*., ITC, 2018]
  - Device-aware Test specialized for unique defects
- Contributions
  - Characterization of a new unique defect "Anomalous Charge Trapping (ACT)"
  - Defect modelling & fault modelling
  - Dedicated test solutions for ACT

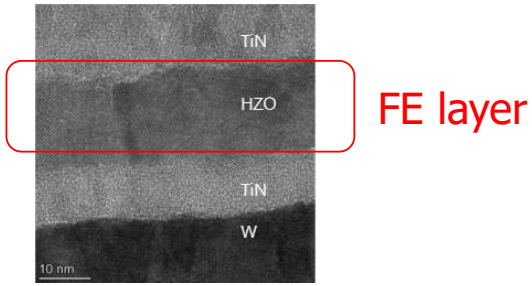
Outline

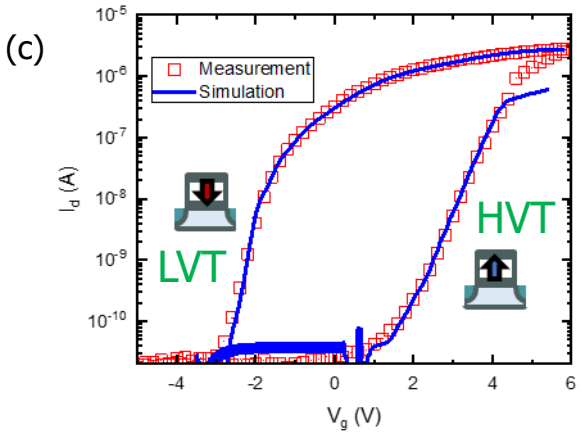
- FeFET Basics
- Defect mechanism & characterization
- Device-aware test methodology
- Defect modeling
- Fault modeling
- Test solutions
- Conclusion

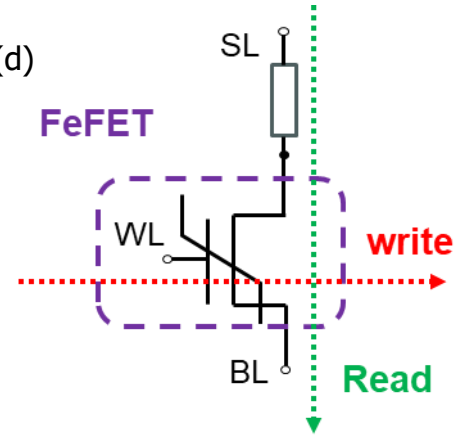
FeFET basics

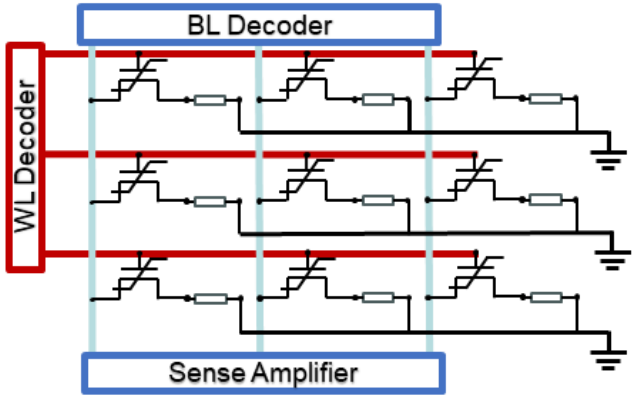
- FeFET structure:
  - Ferro-electrical layer (FE layer)
  - MOSFET-like structure
- FeFET state:
  - High threshold voltage (HVT)
    → 0 state, high resistance
  - Low threshold voltage (LVT)
    → 1 state, low resistance
- 1 FeFET-1 R cell:
  - Write operation
  - Read operation
- 3x3 FeFET array
  - NOR-Flash structure





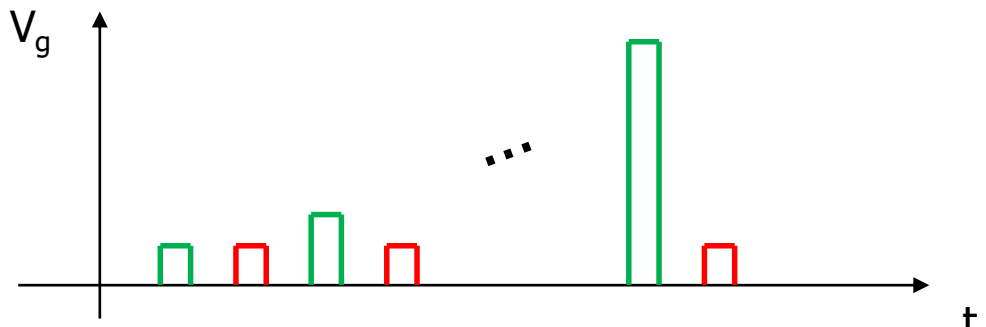






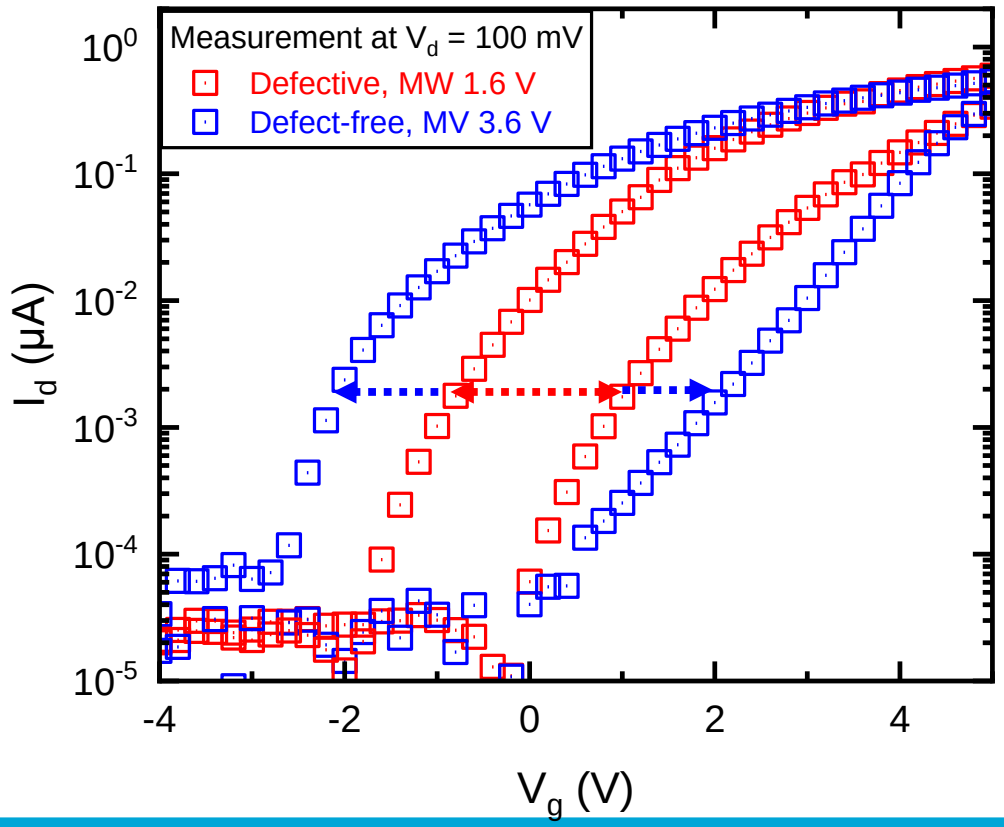
Defect mechanism & characterization

- Measurement method:
  - I_d-V_g measurement
  - Repeating 1 write-1 read
  - Write voltage sweeping in write operations



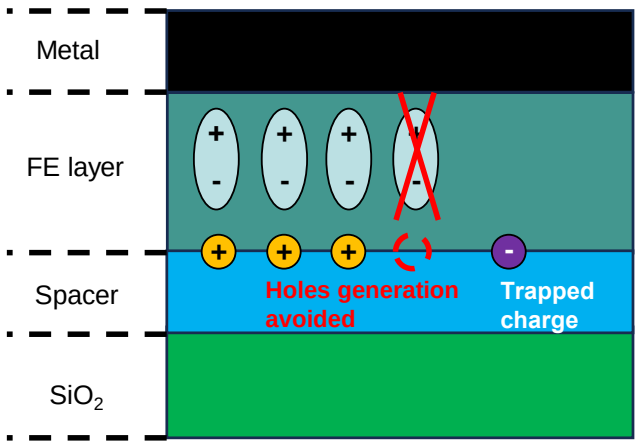
- Low memory window (MW):
  - In HVT state, V_{th} lower trending
  - In LVT state, V_{th} higher trending
  - MW reduce

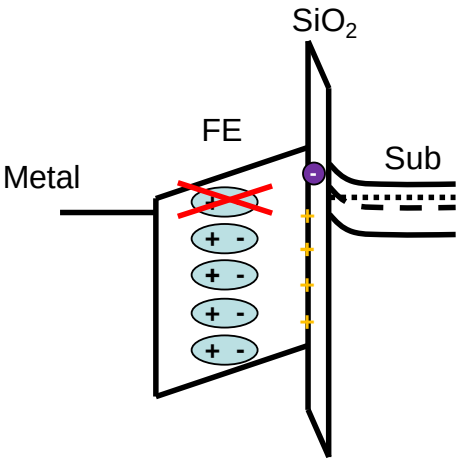
- I_d-V_g curve no shifting:
  - Defective I_d-V_g in the "middle" of defect-free I_d-V_g



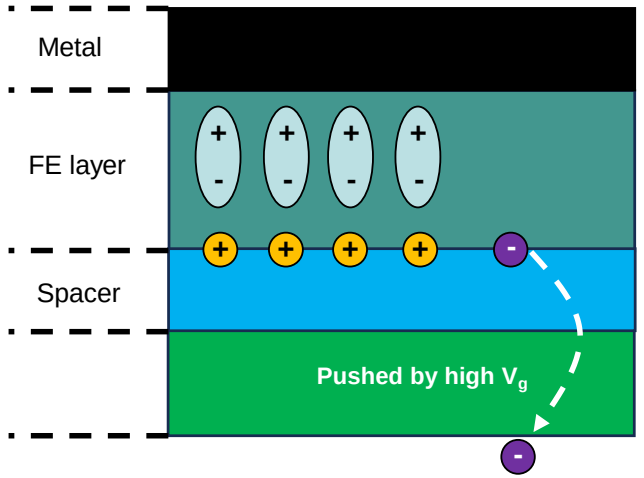
Defect mechanism & characterization

- ACT mechanism:
  - Trap generation
  - Trap capture electrons
  - Partial polarization
  - Memory Window (MW) reduction





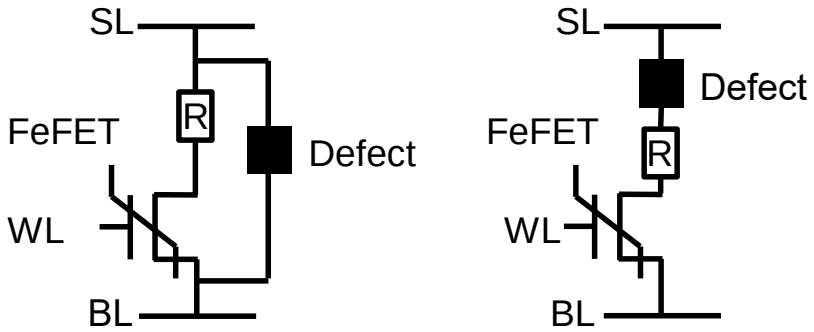
- ACT repair:
  - Possible electron release by a specific V_g (rapidly)
  - Possible electron release with time (i.e. no voltage, seconds)
  - Trap still there → may cause reliability issues



Device-aware test methodology

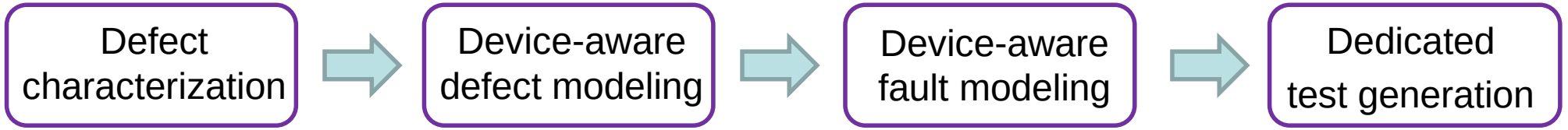
- Conventional memory test process (e.g., for SRAMs and DRAMs):

- Problem: resistor model inaccuracy for unique defect (e.g. ACT)



- Resistance defect model
- Simultaneously increases/reduces R_{cell} for HVT and LVT
- ACT reduces R_{cell} for HVT; increases R_{cell} for LVT

- Device-aware test process



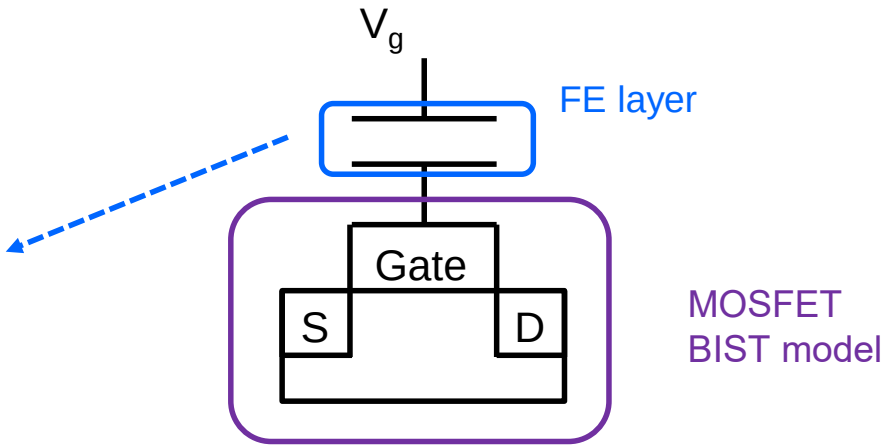
- Implant the defect mechanism into FeFET model
- Design defective FeFET model

Defect modeling

- Defect-free model:

$$P_{\mathrm{FE}} = P_S \cdot \tanh\left(V_{\mathrm{FE}} - \mathrm{dir} \cdot E_C \cdot t_{\mathrm{FE}}\right)$$
$$V_g = V_{FE} + V_{MOS} \qquad (1)$$

P_{FE}	Ferroelectric polarization	P_S	FE layer maximum polarization
V_{FE}	Voltage across the FE layer	dir	Polarization direction
E_C	Coercive field	t_{FE}	FE layer thickness
V_g	Gate voltage	V_{MOS}	Voltage across MOS structure



[N. Kai *et. al.*, VLSI, 2018]

- Low memory window (MW):

$$P_{\mathrm{FE}} = \delta \cdot P_S \cdot \tanh\left(V_{\mathrm{FE}} - \delta \cdot \mathrm{dir} \cdot E_C \cdot t_{\mathrm{FE}}\right)$$

where δ is presented a specific function of V_g:

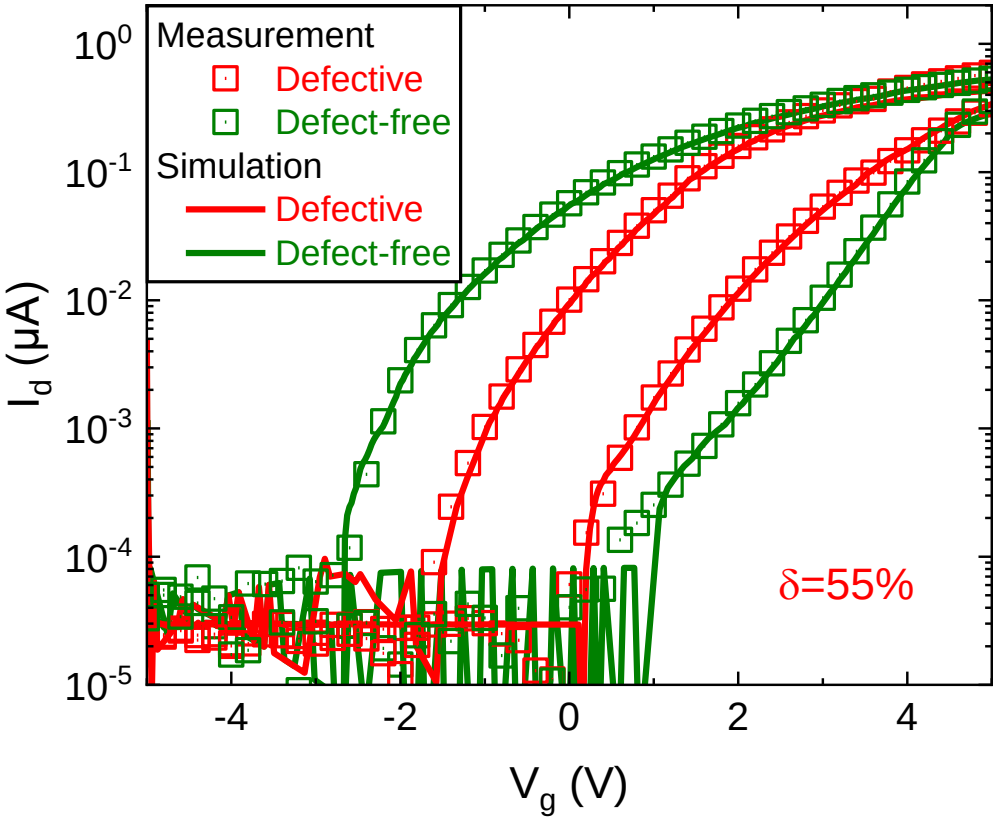
$$\delta = 1 - \delta_0 \cdot g\left(V_g\right), \quad g\left(V_g\right) = \begin{cases} 1 & \left(V_g \geq V_{rp}\right) \\ 0 & \left(V_g < V_{rp}\right) \end{cases}$$

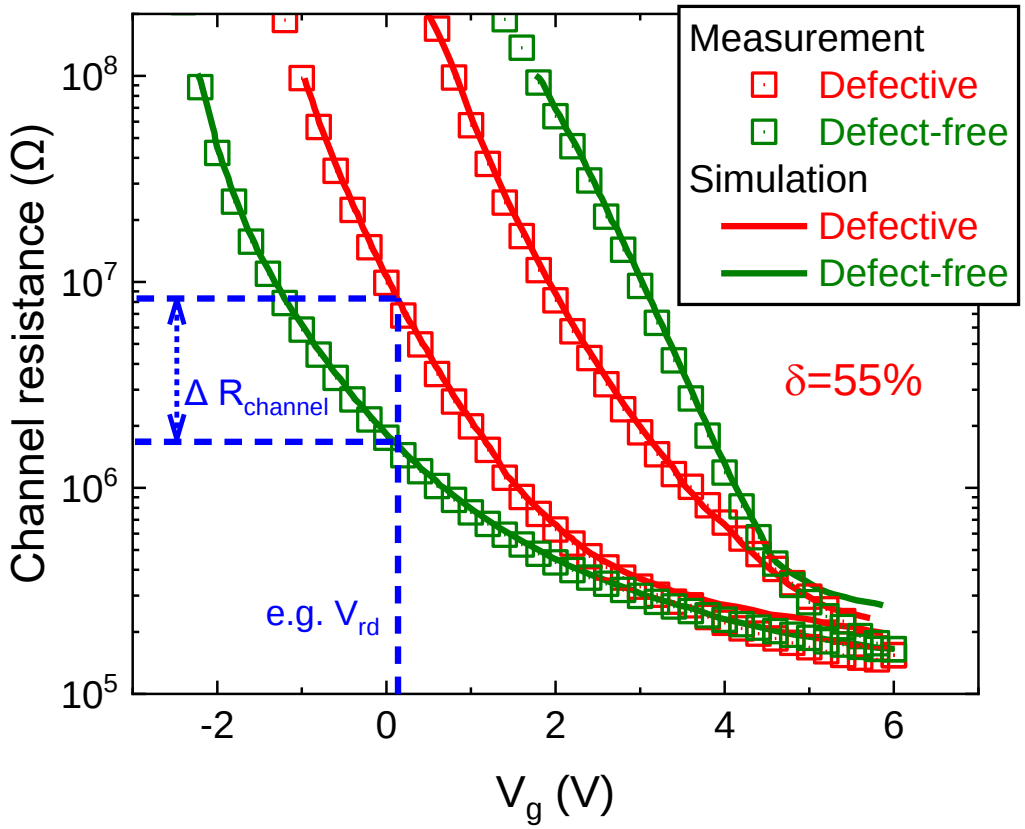
Defect strength → how much polarization is prevented (by trapped electrons)

V_{rp} → repair voltage (in this work, $V_{rp} < 0$)

Defect modeling

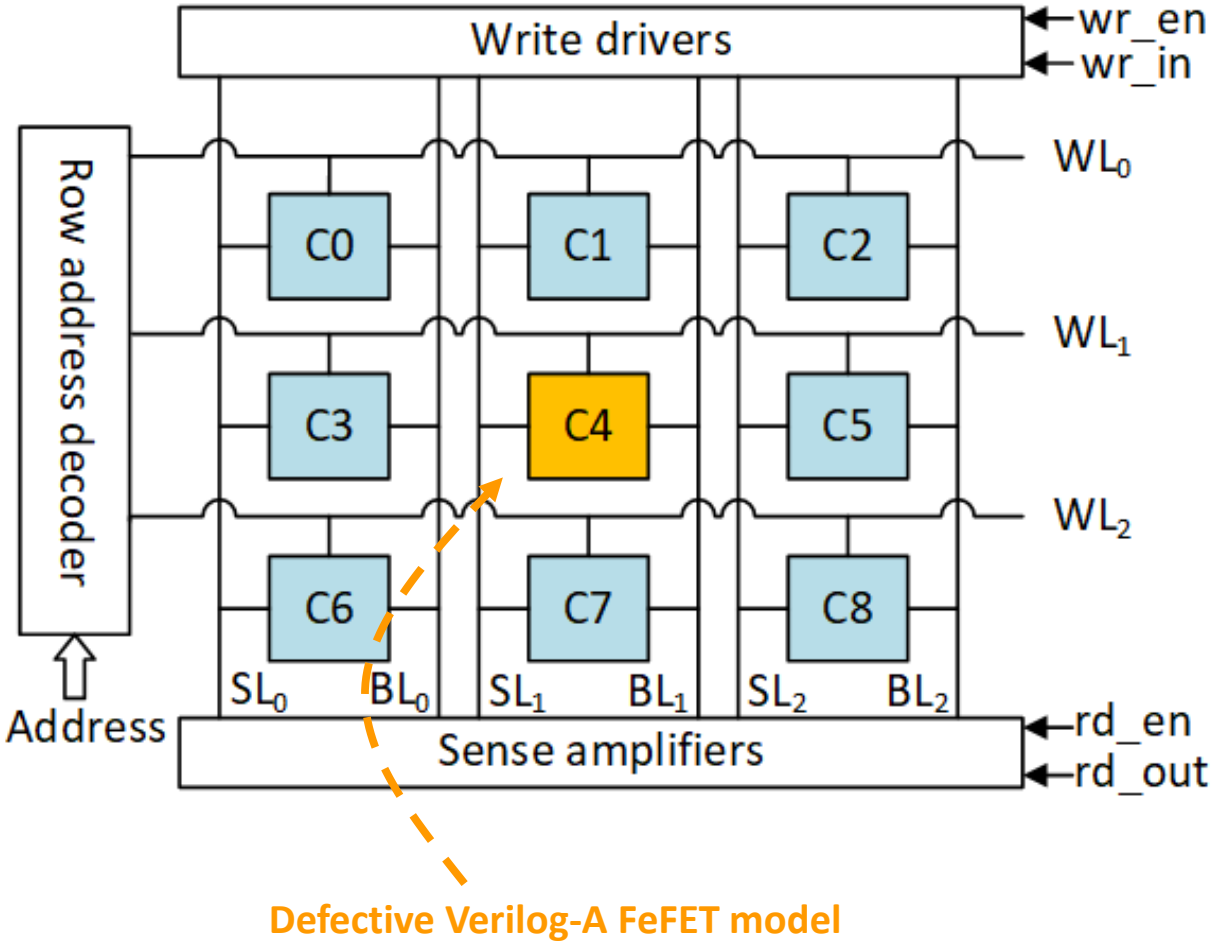
- Fitting process:
  1. Fitting for defect-free devices
  2. Fitting for defective devices by varying δ_0 (defect strength)





Fault modeling

- Simulation set-up:
  - Build 3x3 defect-free FeFET array
  - Variation on MOSFETs and FeFET area
  - MOSFET in SIMC 40 nm
  - Replace C4 with defective model
  - Varying δ_0, simulated operations on C4: S∈{0, 1, 0w1, 1w0, 0w0, 1w1, 0r0, 1r1}
  - Observe C4 faulty behaviors



Fault modeling

- Fault models:
  - The FeFET turns to ('U') state
    - U: undefined state with resistance between defined high 'high' and 'low' resistances
  - Hard-to-Detect (HtD) faults are observed

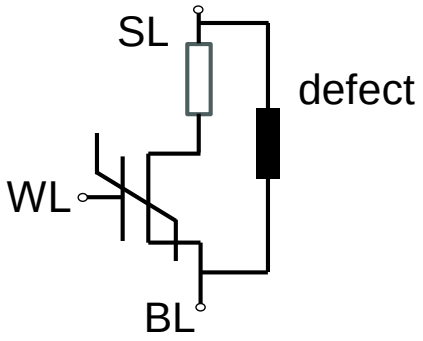
Table 2: Fault models

δ_0	Fault	Fault type	δ_0	Fault	Fault type
[0, 0.3)	Fault-free	\	[0.56, 1]	$< 1r1/U/? >$	HtD
[0.3, 0.56)	$< 0w1/U/- >$	HtD		$< 1/U/- >$	
	$< 1w1/U/- >$			$< 1w0/U/- >$	
	$< 1r1/U/? >$			$< 0w0/U/- >$	
	$< 1/U/- >$			$< 0r0/U/- >$	
[0.56, 1]	$< 0w1/U/- >$	HtD		$< 0/U/- >$	
	$< 1w1/U/- >$				

Fault modeling

- Comparison with fault modeling by conventional/device-aware method:

Conventional defect modeling by linear resistor



Conventional fault modeling

<0r0/0/?>
<0r0/0/1>

Device-aware fault modeling

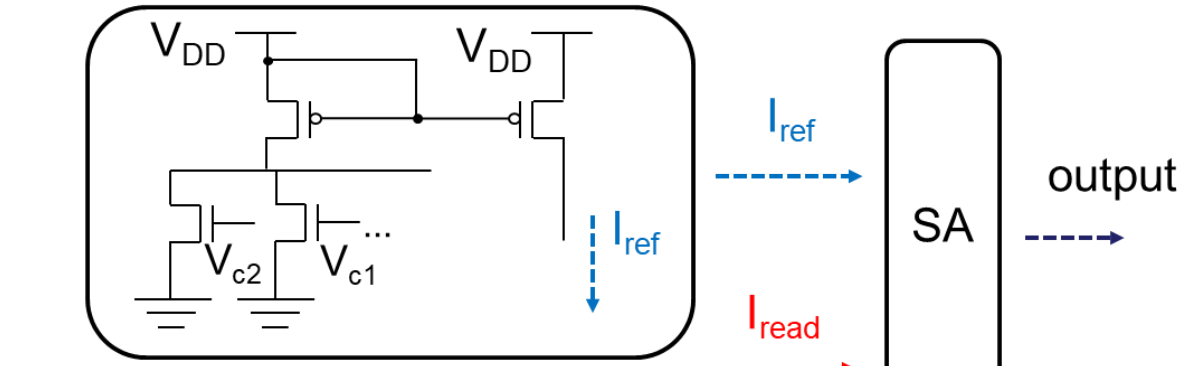
<0w1/U/-> <1w0/U/->
<1w1/U/-> <0w0/U/->
<1r1/U/?> <0r0/U/?>
<1/U/-> <0/U/->

- Conventional fault modeling results in incomplete fault maps
- Test solutions derived from incomplete fault maps cause high escapes

Test solutions

- March test:
  - Targeting fault <1r1/U/?>
  - {⇳ (w1); ⇳ (r1)} → high escapes due to 'U'
  - Repeating the march algorithm increases the defect capturing rate, also increasing test time

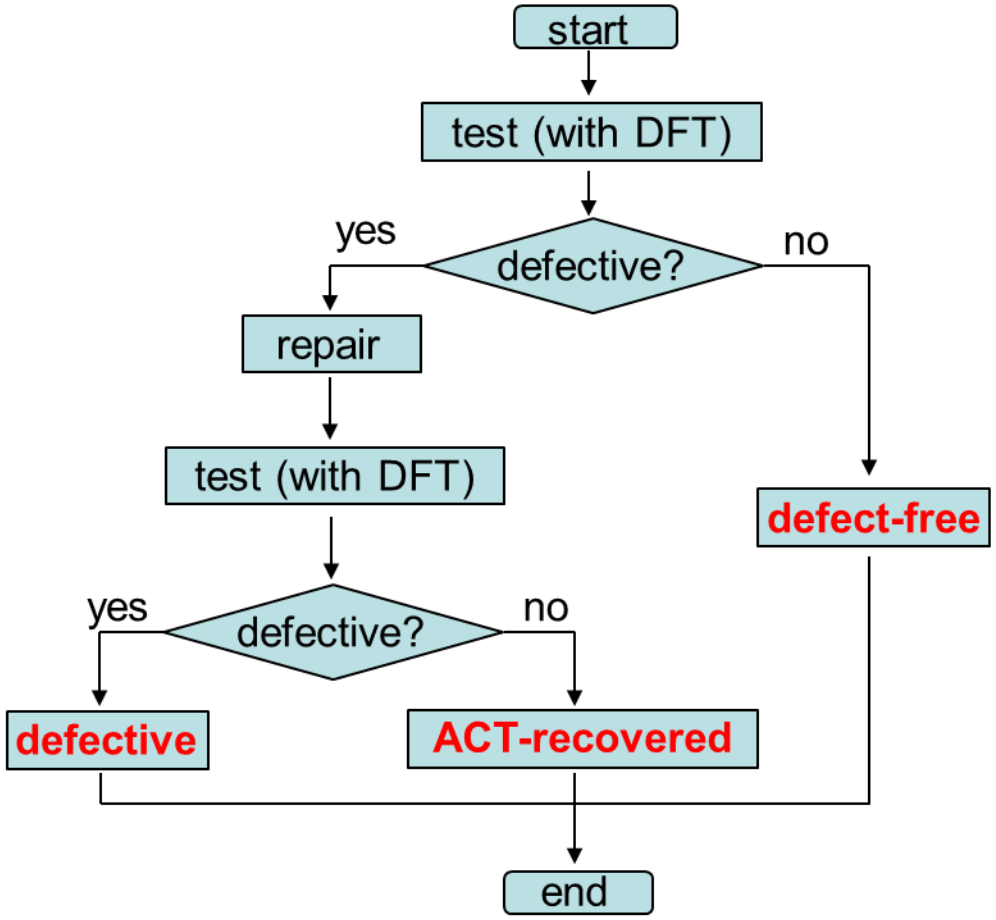
- Design-for-Test:
  - Trimming circuit to directly extract the FeFET S/D resistance
  - Detect 'U' state



trimming-based I_{ref} generator

Test solutions

- Flow chart of diagnosis and repairing:
  - Test by DfT
  - Repair by high V_g → if repairable, the defect is diagnosed as ACT



Comparison FeFET defects

Defect	Mechanism	Defective FeFET performance	Related FeFET structure
SAP Thapar, et al. *"Analysis and Characterization of Defects in FeFETs."* 2023 ITC	Unchanged domains caused by Crystallization imperfection	Increased LVT decreased HVT reduced memory window **unrepairable**	FE layer
ACT This work	Trap charge **related** with FE layer	Increased LVT decreased HVT reduced memory window **repairable**	FE layer
TVS (On Going)	Trap charge **unrelated** with FE layer	Simultaneous changes in LVT and HVT Unchanged memory window	Oxide layer

[1] Thapar, et al. *"Analysis and Characterization of Defects in FeFETs."* 2023 ITC
[2] Wang, et al. *"Defects, Fault Modeling, and Test Development Framework for FeFETs."* 2024 ITC
[3] Ichihara, et al. *"Accurate picture of cycling degradation in HfO 2-FeFET based on charge trapping dynamics revealed by fast charge centroid analysis."* 2021 IEDM

Conclusion

- Challenges in FeFET testing
  - Specific mechanism in FeFET
  - Write/read-based tests show high escape in detecting unique defects
- Solution
  - Device-aware tests
  - Design defective FeFET model
  - Complete fault model
  - Dedicated test solution
- Future work
  - Device-aware tests for other FeFET application (e.g., CIM)