

# **ML-Assisted RFIC Design Enablement: The New Frontier of AI for EDA**

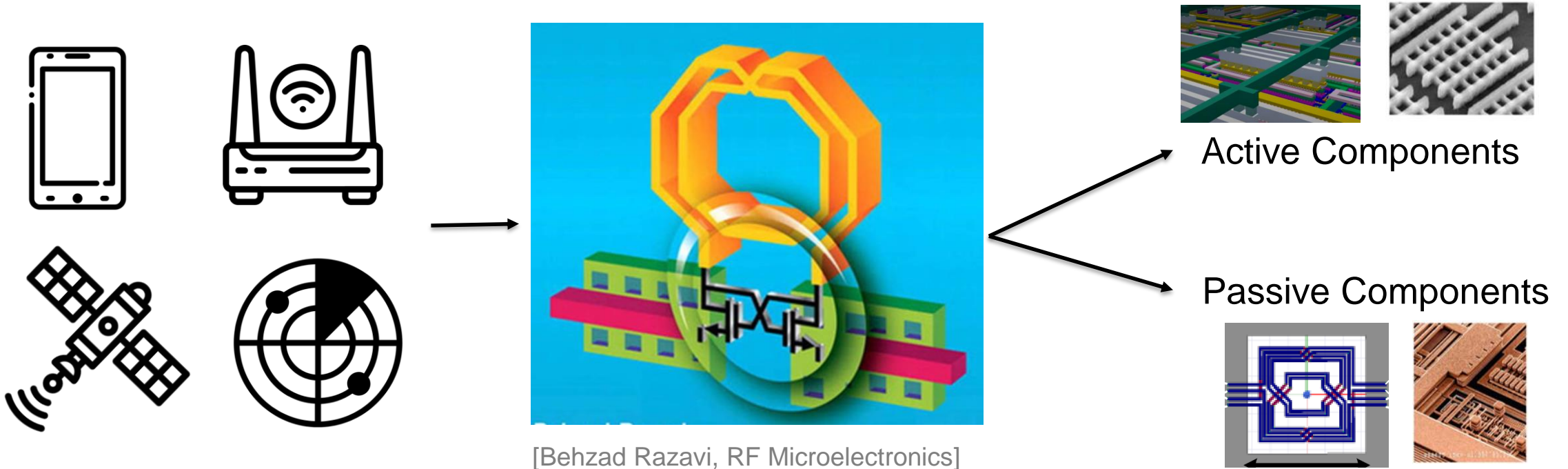
Hyunsu Chae<sup>1</sup>, Song Hang Chai<sup>1</sup>, Taiyun Chi<sup>2</sup>, Sensen Li<sup>1</sup>, and David Z. Pan<sup>1</sup>

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<sup>2</sup>Rice University, Houston, Texas, USA

# RFIC (Radio Frequency Integrated Circuit)

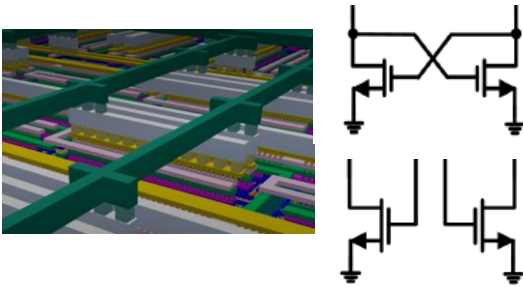
- ♦ RFIC components are fundamental in wireless systems
- ♦ RFIC = active + passive components



# RFIC = Active + Passive

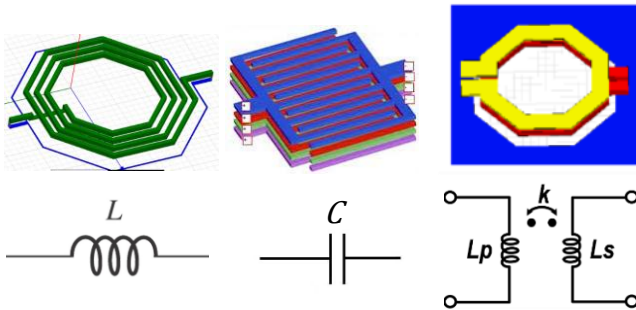
- ♦ Active-Passive interactions influence the overall RFIC performance

## Active Components



- ♦ Provides the essential power and gain
- ♦ Signal generation, amplification,...

## Passive Components

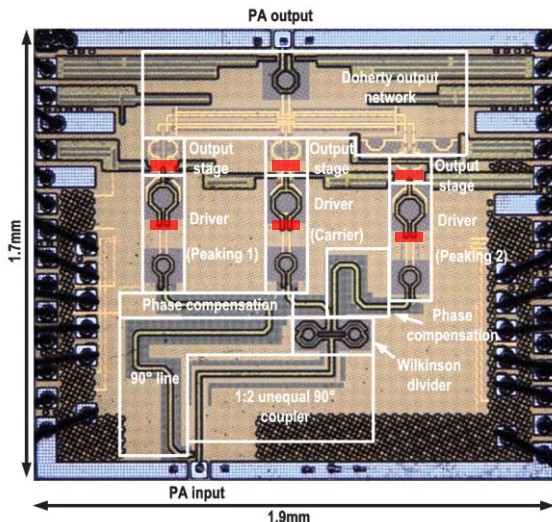


- ♦ Define the frequency response
- ♦ Impedance matching, filtering, phase shifting, stabilization, harmonic manipulation,...

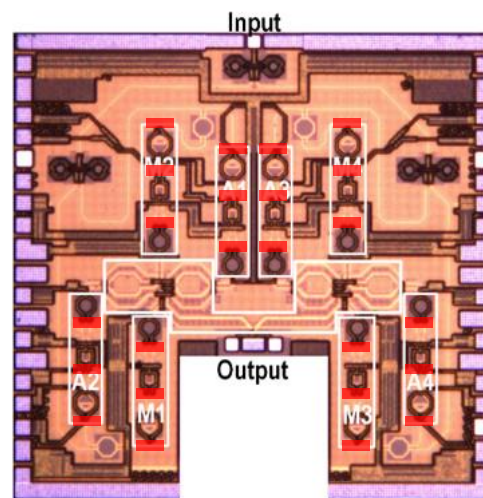
- ♦ The majority of RFIC design efforts are focused on **passive design and optimization**

# RFIC Passive Design Challenges

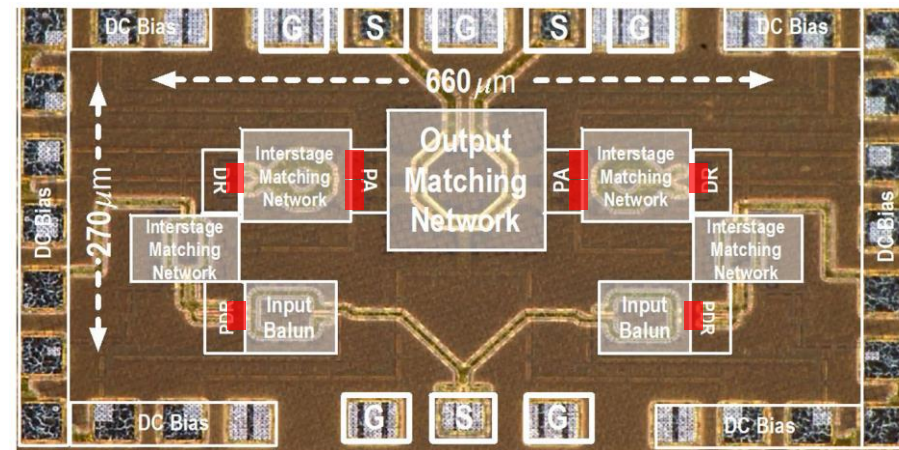
- ◆ Need to balance different design objectives across frequencies
  - › Minimize loss, maximize bandwidth, address impedance transformation
- ◆ Follows active component design and can limit their performance
- ◆ Occupy most of chip area
  - › e.g., the passive component in an RF power amplifier (PA) occupies over 80% of the core chip area



[Zhang+, JSSC'23]



[Zhang+, TMTT'23]

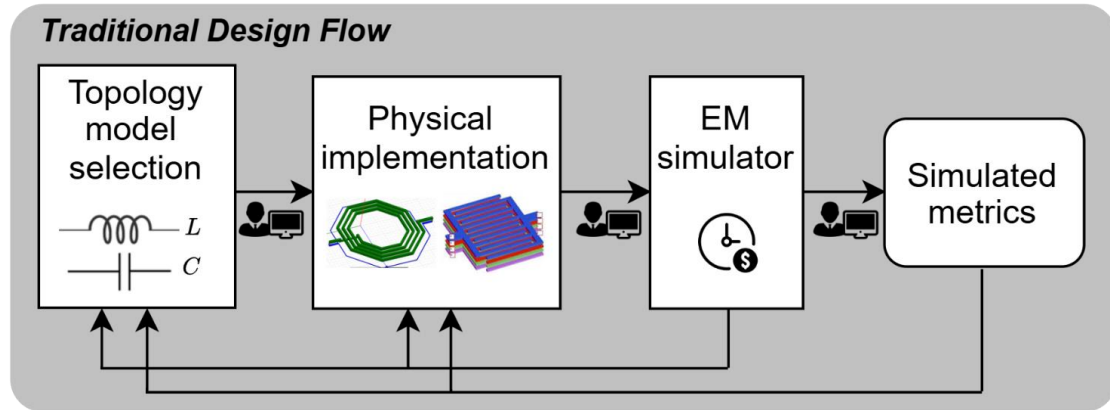


[Li+, JSSC'24]

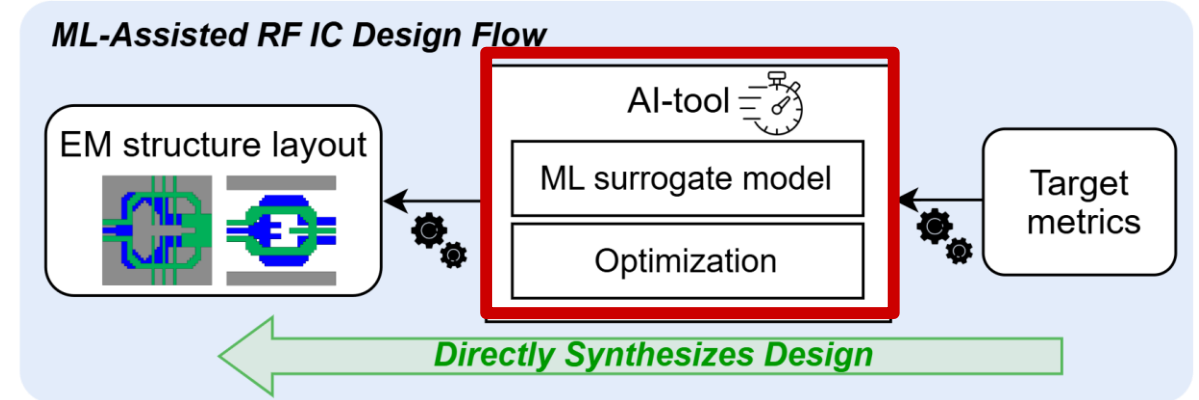
■ Actives



# RFIC Passive Design Flow

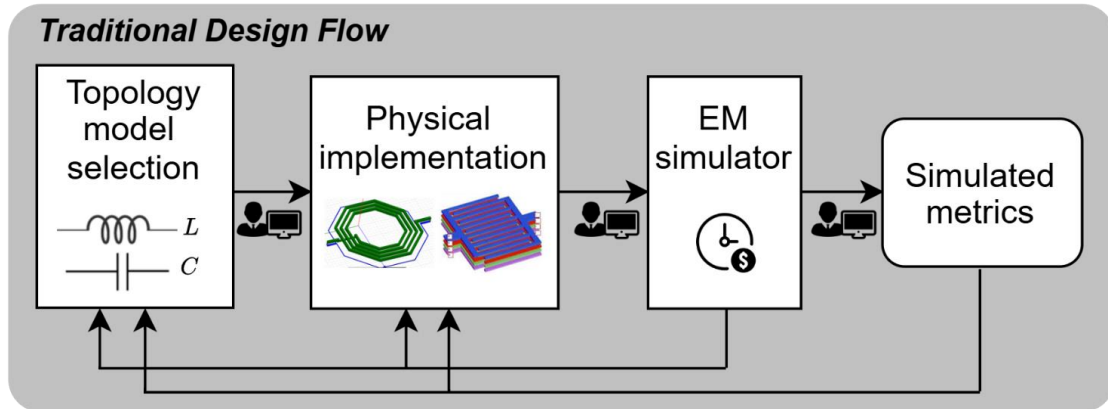


- ☹️ Computationally expensive simulations
- ☹️ Iterative
- ☹️ Heuristically-constrained
- ☹️ High entry barriers for new designers

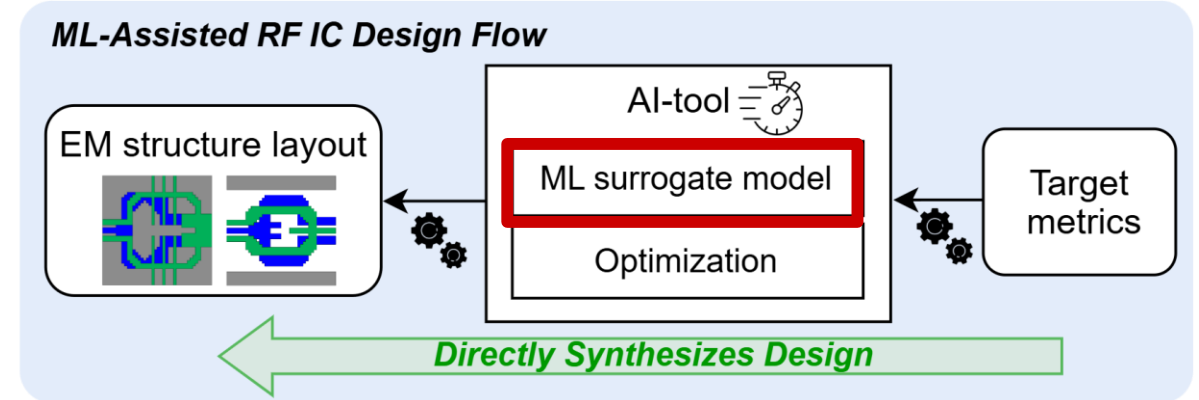


- 😊 Fast evaluation utilizing ML models
- 😊 Automated
- 😊 Non-intuitive and beyond human
- 😊 Lowered entry barriers for new designers

# RFIC Passive Design Flow



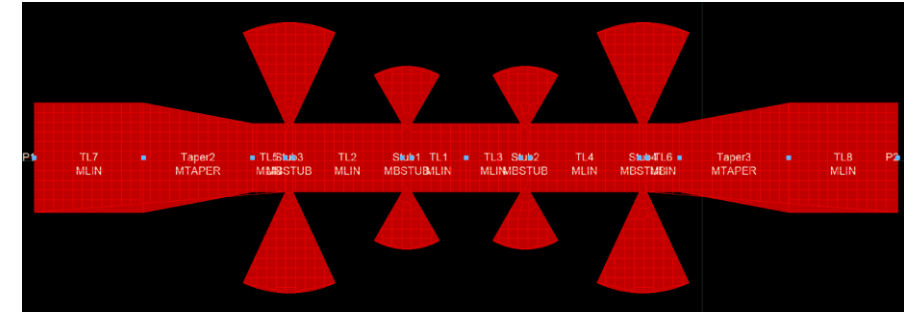
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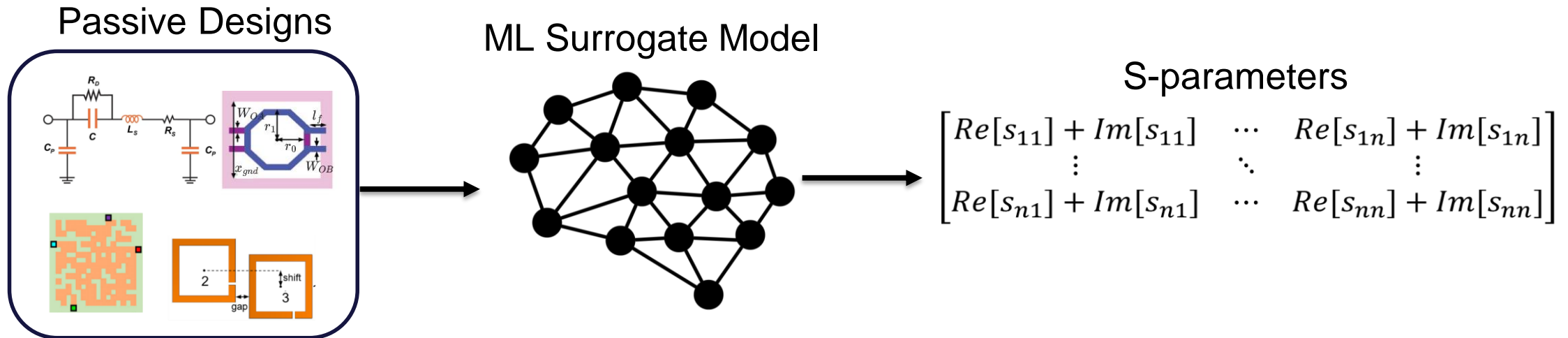
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# ML Surrogate Modeling

- EM simulation is the major bottleneck of RF manual design
  - Solves Maxwell's equations with 3D mesh

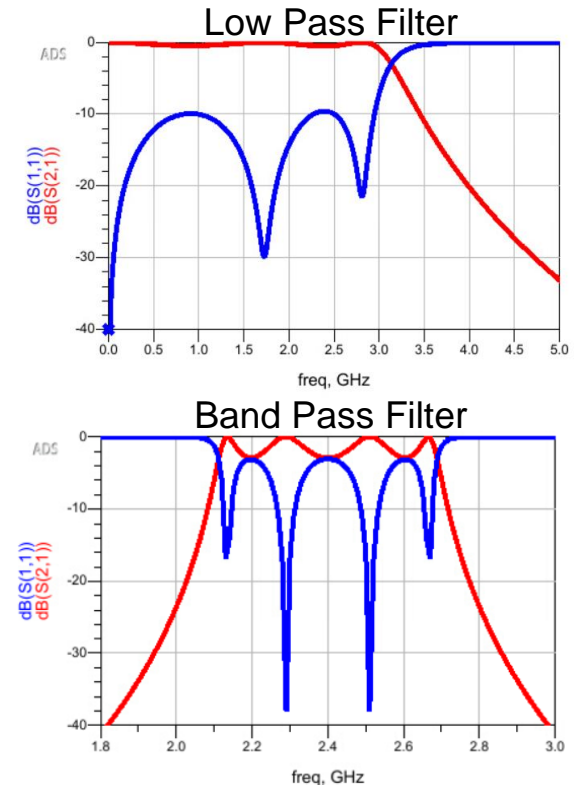


- Replace EM simulation with ML surrogate models for faster performance evaluation



# ML Surrogate Modeling

- ♦ S-parameters (Scattering parameters)
  - › Describes the electrical behavior of a multi-port network
    - Characterizes the voltage (power) being transferred between ports
  - › Matrix of complex numbers over frequency
  - › Can be converted to Z, Y-parameters or other metrics to analyze various characteristics
- ♦ Limited research on ML surrogate modeling for RF passive designs..
- ♦ Include reviews of related works in package design



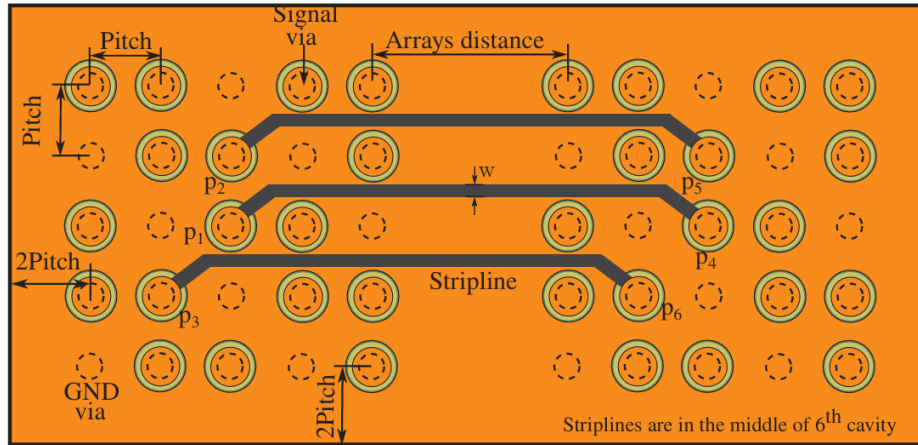


# ML Surrogate Modeling

- ♦ Categorize based on different representations
- ♦ Tabular (or Template) Based ML Modeling
  - › EM structures are represented using predefined templates and parameter sets (physical dimensions, material properties,...)
- ♦ Graph Based ML Modeling
  - › Metal traces in the EM structures are segmented to form graph representations
- ♦ Image Based ML Modeling
  - › RF passive layouts are converted into layers of pixelated images representing metal or non-metal regions

# Tabular (or Template) Based ML Modeling

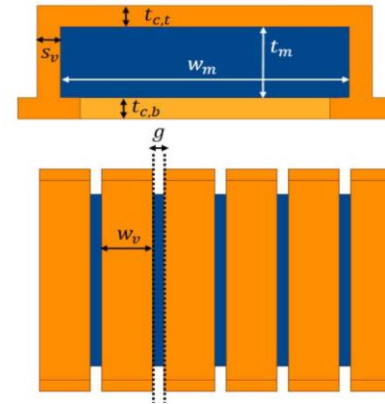
[Sánchez-Masís+, LAMC'23]



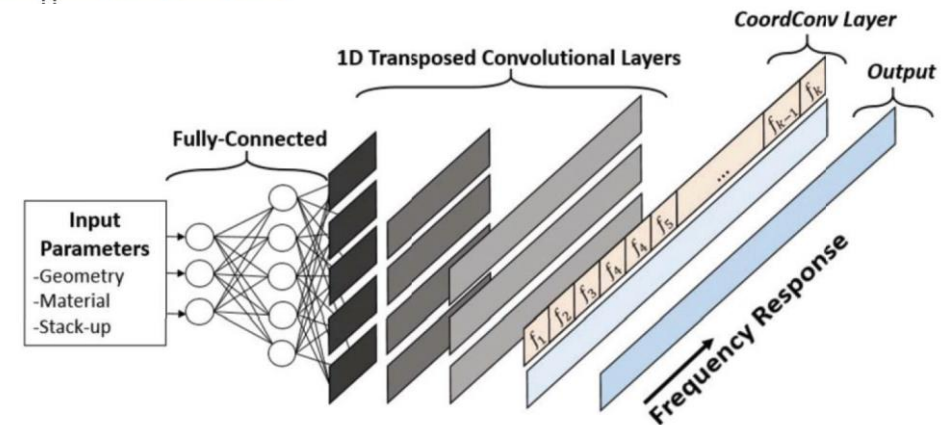
cavity height (h)	9±3mils	plate thickness (t)	{ 1, 2 }mils
pitch	40±20mils	stripline width (w)	5.5± 1.5mils
pad radius (pr)	9.25±2.75mils	distance between arrays (d)	10.5±9.5cm
antipad radius (ar)	14.75±4.25mils	relative permittivity ( $\epsilon_r$ )	4.1 ±0.3
loss tangent ( $\delta$ )	{ 0.002, 0.02, 0.2 }		

- Parameterizes PCB link between vias
- Multi-layer perceptron (MLP) model for a frequency point

[Torun+, ICCAD'19]



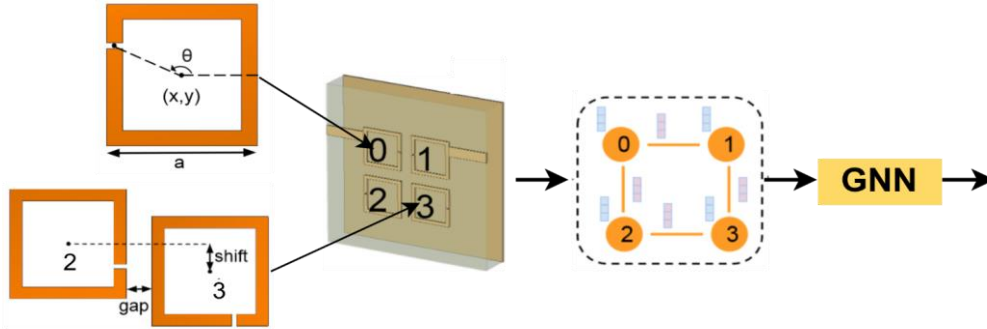
Parameter		Unit	Min	Max
Gap between windings	g	mil	2	20
Number of windings	N		3	13
Size of via	$s_v$	$\mu\text{m}$	50	103
Copper Trace Width	$w_c$	mil	2	20
Copper Thickness Bottom	$t_{c,b}$	$\mu\text{m}$	35	170
Copper Thickness Top	$t_{c,t}$	$\mu\text{m}$	35	170
Magnetic Core Thickness	$t_d$	$\mu\text{m}$	50	650
Magnetic Core Width	$w_d$	$\mu\text{m}$	50	350



- Parameterizes solenoidal inductor
- Transposed-CNN model for across multiple frequencies

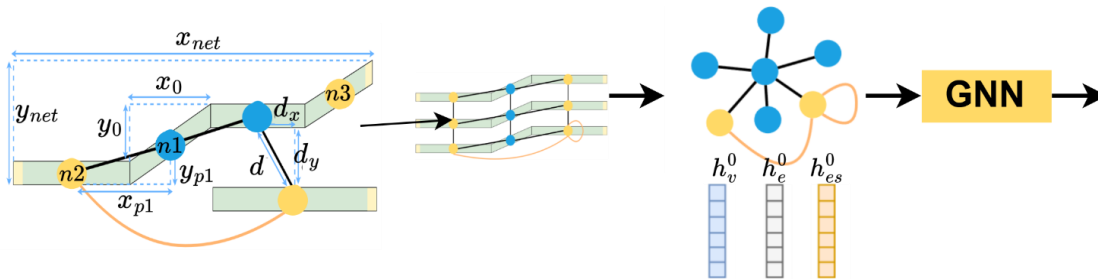
# Graph Based ML Modeling

[Zhang+, ICML'19]



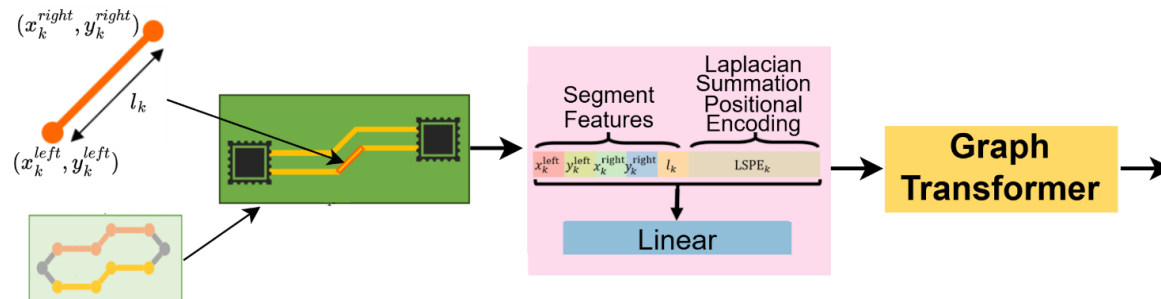
- Represents  $N$ -resonator filter as graph
  - Nodes : resonators (center coordinates, etc. )
  - Edges: electromagnetic interaction between resonators
- GNN model

[Liu+, TCPMT'24]



- Represents PCB interconnect (UCIe) as graph
  - Nodes : each segmentation
  - Edges: connection between segmentations
- GNN model

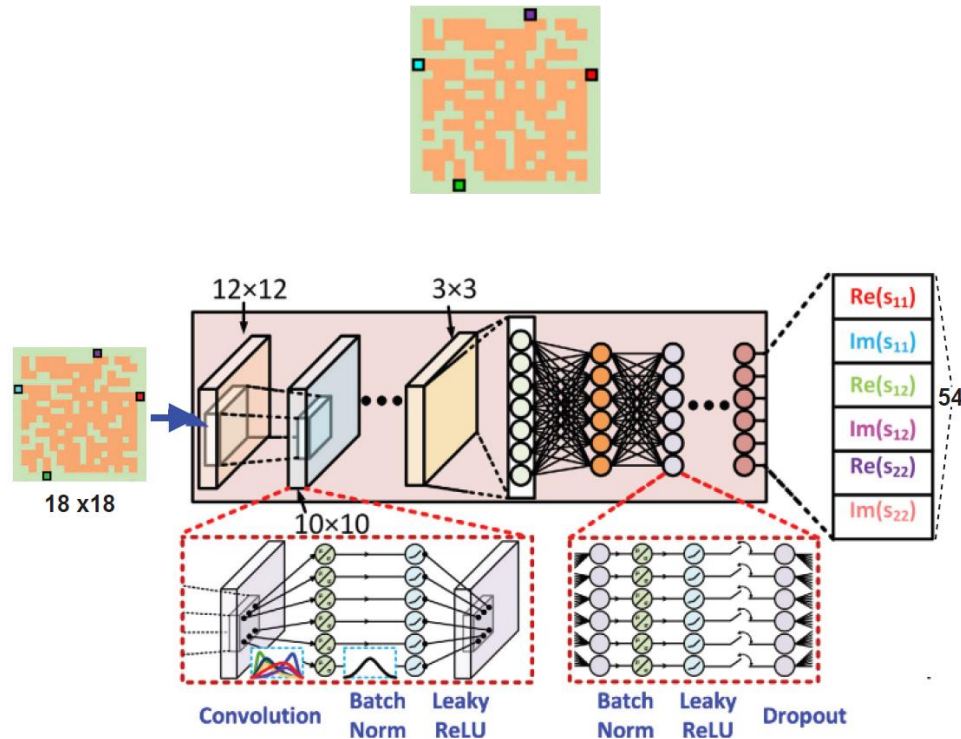
[Kim+, DAC'24 ]



- Represents PCB interconnect as graph
- Graph Transformer model

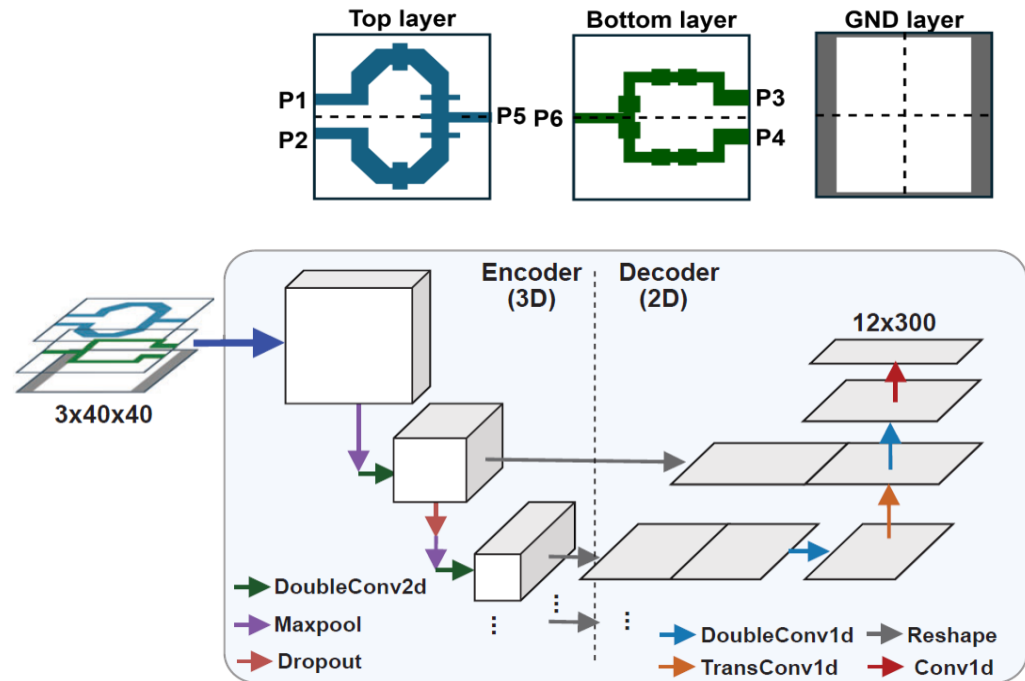
# Image Based ML Modeling

[Karahan+, JSSC'23]



- Single-layer layout (pixelated to 18x18) for matching network
- Deep-CNN model

[Chae+, ICCAD'24]



- Multi-layer layout (pixelated to 3x40x40) for generic impedance transformation network
- 3D-to-2D UNet model

# ML Modeling: Challenges

- ♦ **Challenge:** Representing solution space
  - › Tabular: Requires a predefined fixed set of template parameters
  - › Graph: Faces scalability issues as the trace segmentations increases
  - › Image: Demands significant computational resources
  - › Performance comparison is difficult
- ♦ **Challenge:** Quality and quantity of the dataset
  - › Limited open datasets: NDA constraints from semiconductor foundries limits open-source RFIC datasets
  - › Costly dataset generation: Training datasets rely on expensive and time-consuming EM simulations

# ML Modeling: Future Directions

- ◆ **Current Key Contributions:** Physics-augmented ML modeling

- › Reduce data dependency by integrating physical knowledge with ML

[Torun+, TMTT'20] [Chae+, ICCAD'24]

- › Causality Enforcement Layer :

$$\text{Im}[H(f)] = -\mathcal{H}\{\text{Re}[(H(f))]\}$$

- › Passivity Enforcement Layer:

$$\sum_N S_{mn}^2 \leq 1$$

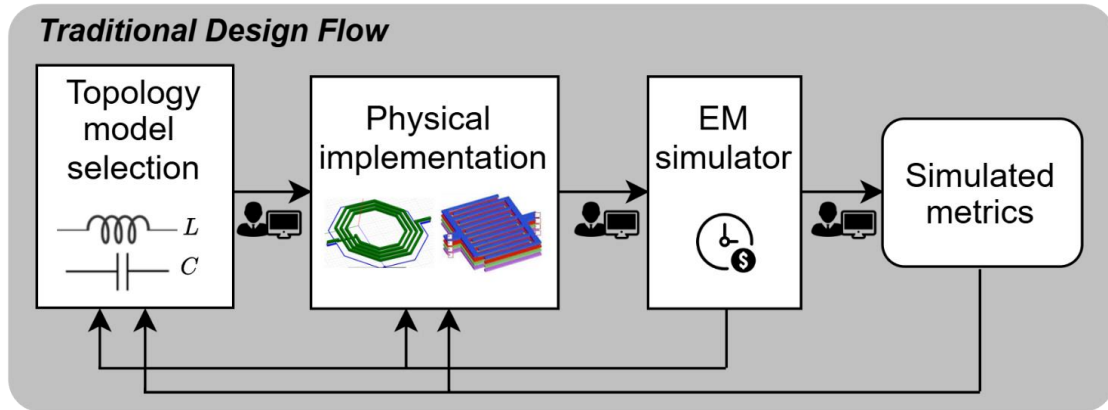
- › Kramer-Kronig Compensation Layer:  $\text{Im}[S_k]' = \text{Im}[S_k] + \text{linear}_k\{\text{Re}[S_k]\}$

- ◆ **Future Directions:**

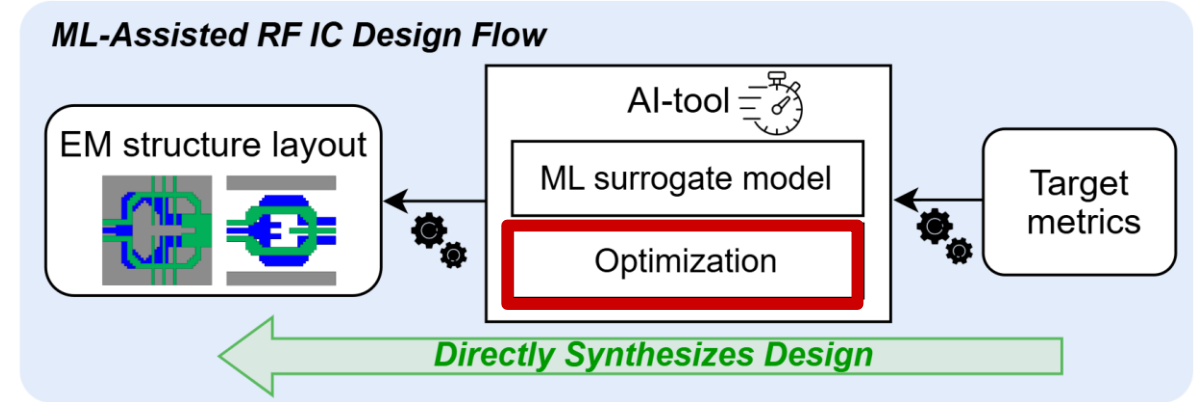
- › Further exploration of methods to embed physical law into ML model
- › Use of fast solvers with optimal complexity and transfer learning for technology-agnostic applications
- › Development of open-source datasets



# RFIC Passive Design Flow



- ☹️ Computationally expensive simulations
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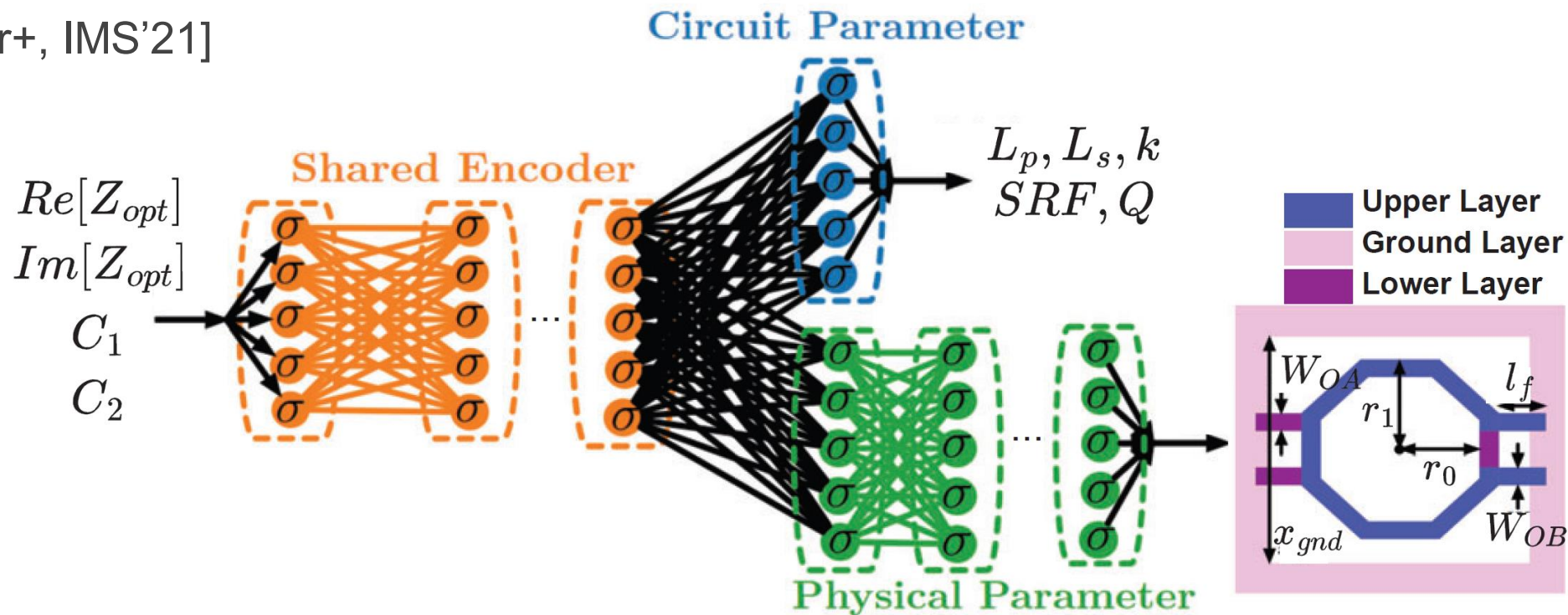
# Inverse Design Optimization

- ♦ Quickly synthesize RF passive design to satisfy the given target performance
- ♦ Tabular Design Space Optimization
- ♦ Pixelated Design Space Optimization
- ♦ Hybrid (template and pixelated) Design Space Optimization

# Tabular Design Space Optimization

- ♦ Directly train ML model to predict the design parameters
  - » ML model is trained to do the “inverse” design
  - » Requires a strategy to resolve multi-modal output problem

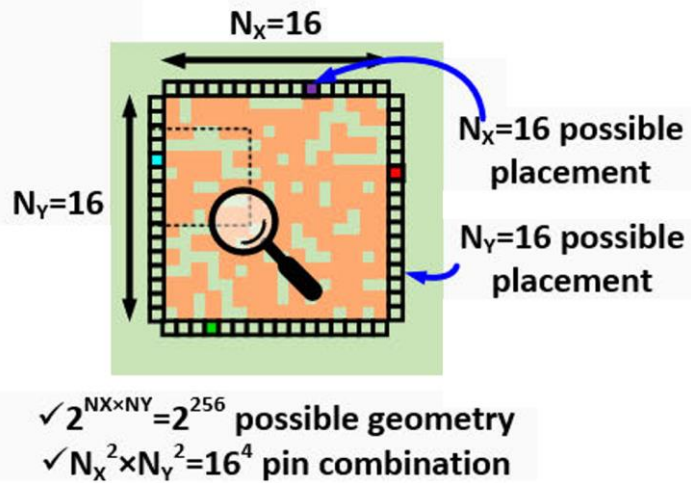
[Er+, IMS'21]



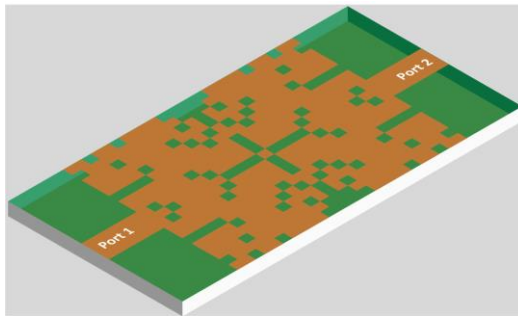
# Pixelated Design Space Optimization

- The entire design area is pixelated into bitmap of metal or non-metal

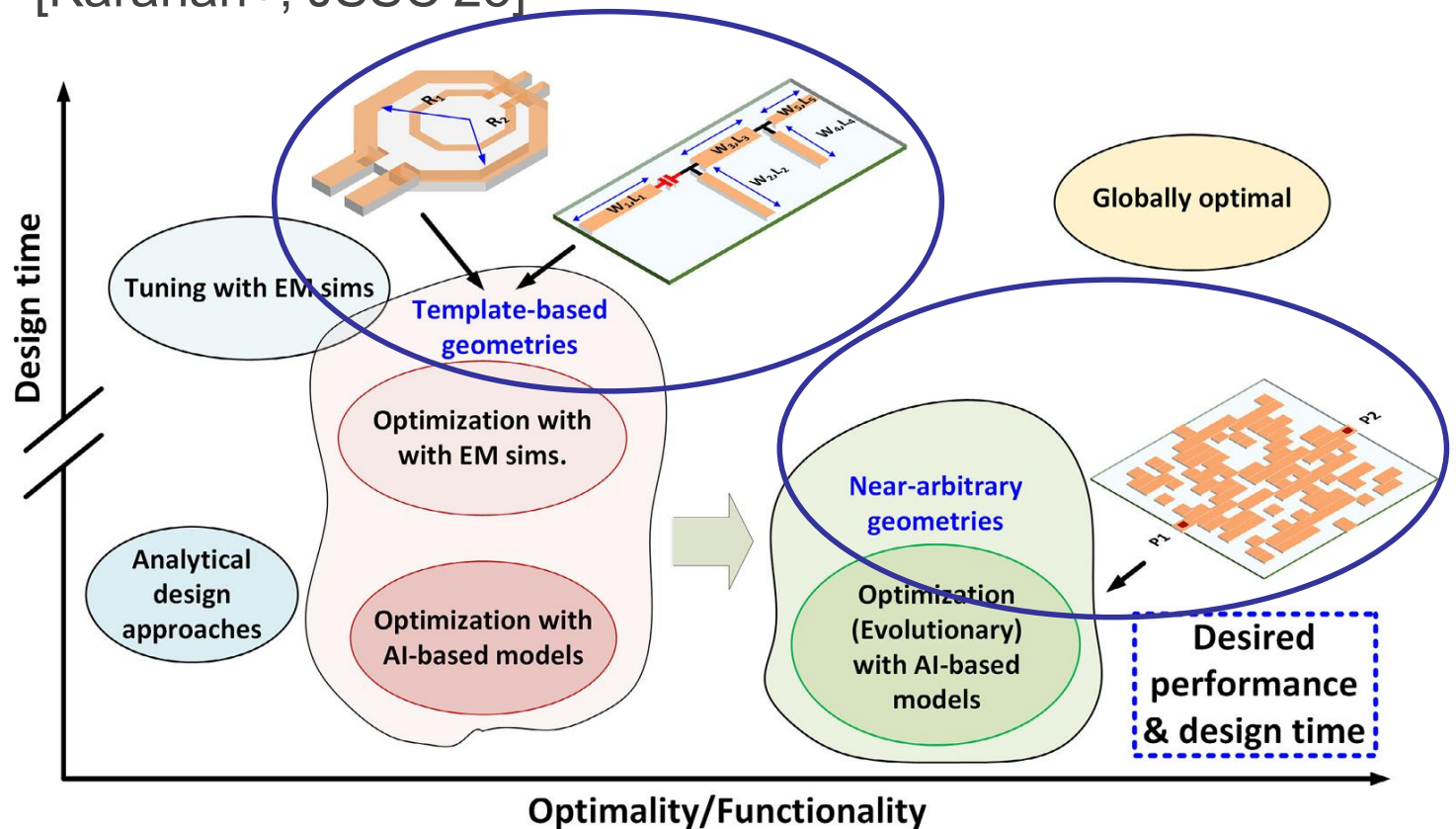
[Karahan+, JSSC'23]



[Lee+, NEWCAS'23]



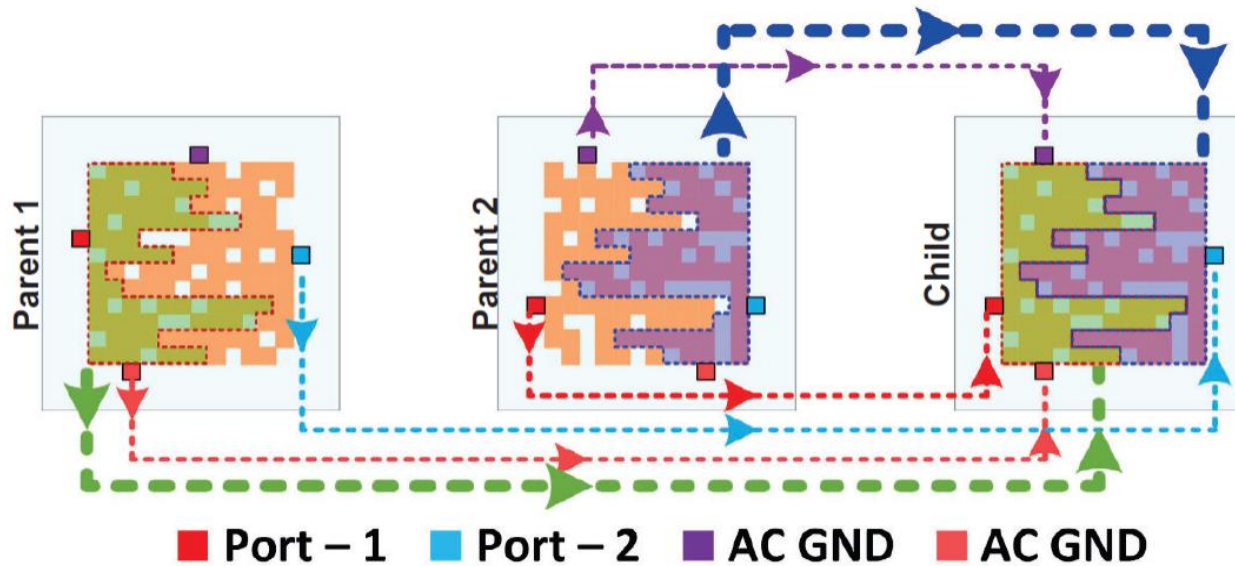
[Karahan+, JSSC'23]



# Pixelated Design Space Optimization

## ♦ Genetic Algorithm-based Optimization

[Karahan+, JSSC'23]



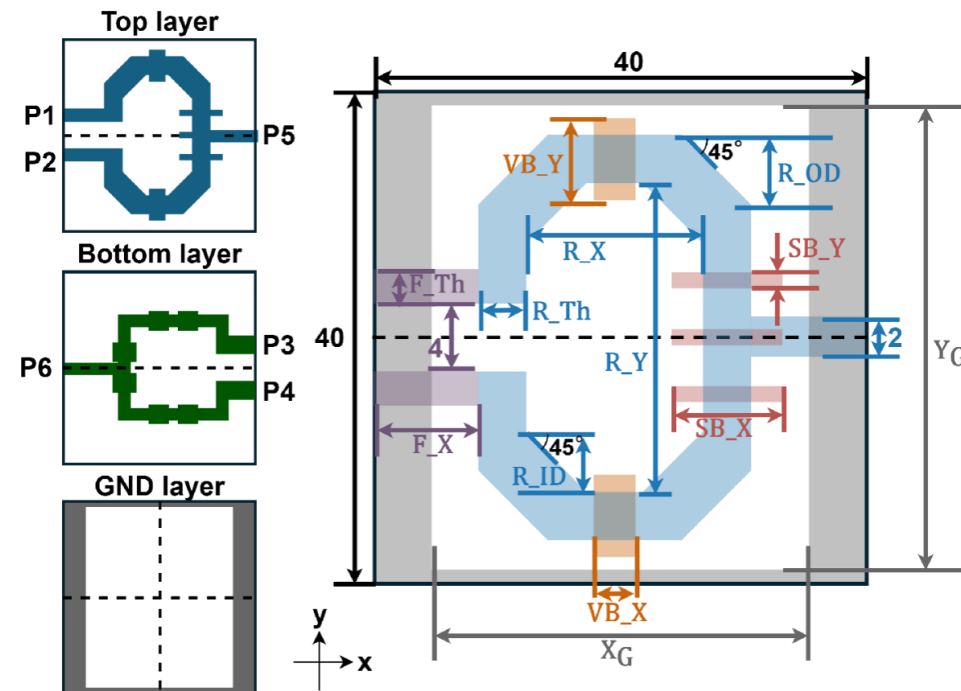
- › Two best performing designs are selected from random set of designs
- › Offsprings are reconstructed from each parent through a random cut line
- › Random mutations on pixels are applied



# Hybrid Design Space Optimization

- The design space is represented as the combination of conventional and pixelated approach

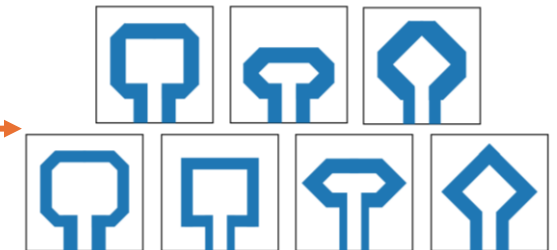
[Chae+, ICCAD'24]



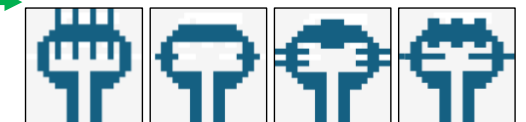
28 parameters

	$x$	Description	$[x_L, x_U]$	$dx$
GND layer	XG	Ground cut x	[0, 40]	2
	YG	Ground cut y	[0, 40]	2
Top/ Bottom layer	F_Th	Feedline thickness	[2, 5]	1
	F_X	Feedline length	[2, 30]	1
	R_Th	Ring thickness	[2, 8]	1
	R_X	Ring inner boundary x	[4, 32]	1
	R_Y	Ring inner boundary y	[6, 36]	2
	R_ID	Ring inner diagonal	[0, 14]	1
	R_OD	Ring outer diagonal	[0, 15]	1
	VB_N	Vertical bump number		
	VB_X	Vertical bump x		
	VB_Y	Vertical bump y		
	SB_N	Side bump number		
	SB_X	Side bump x		
	SB_Y	Side bump y		

Diverse ring shapes



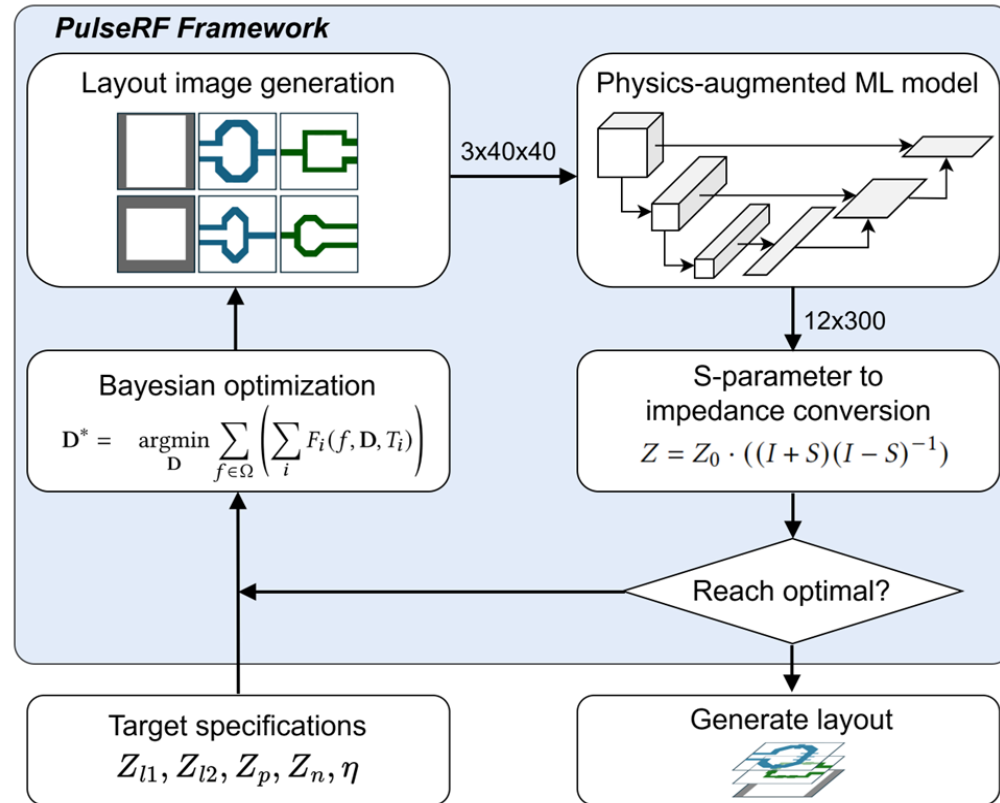
Local deformations







# Hybrid Design Space Optimization

## Bayesian Optimization



[Chae+, ICCAD'24]

- › Select new designs through probabilistic decision-making
- › Optimize for ring-structure parameters
- › Local deformations are treated as noise

		Manual	PulseRF
Design Target		$Z_p = Z_n = 100 + j0 @ 140\text{GHz}$	
Results	Design Time	a few hours	6 mins
	Layout		
	Synthesized Results	$Z_p = Z_n = 5.60 + j35.92$ $\eta = 0.65$	$Z_p = Z_n = 87.72 + j0.20$ $\eta = 0.89$

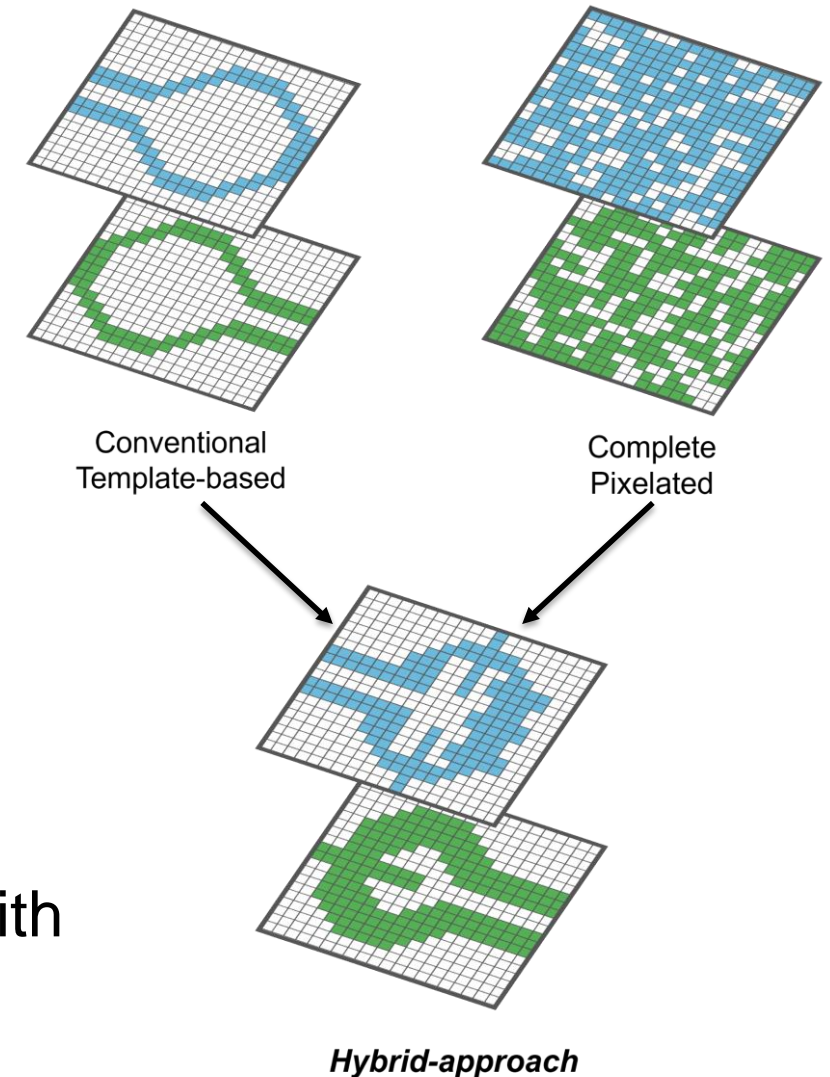
Non-intuitive structure can achieve beyond template-based design

# Inverse Design: Challenges

- ♦ **Challenge:** Design space definition
  - › Conventional tabular: highly restricted
  - › Complete pixelated: randomly scattered pixels and isolated shapes lead to redundant design performance

→ Need to balance between exploitation and exploration of the design space

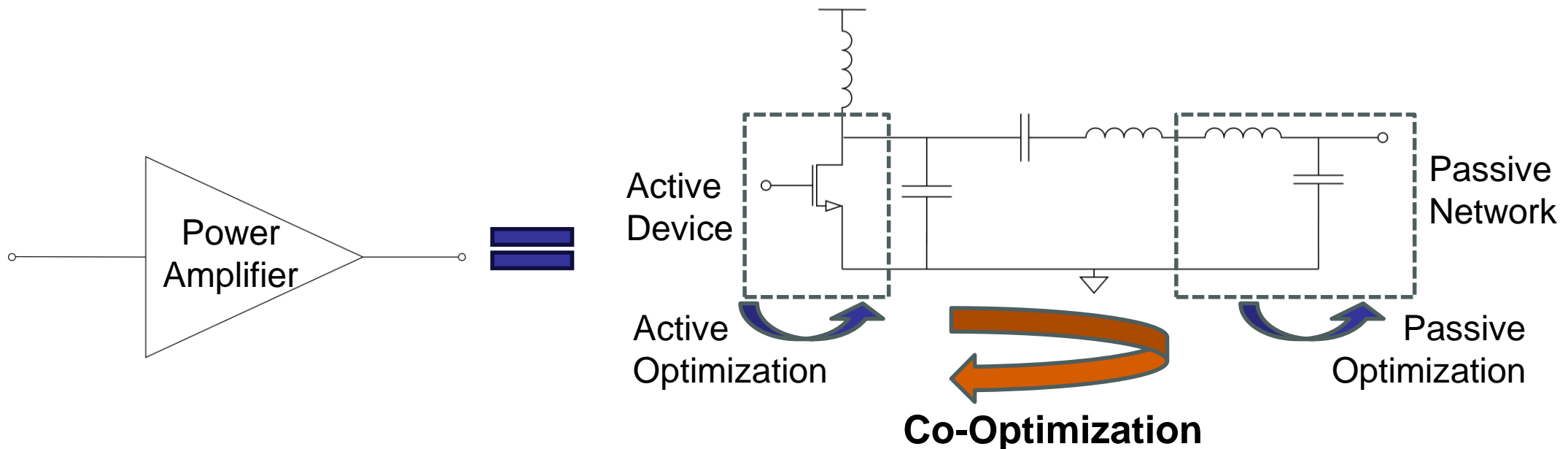
- ♦ **Solution:**
  - › Hybrid-approach of flexible template-based with local deformations



# Inverse Design: Future Direction

## ♦ Future Directions:

- Incorporate RFIC domain knowledge to design space definition to ensure meaningful performance outcomes
- Introduce non-intuitive features to enhance flexibility
- Shift towards active-passive co-optimization, integrating both components into an end-to-end AI-assisted design flow



# Conclusion

- ♦ We have just scratched the surface of AI for RF IC design automation
- ♦ Won't replace experienced designers, but will replace “mundane” jobs, improve productivity, democratize RF IC designs (workforce development)
- ♦ A lot of future research opportunities: incorporating physic laws, transfer learning, technology-agnostic applications, explainability, optimality, active-passive co-optimization,...

# NSTC 1<sup>st</sup> Jump Start R&D Program: AIDRFIC



- ♦ **UT Austin led project “GENIE-RFIC: Generative ENgine for Intelligent and Expedited RFIC Design” selected**
- ♦ **We are hiring PhD students and postdocs (please contact Prof. David Pan)**

## NATCAST ANNOUNCES ANTICIPATED AWARDEES, APPROXIMATELY \$30 MILLION INVESTMENT THROUGH FIRST NSTC R&D JUMP START PROJECT

October 18, 2024

*AIDRFIC awards will propel AI-driven RFIC design innovation, enhance U.S. global competitiveness in semiconductor R&D*

WASHINGTON, D.C., October 18, 2024 – Natcast, the purpose-built, non-profit entity designated by the Department of Commerce to operate the National Semiconductor Technology Center (NSTC) established by the CHIPS and Science Act of the U.S. government, today announced three anticipated awardees and approximately \$30 million in funding through the Artificial Intelligence Driven RF Integrated Circuit Design Enablement (AIDRFIC) program, the first **NSTC R&D Jump Start** project. The anticipated awards will revolutionize RFIC design by integrating artificial intelligence (AI) and machine learning (ML) technologies, addressing one of the U.S. semiconductor industry’s most pressing design productivity challenges and strengthening U.S. leadership in broadband, 5G, and next-generation radio-frequency hardware.

Natcast has selected three anticipated proposal teams for award. These teams are led by Keysight Technologies, Princeton University, and the University of Texas at Austin, respectively, and comprise top experts from academia and industry. Projected awards will range from \$7.5 million to \$10 million each, with projects expected to commence in 2025 and last 30 months. The success of these projects will



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**Thank You**