Design and In-training Optimization of Binary Search ADC for Flexible Classifiers

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Agenda

- Introduction
  - Flexible Electronics
  - ADCs in Flexible Electronics
- Optimization Approach
  - Full Binary Search ADC
  - Pruned Binary Search ADC
- Results
- Conclusions

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- **Introduction**
  - Flexible Electronics
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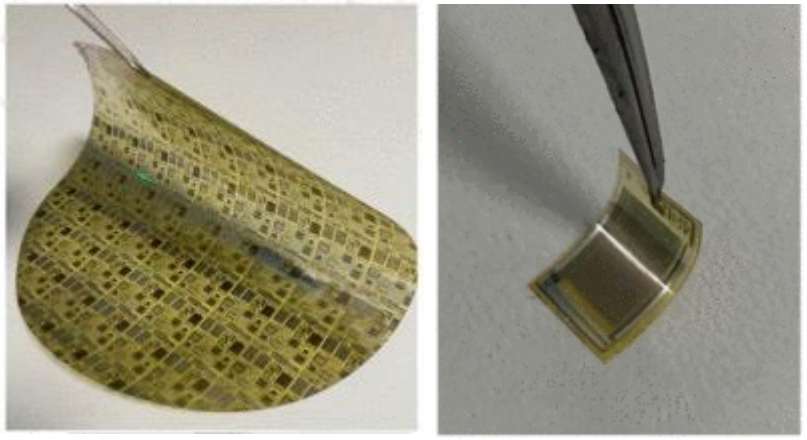
Introduction: Flexible Electronics

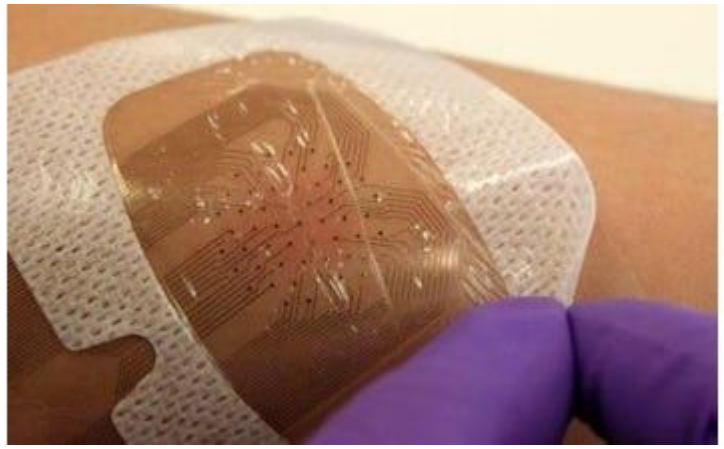
- Flexible Electronics (FE): electronic devices that can bend, stretch, and conform to various shapes, offering advantages such as mechanical flexibility, lightweight, and low-cost production.



H. Çeliker, A. Sou, B. Cobb, W. Dehaene and K. Myny, "Flex6502: A Flexible 8b Microprocessor in 0.8µm Metal-Oxide Thin-Film Transistor Technology Implemented with a Complete Digital Design Flow Running Complex Assembly Code," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 272-274

Introduction: Flexible Electronics

- Complementary to silicon-based technologies.
- Applications span across multiple domains, such as healthcare, forensics, packaging, and other fields like consumer electronics.



IDTechEx. "Flexible Electronics and Smart Bandages Are Key to Cost Savings."

Introduction: Flexible Electronics

- We are using PragmatIC FlexICs PDK based on Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistor (TFT) technology.
- Challenges: Large feature sizes, high-power consumption, availability limited to only N-type transistors.
- Objective: Find optimization approaches.

Introduction: ADCs in Flexible Electronics

- Analog to Digital Converters (ADCs) in FE: primary bottleneck in achieving efficient, compact, and low-power flexible Machine Learning systems.

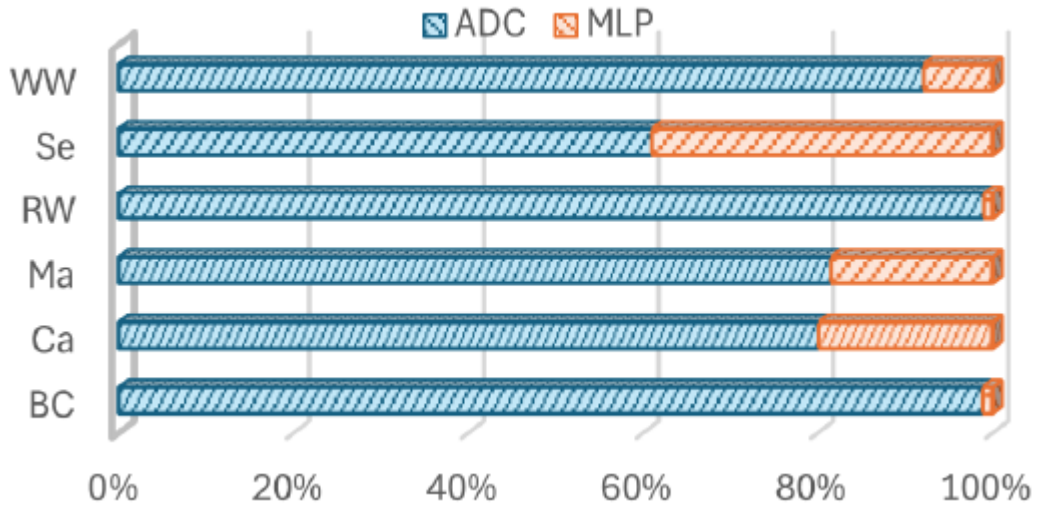


Fig. 1: Transistor Count Evaluation of the printed classification System in [2]

[2] Florentia Afentaki and et al. 2024. Embedding Hardware Approximations in Discrete Genetic-based Training for Printed MLPs. In 2024 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 1–6.

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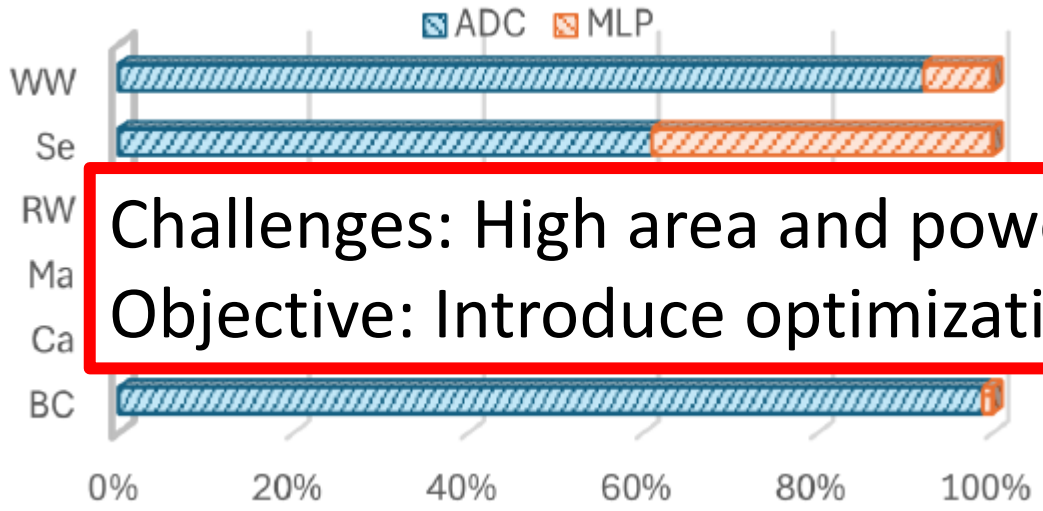


Challenges: High area and power consumption of ADCs.

Objective: Introduce optimization approaches for ADCs.

[2] Florentia Afentaki and et al. 2024. Embedding ic-based Automation DATE).

Fig. 1: Transistor Count Evaluation of the printed classification System in [2]

Introduction: ADCs in Flexible Electronics

- Conventional ADCs:
  - Flash ADCs: High speed, but large area and power.
  - Binary ADCs: More efficient but can be optimized further.

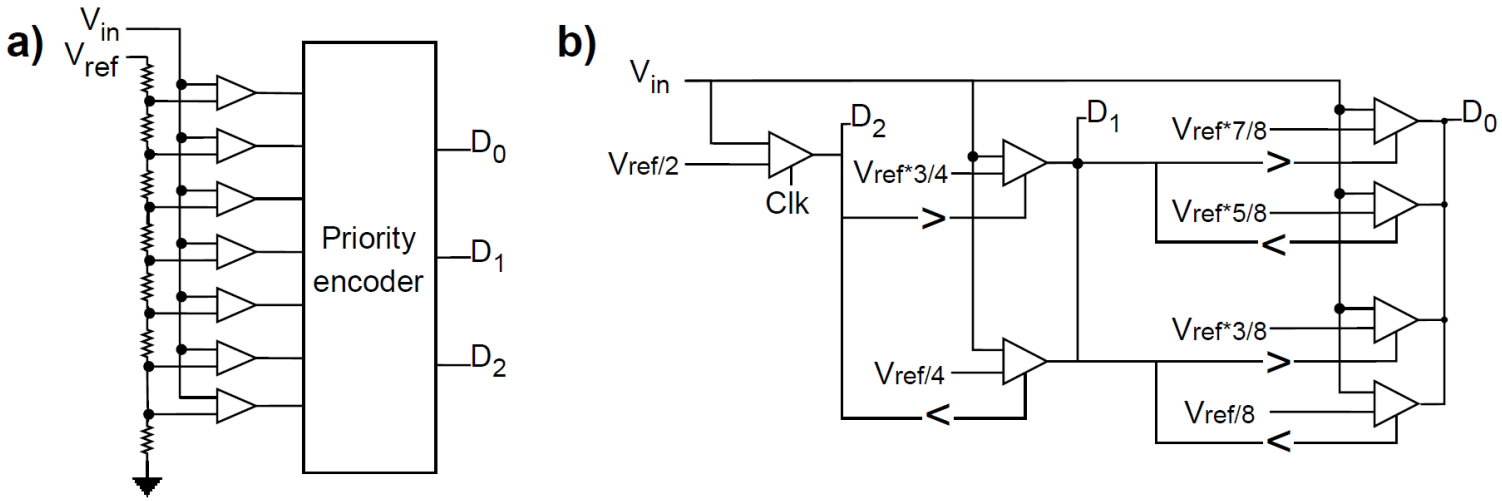
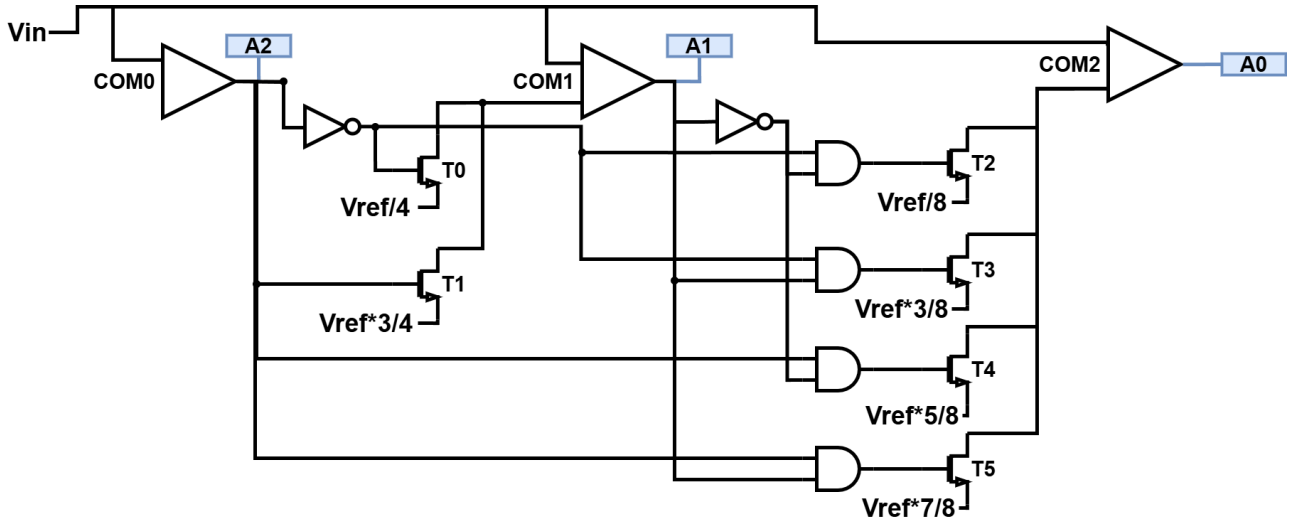


Fig. 2: Schematic of 3-bit ADC: a) Flash b) Binary Search

Introduction: ADCs in Flexible Electronics

- State-of-the-art Binary Search ADC
  - No need of an external clock signal
  - Control block made with logic gates NOT and ANDs.



[3] Shah Palash Manish Bhai and Dattatraya N. Gaonkar. 2016. Design of binary search ADC using N comparators. In 2016 IEEE First International Conference on Control, Measurement and Instrumentation (CMI). 499–502.

Fig. 3: Schematic of a 3-bit Binary Search ADC presented in [3]

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- Introduction
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  - ADCs in Flexible Electronics
- **Optimization Approach**
  - Full Binary Search ADC
  - Pruned Binary Search ADC
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Optimization Approach 1: Full Binary Search ADC Design

- Transition from Flash to Binary Search ADCs.
- Key Features:
  - **No encoder required**, reducing both area and power.
  - Efficient design rules tailored for FE.

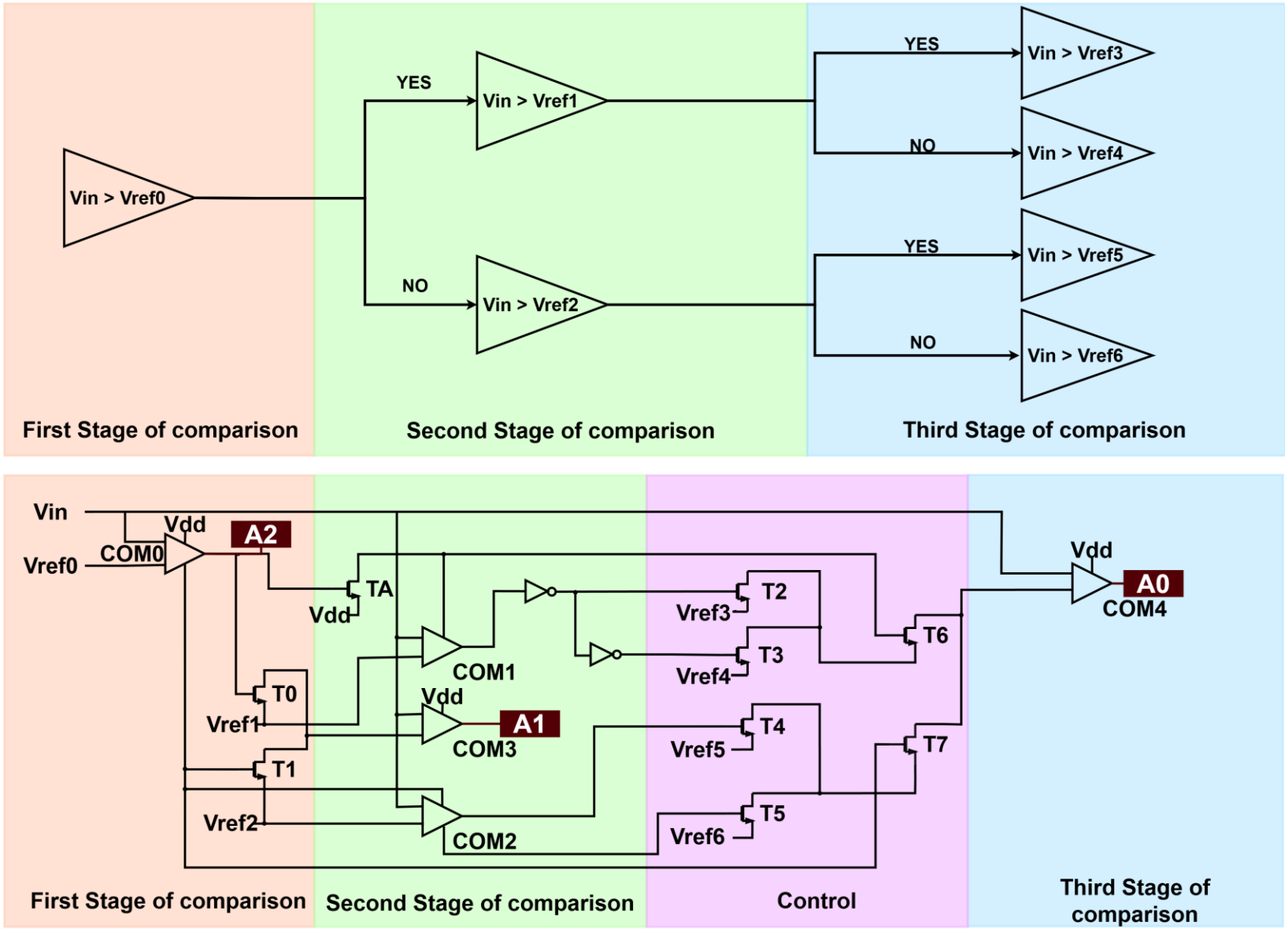
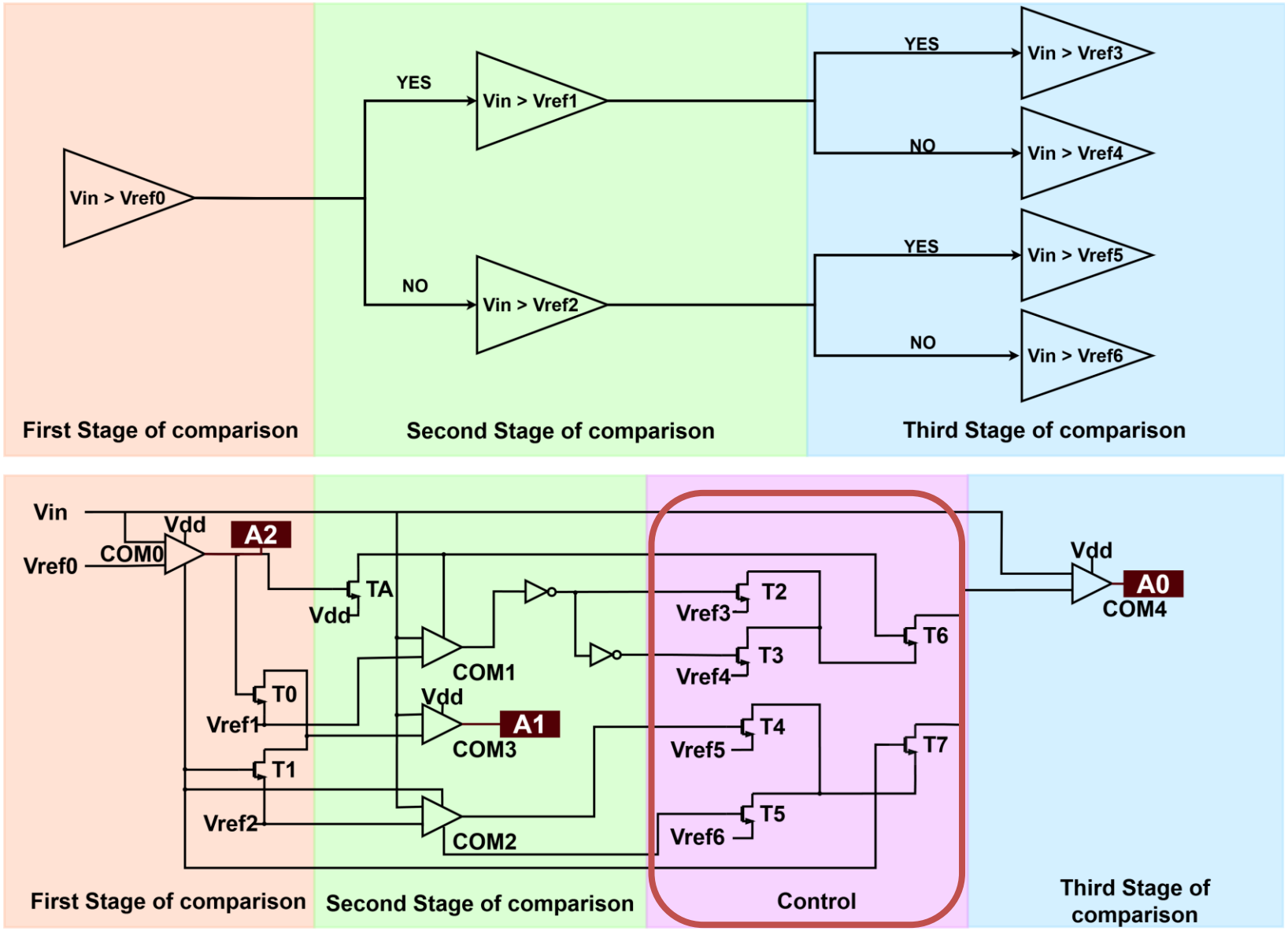


Fig. 2. Block diagram of a Binary Search ADC and the schematic of proposed 3-bit Binary Search ADC



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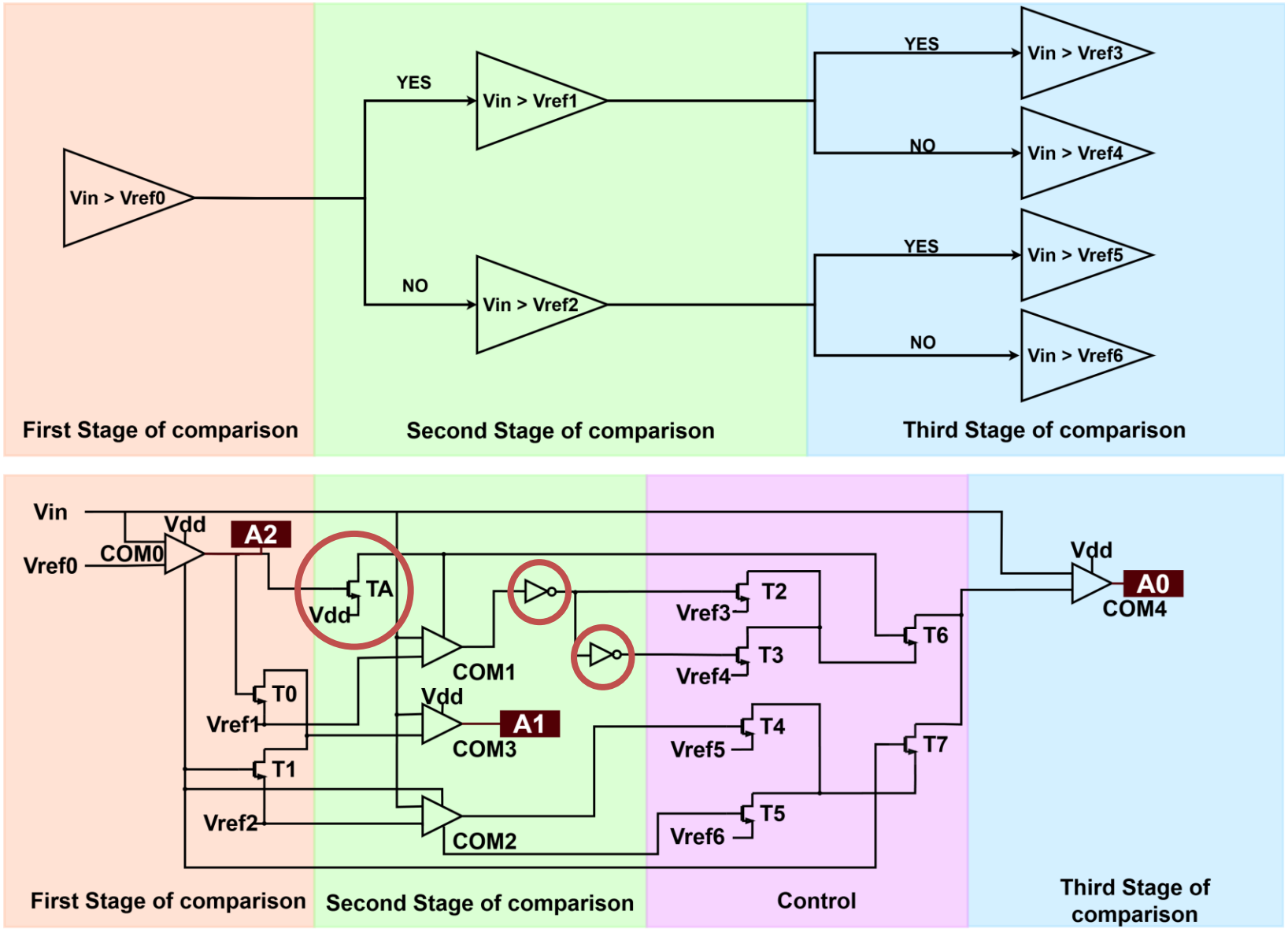

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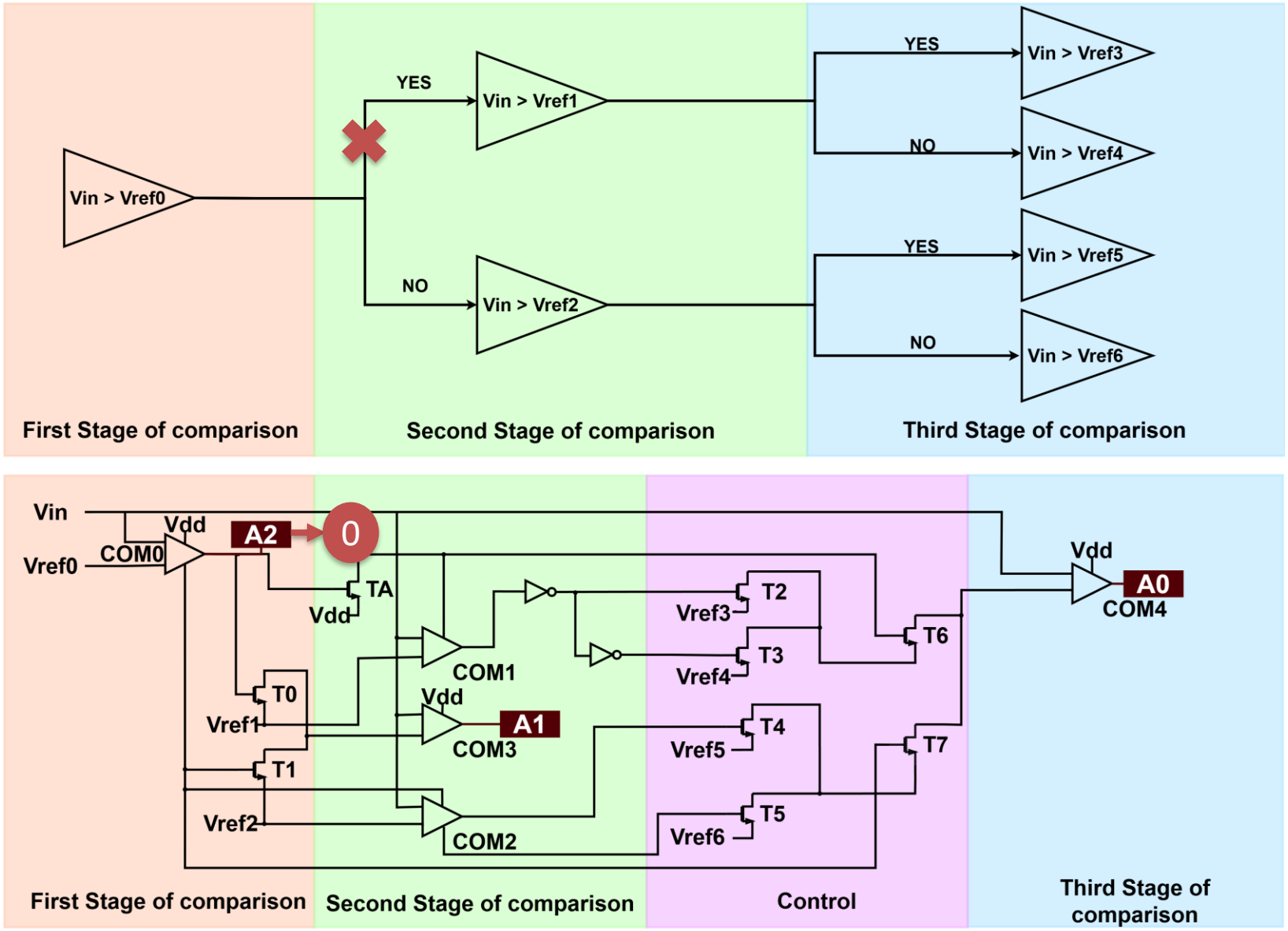

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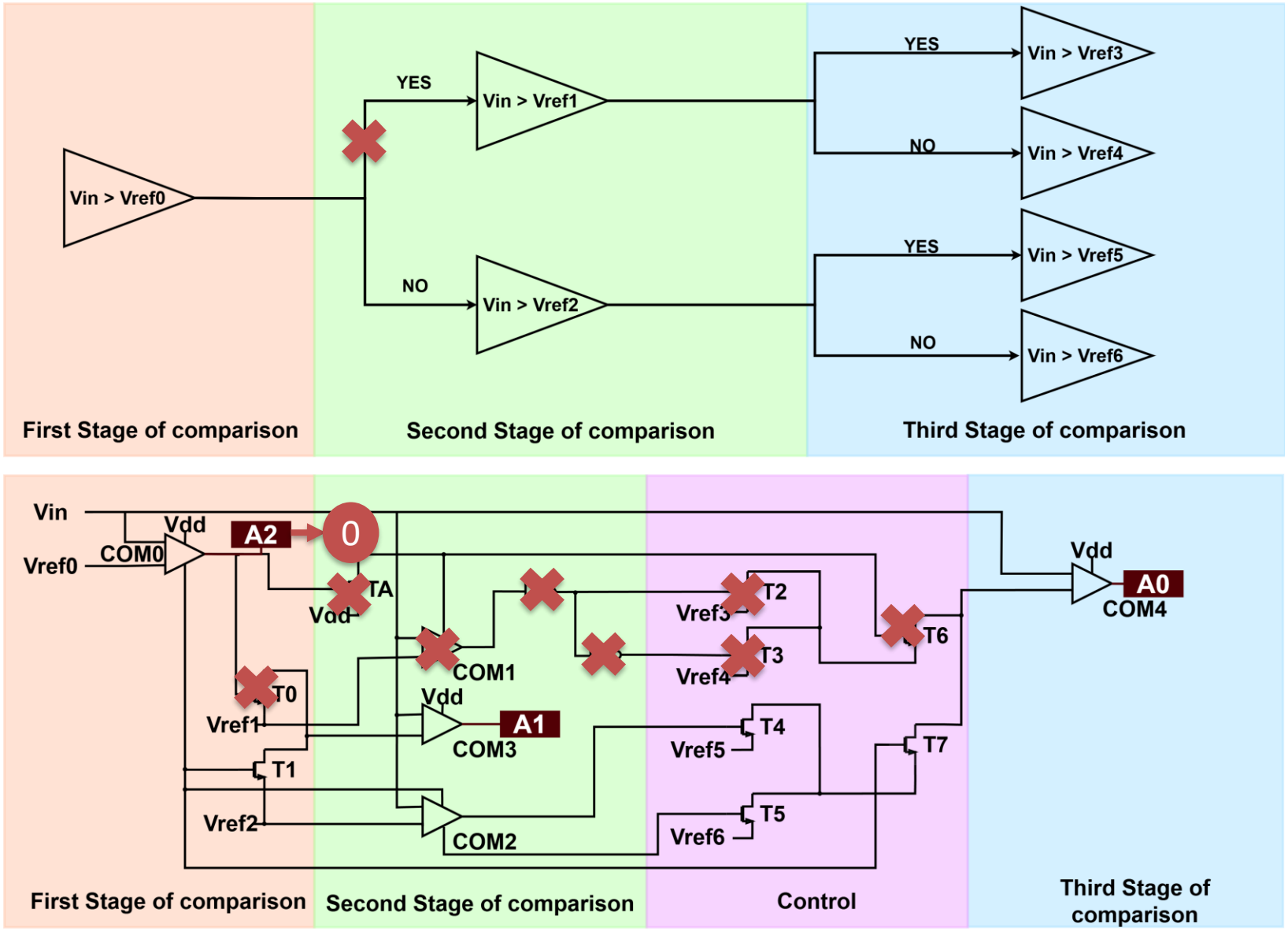

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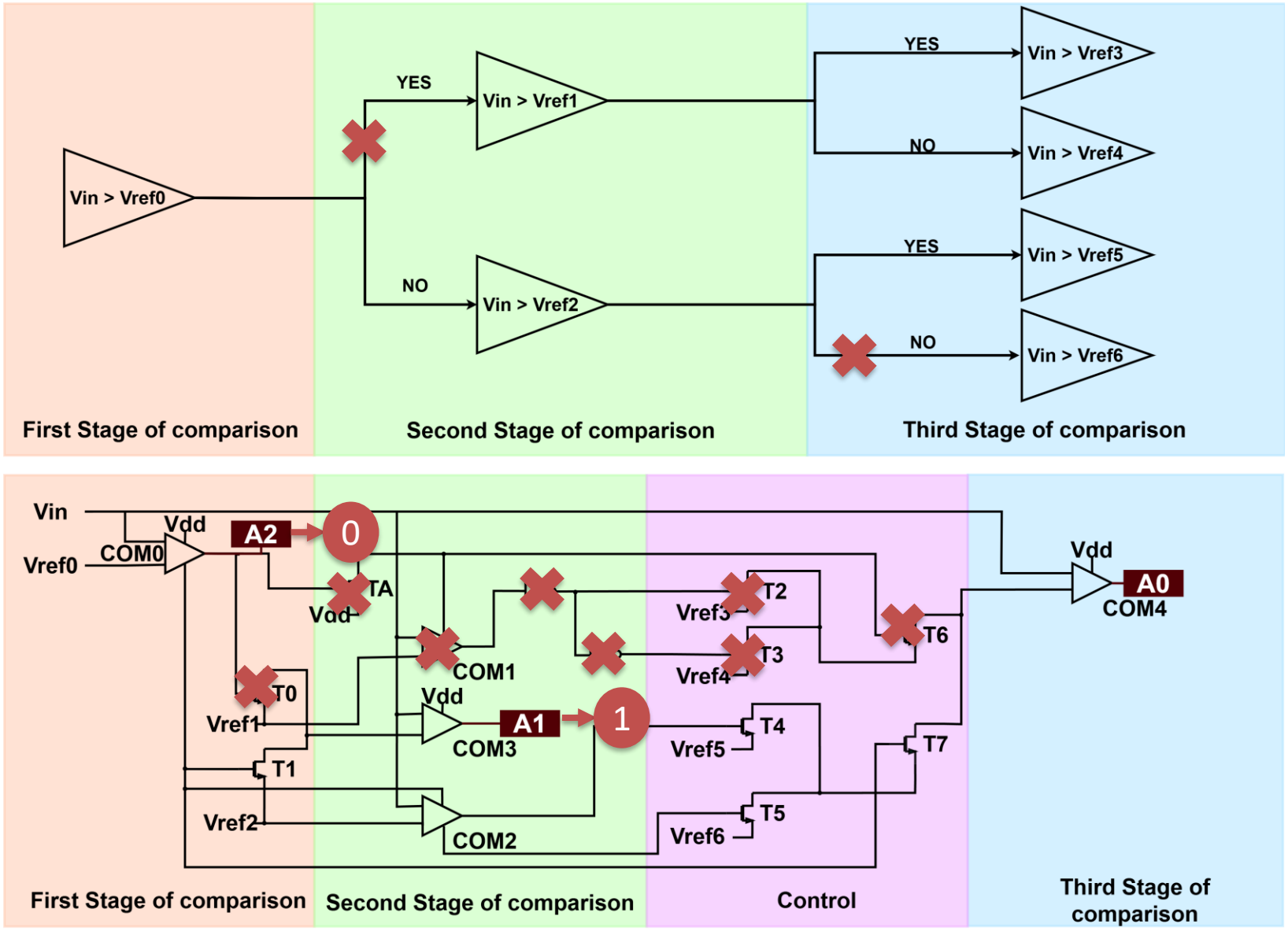

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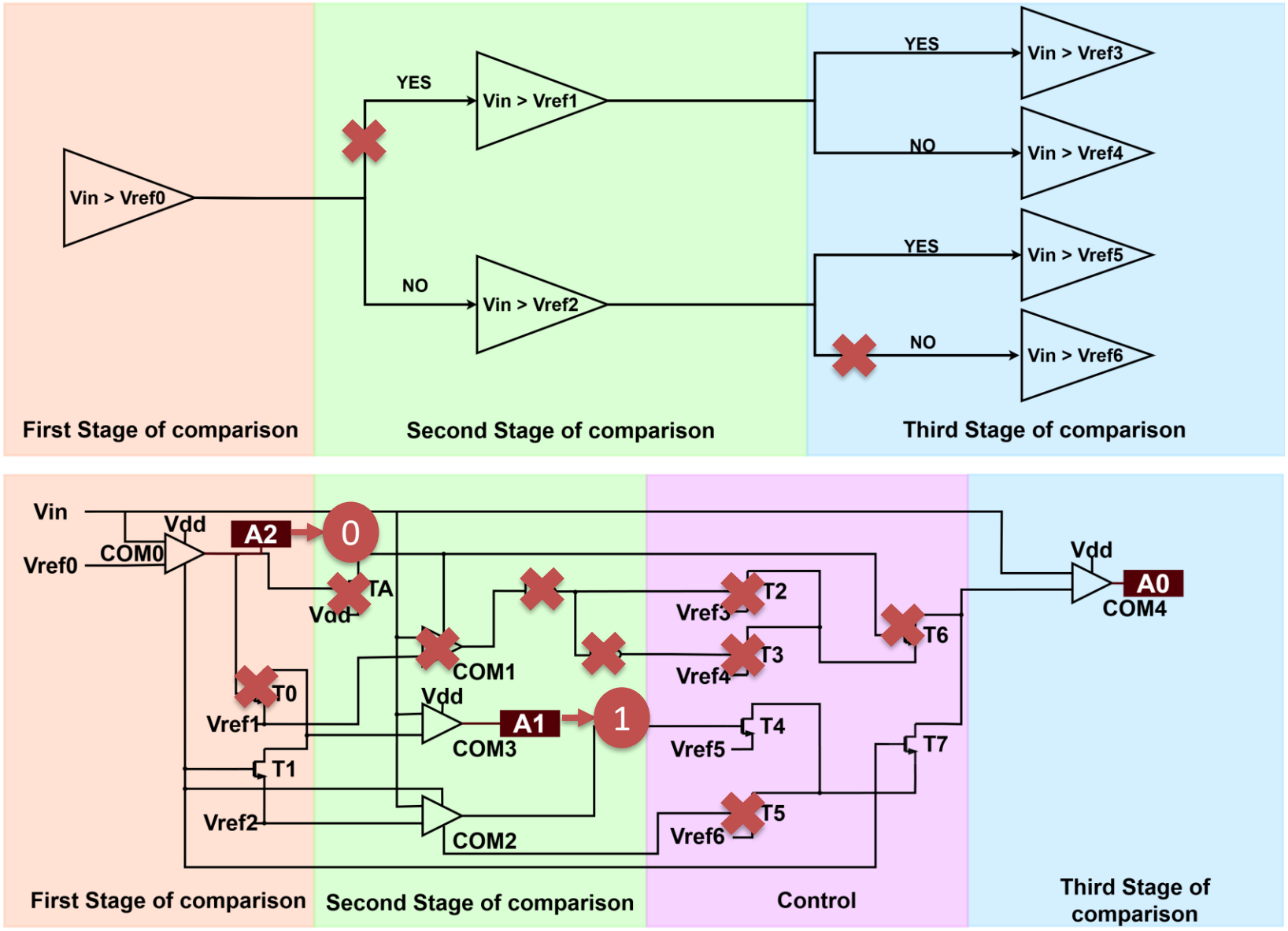

Fig. 2. Block diagram of a Binary Search ADC and the schematic of proposed 3-bit Binary Search ADC

Optimization Approach 1: Full Binary Search ADC Design

- Our solution lies in the comparator!
  - It incorporates two outputs: Vout and Vout’
  - Having the inverse of the comparator does not add more transistors or resistors in the design, just an extra wire.

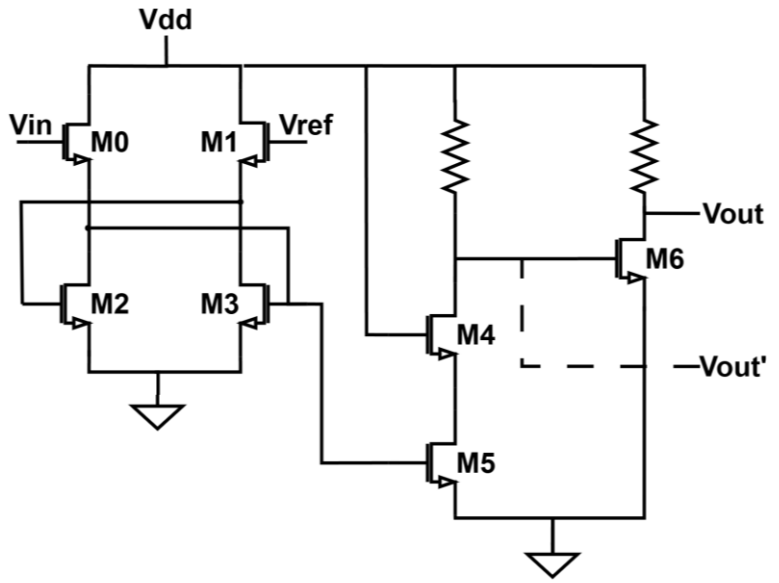

Fig. 3: Schematic of each comparator

Optimization Approach 2: Pruned Binary Search ADCs

- Motivation:
  - Customize ADCs for specific sensor inputs.
  - Minimize used representations and circuitry.
- Pruning Procedure:
  - Pruning is made in the state-of-the-art design.
  - Remove unnecessary quantization levels.
  - Reduce transistors, comparators, and logic gates in the control block.
- Result: Efficient area and power savings.

Optimization Approach 2: Pruned Binary Search ADCs

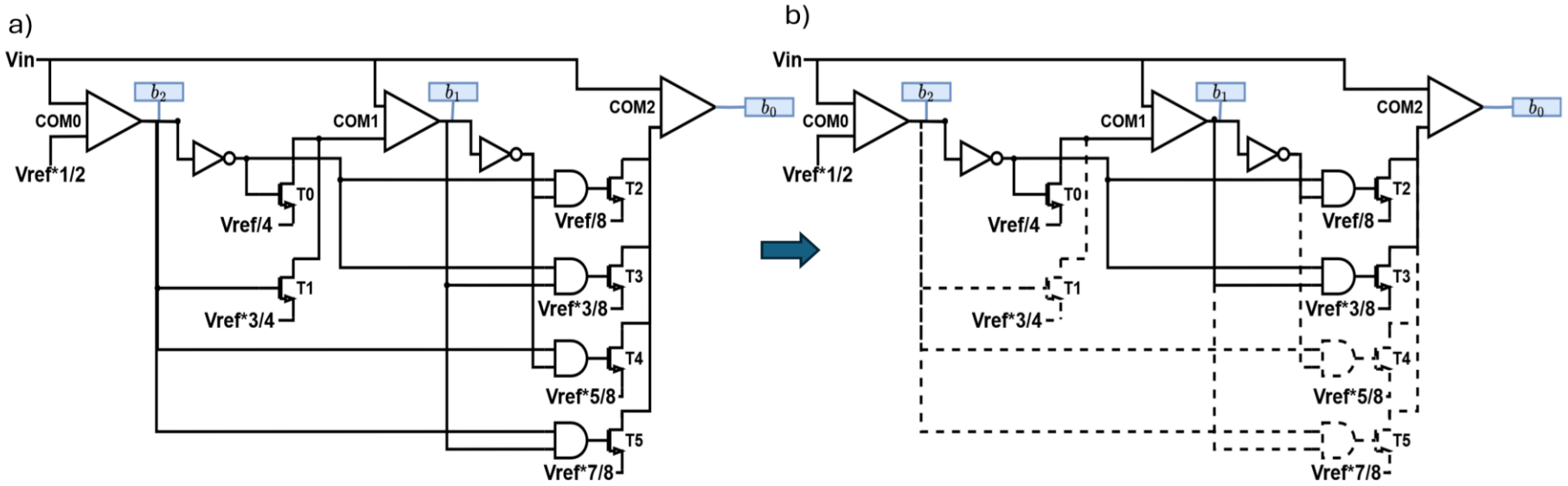

Fig. 4: Schematic of: a) conventional 3-bit Binary ADC and b) an example of an equivalent partial/pruned ADC

Optimization Approach 2: Pruned Binary Search ADCs

- Multi-objective Problem:
  - Maximize classification accuracy.
  - Minimize ADC area.
- Solution:
  - NSGA-II Genetic Algorithm.
  - Binary encoding of quantization levels.
  - Fitness evaluation: Accuracy vs. area.

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Results: Full Binary Search ADC

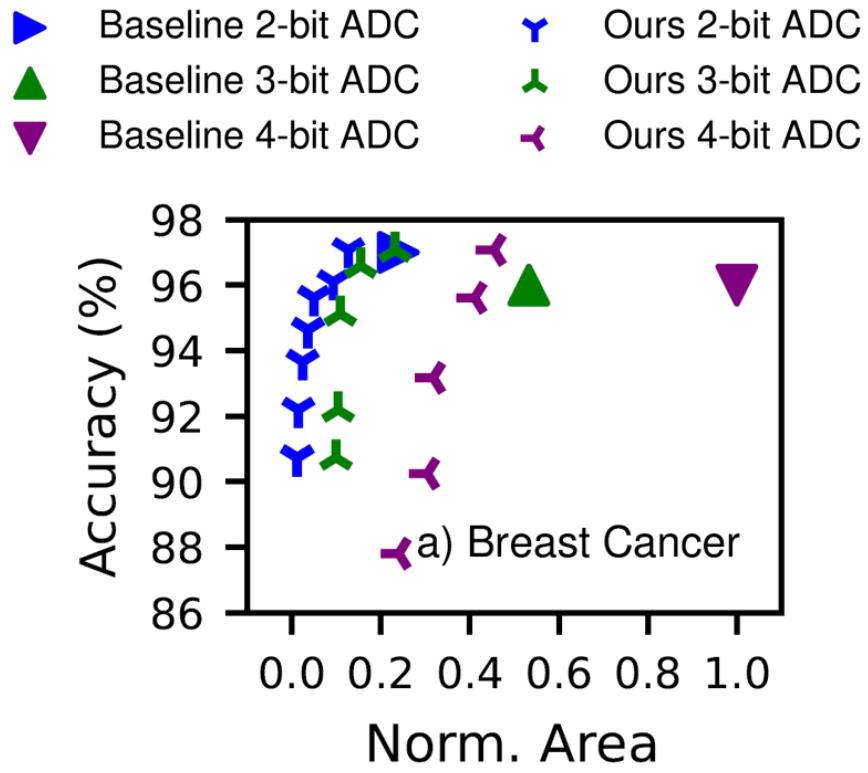
- Comparison:
  - Flash ADC vs. Baseline Binary Search ADC vs. New Design Binary Search ADC.
- Key Findings:
  - For 3-bits:
    - Area reduction: Up to 5.4×.
    - Power savings: Up to 3.3×.
  - For 4-bits:
    - Area reduction: Up to 4.3×.
    - Power savings: Up to 5×.

Architecture		Accuracy (bits)	Area(μm^2)	Power (nW)
Flash		3	95066	993,2
		4	212635	2684
Binary Search	Baseline	3	35722	365,1
		4	86556	829,5
	New design	**3**	**17679**	**360**
		4	**50027**	**541,8**

Table 1. Comparison between full ADCs

Results: Pruned ADCs - Pareto Analysis

- Pruned ADCs outperform baseline designs.



– Up to 24.2× area reduction for 2-bit ADCs.
– Negligible accuracy loss (<5%).

Fig. 5: Pareto space of Accuracy vs normalized Area of 2, 3 and 4-bit ADCs for Breast Cancer dataset.

Results: Pruned ADCs

- From Flash to Full Binary Search ADC transistor count is reduced by 46% on average. Further transitioning to Pruned Binary Search ADC reduces transistor count by an additional 51% on average.
  - Accuracy increased on average 3%.

	Accuracy		Area (TC)[2]			(3)	(4)	(5)
	Baseline[1]	Pruned	Flash	Binary	Pruned	Gains (%)	Gains (%)	Gains (%)
2bit	73	78.2	423	235	134	56	57	316
3bit	77	78.0	1138	523	249	46	48	458
4bit	76	78.0	2676	981	474	37	48	565

Table 2. [1]Accuracy for both Flash and Binary Baseline ADCs. [2]Area in Transistor Count. [3]Area gains by replacing Flash with Binary ADC. [4]Area gains by replacing Binary with Binary Pruned ADCs. [5]Area gains by replacing Flash with Binary Pruned ADCs.

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Conclusions

- ADCs are the primary bottleneck in achieving efficient flexible Machine Learning systems, making it essential to explore optimization strategies.
- Binary Search ADC emerges as a promising solution for designs constrained by area and power requirements.
- Our exploration benefit from
  - Full Binary Search ADC: 5.4× area reduction compared with Flash ADC.
  - Pruned Binary Search ADCs: 5× transistor count reduction for less than 1% accuracy loss.

ありがとうございます (Thank You!)

- Thank you for your attention.
- Looking forward to your questions!

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