On Awareness of Offset-Via and Teardrop in Advanced Packaging Interconnect Synthesis

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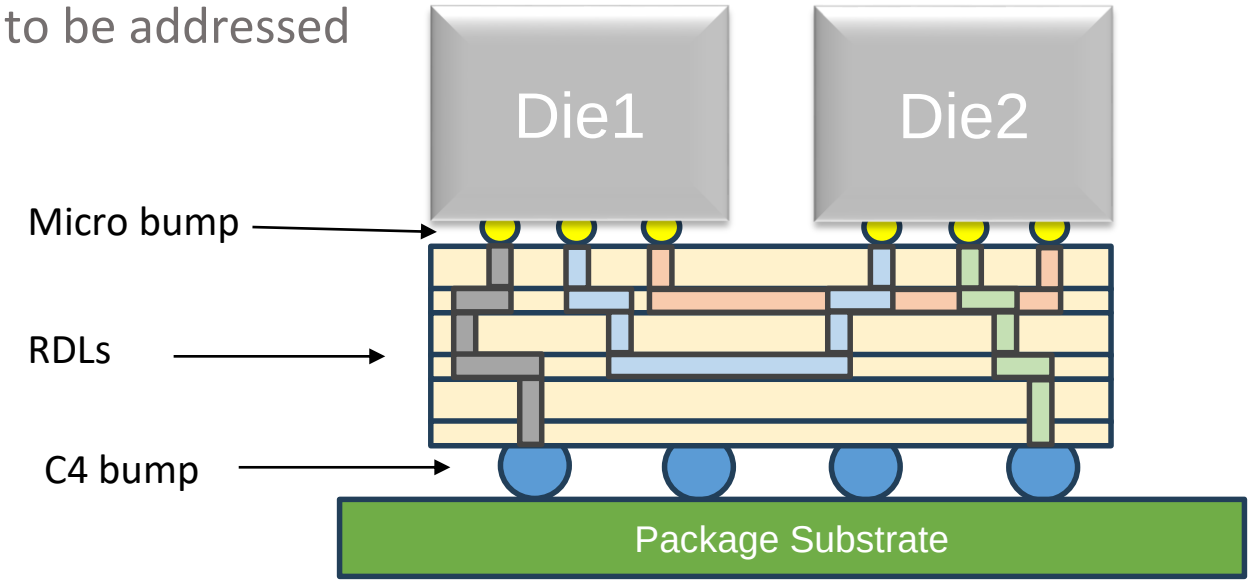
Outline

- **Introduction**
- Optimizing Offset-via Assignment
- S-route Guided A* Search
- Experimental Result
- Conclusion

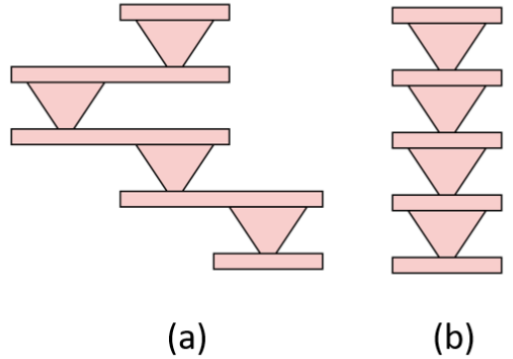
Introduction

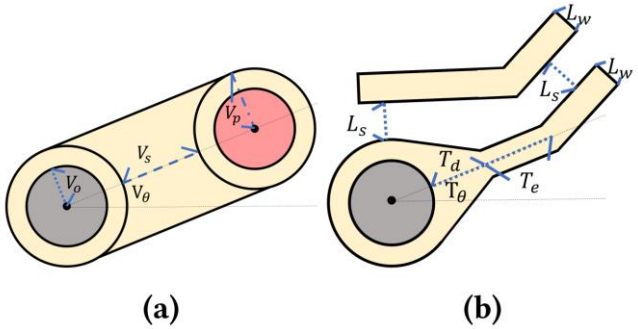
- **Background and Motivation**
  - The area of single chips has continuously increased
  - While this has boosted performance, it has also led to a decrease in manufacturing yield
  - Chiplet technology has become mainstream
  - Connect different chiplets through fine-pitch Redistribution Layer (RDL) connections
- **Challenges of Advance Package**
  - Offset-vias and teardrops enhance reliability and manufacturability
  - Signal integrity (SI) issues need to be addressed



Offset-Via and Teardrop

- Traditional stack-via suffers more line strain
  - Especially when the number of RDL layers is increased
- Offset-Via improves the reliability
  - Two adjacent layers cannot have vias in the same position
- Teardrop
  - Connecting wires directly to vias can also lead to high stress and cracks
  - Employing metal shrinkage from the via to the wire can alleviate stress
- Incorporating offset-via and teardrop structures in die-to-die routing [1]
  - Helps reliability
  - Significantly reduces the routing resources

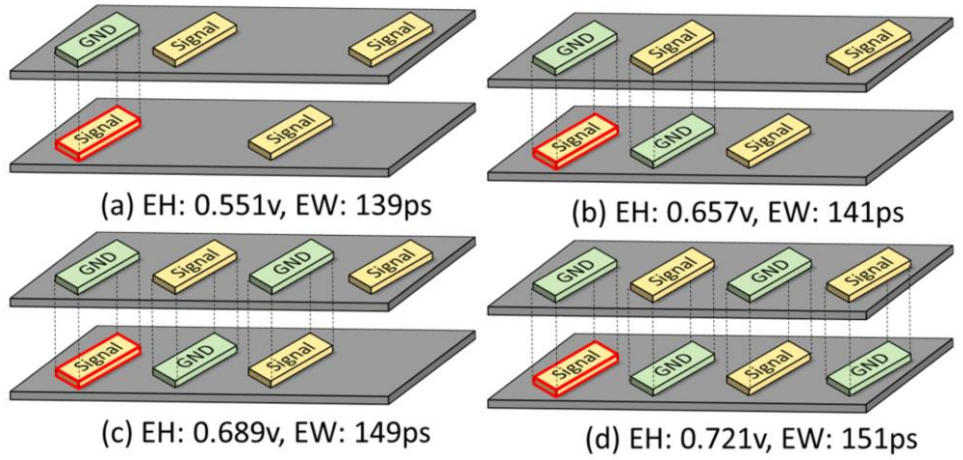


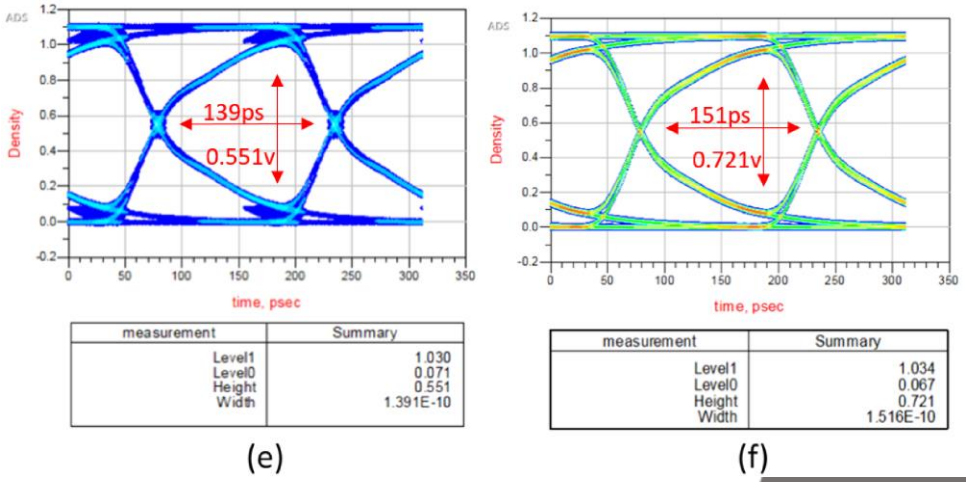


[1] H.-M. Chen, C.-W. Ho, S.-H. Wu, W. Lu, P.-T. Huang, H.-J. Chang, and C.-N. J. Liu,“Reshaping system design in 3d integration: Perspectives and challenges,” in Proceedingsof the 2023 International Symposium on Physical Design, pp. 71–77, 2023.

Signal Integrity

- Signal integrity (SI) becomes a more serious issue
- Eye Diagram is a typical way to evaluate SI
  - Eye Width (EW) increase:
    - Lowering the likelihood of timing errors
  - Larger Eye Height (EH)
    - Reducing the possibility of functional errors
- Analyze the SI performance by using Keysight ADS
  - Different ground shielding structures
- Fully shielding is often required for high performance packages
  - Increase the requirement for routing resource
  - Very challenge in high density packages

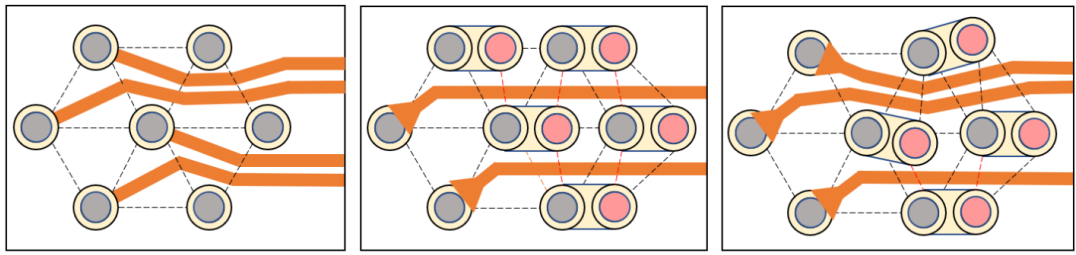




[3] Y. Chiang, S. Tai, W. Wu, J. Yeh, C. Wang, and C. Douglas, “Info_os (integrated fan-outon substrate) technology for advanced chiplet integration,” in 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), pp. 130–135, IEEE, 2021.

Related Works

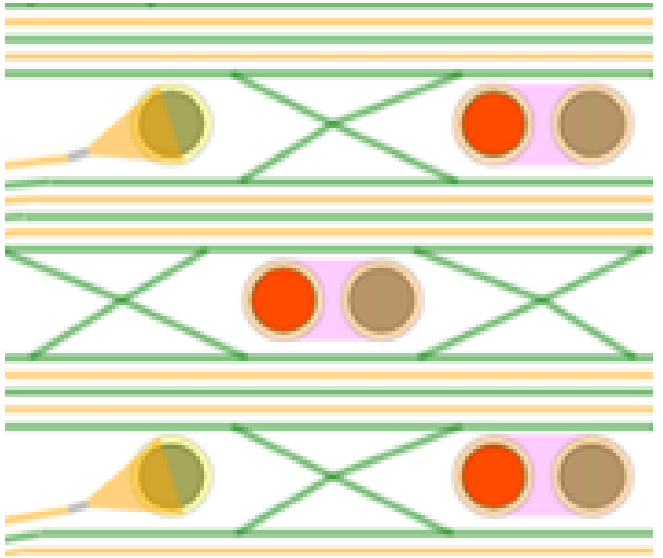
- [2] proposed the first any-angle RDL router in the literature
- [4] proposed a crossing-aware A* search algorithm
  - Using the chord-based tile model
  - Create the Voronoi Diagram to accommodate irregular vias
- [5] proposed the Access Point Determination algorithm to minimize wire length
- Previous work
  - Allowed the via in each layer to be placed anywhere
  - The routing region is much bigger than the via size
- Apply offset-via structure and the density bump pattern
  - The routing resource will be significantly reduced



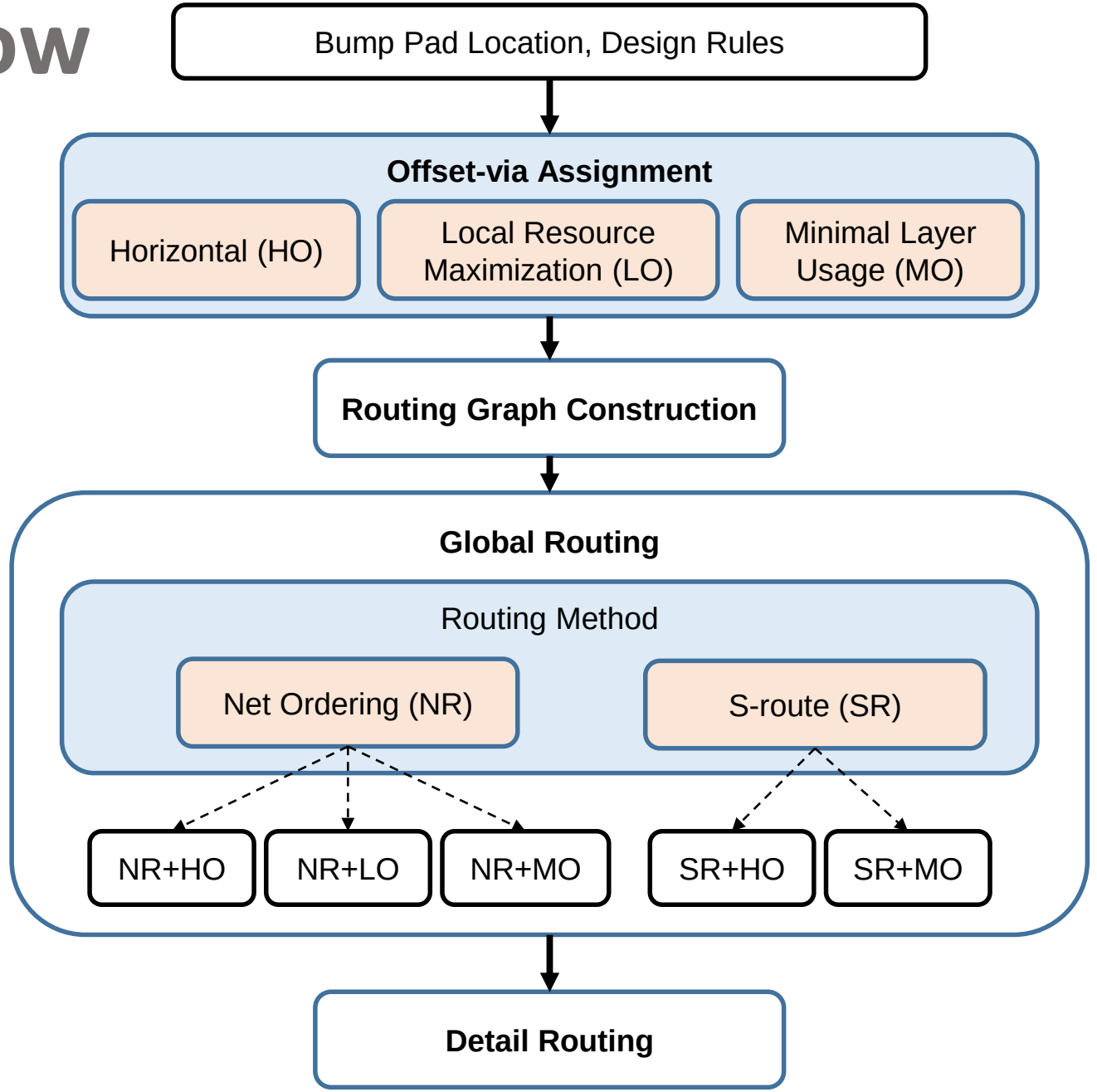
[2] M.-H.Chung,J.-W.Chuang,andY.-W.Chang, “Any-angle routing for redistribution layers in 2.5 d ic packages,” in 2023 60th ACM/IEEE Design Automation Conference (DAC), pp. 1–6, IEEE, 2023
[4] Y.-J. Cai, Y. Hsu, and Y.-W. Chang, “Simultaneous pre-and free-assignment routing for multiple redistribution layers with irregular vias,” in 2021 58th ACM/IEEE Design Automation Conference (DAC), pp. 1147–1152, IEEE, 2021.
[5] H.-T. Wen, Y.-J. Cai, Y. Hsu, and Y.-W. Chang, “Via-based redistribution layer routing for info packages with irregular pad structures,” IEEE Transactions on Computer-Aided Design of Integ Circuits and Systems, vol. 41, no. 12, pp. 5554-5567, 2022.

Contribution

- First work based on offset-via, teardrop and fully shielding consideration to solve Die-to-Die routing
- Propose a Minimal Layer Usage Offset-Via Assignment
  - Allow any-angle rotation of offset-via and teardrop
  - Increase routing resource utilization
- Propose an S-route method
  - Reduce net detour for more speedup
  - Keep the length matching
- The experimental results on HBM3 chips show that
  - The wire length is reduced by 7% and 50%
  - The RDL layer usage is reduced by 50%
  - Do not route on the first layer to keep better resource usage and length matched for subsequent layers



Algorithm Flow



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- **Optimizing Offset-via Assignment**
- S-route Guided A* Search
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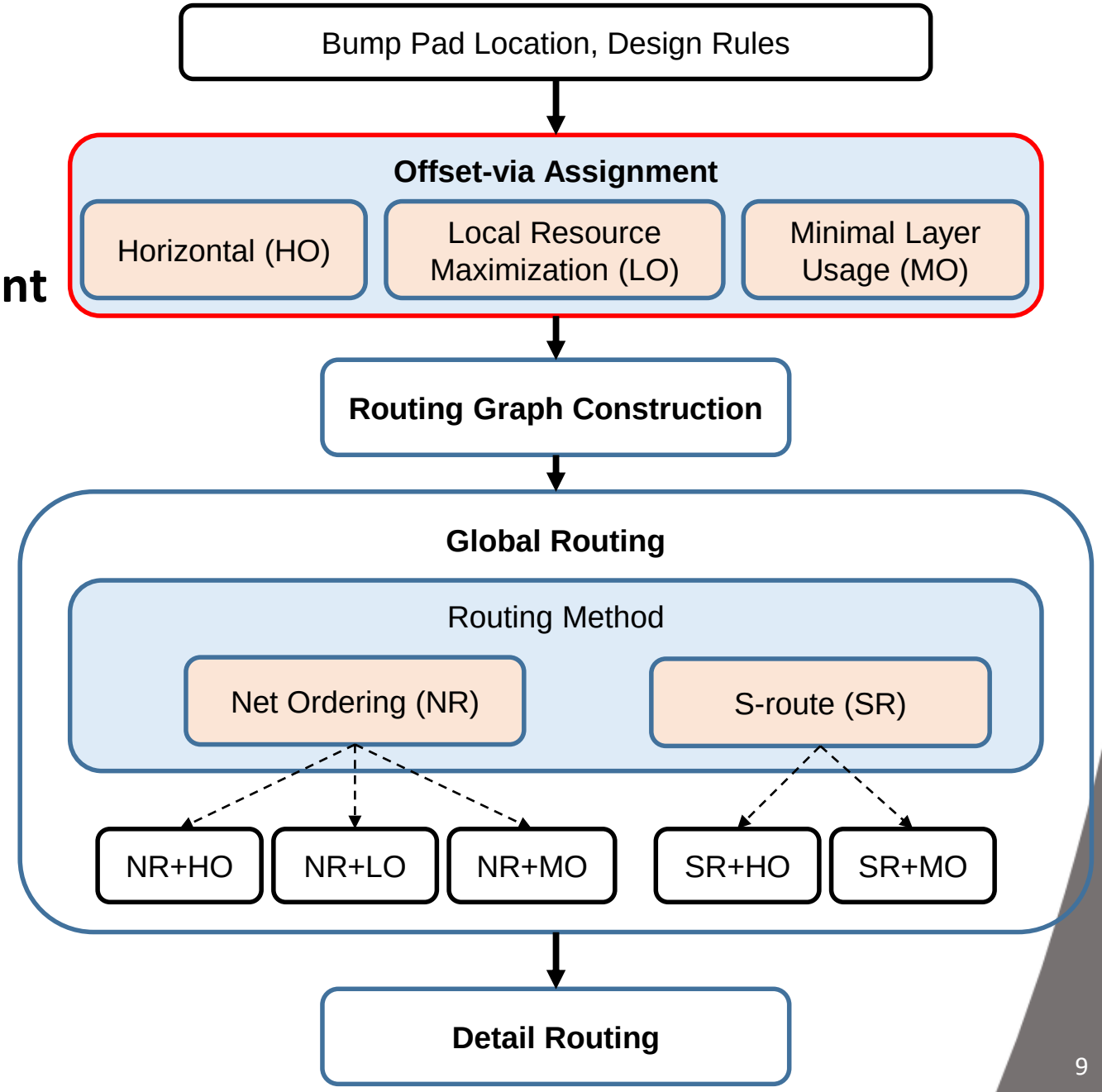
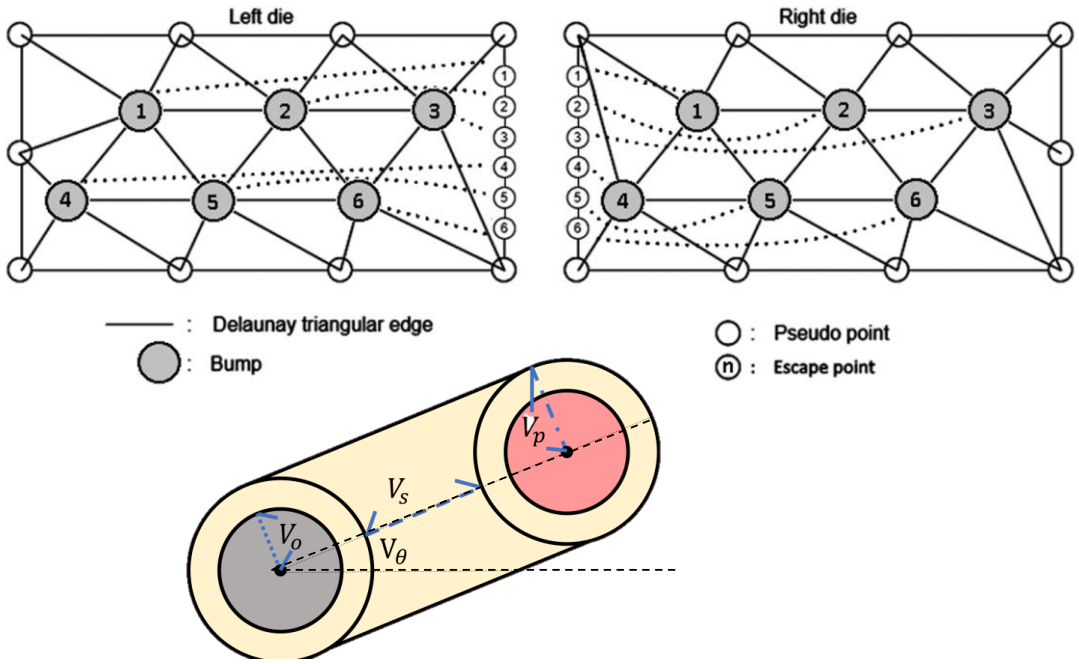
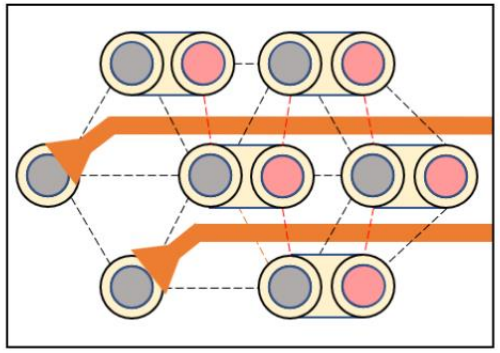
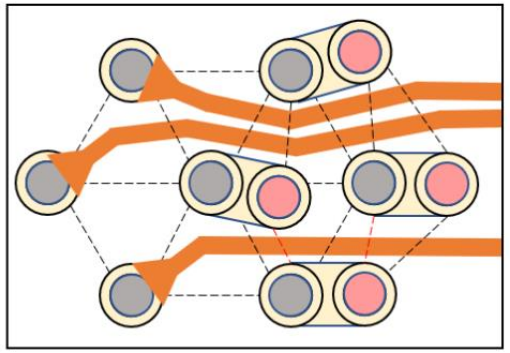


Optimizing Offset-via Assignment

- Input
  - The bumps in two dies
  - The pseudo point in the outline
  - Escape point
  - Construct the Delaunay triangulation graph
- Output
  - The rotation of each offset-via
- Goal
  - Determine the maximum total capacity after applying the offset-via
- Limitation
  - Minimum line width/spacing
  - Fully shielding constraint

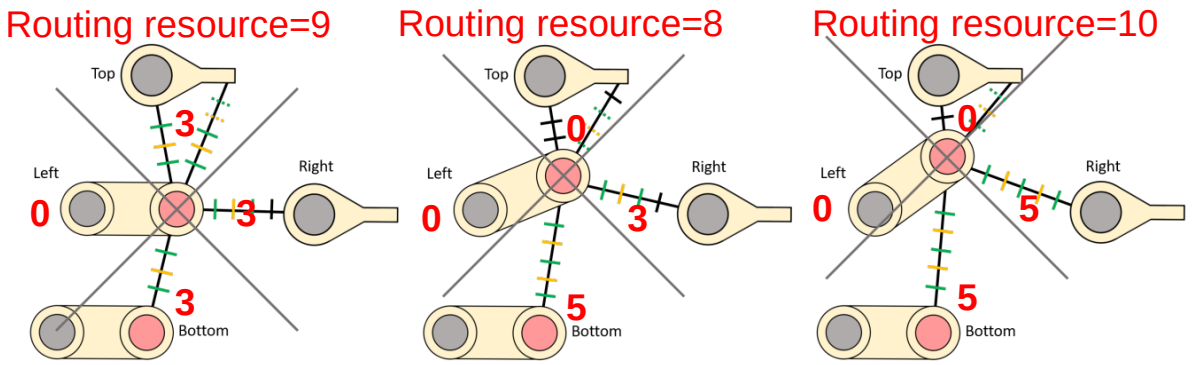






Local Resource Maximization Assignment

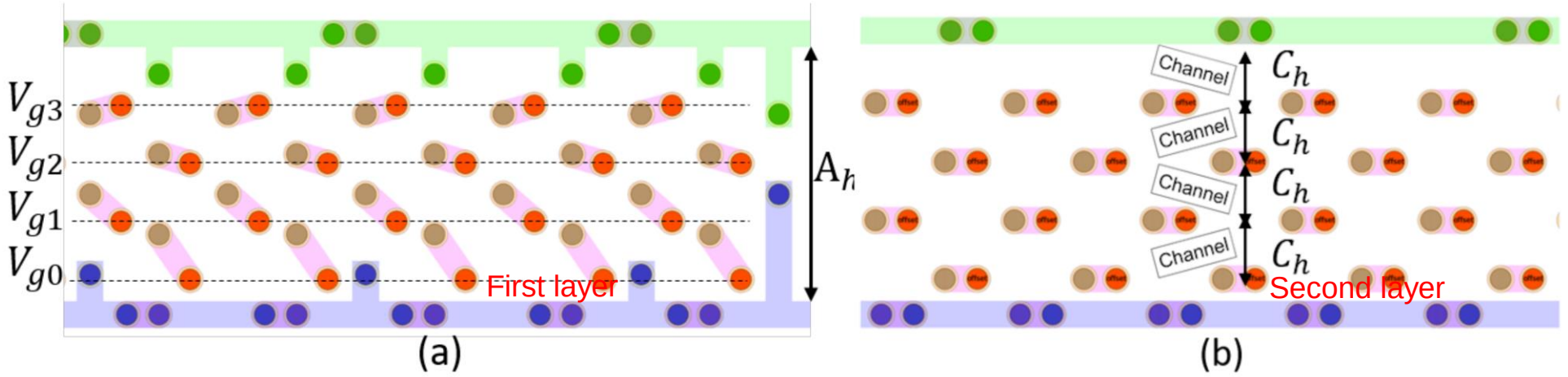
- Optimize routing resources on each layer individually
- Iteratively evaluating the routing resources around the via and choosing the angle that yields the largest sum of routing resource
- Assumption
  - Split the space near the offset-via into four routing regions
  - Each edge should follow fully shielding constraint
  - Each routing region passes the same number of net
  - The number of net is an odd number



(a) Horizontal offset-via and teardrop (b) Rotate the offset-via with 30 degree (c) Rotate the offset-via with 60 degree

Minimal Layer Usage Assignment

- Maximize the routing resources of the entire RDL layer
- The first layer is used to **determine the offset-via positions**
- Distributes routing resources **evenly across each row**, creating channels
- Channel height: $C_h = \frac{A_h - V_p - \mathrm{L}_s}{N_{vg}}$
- Via group y-coordinate: $v_{gi} = V_p + \mathrm{L}_s + i * C_h, 0 \le i \le N_{vg} - 1$



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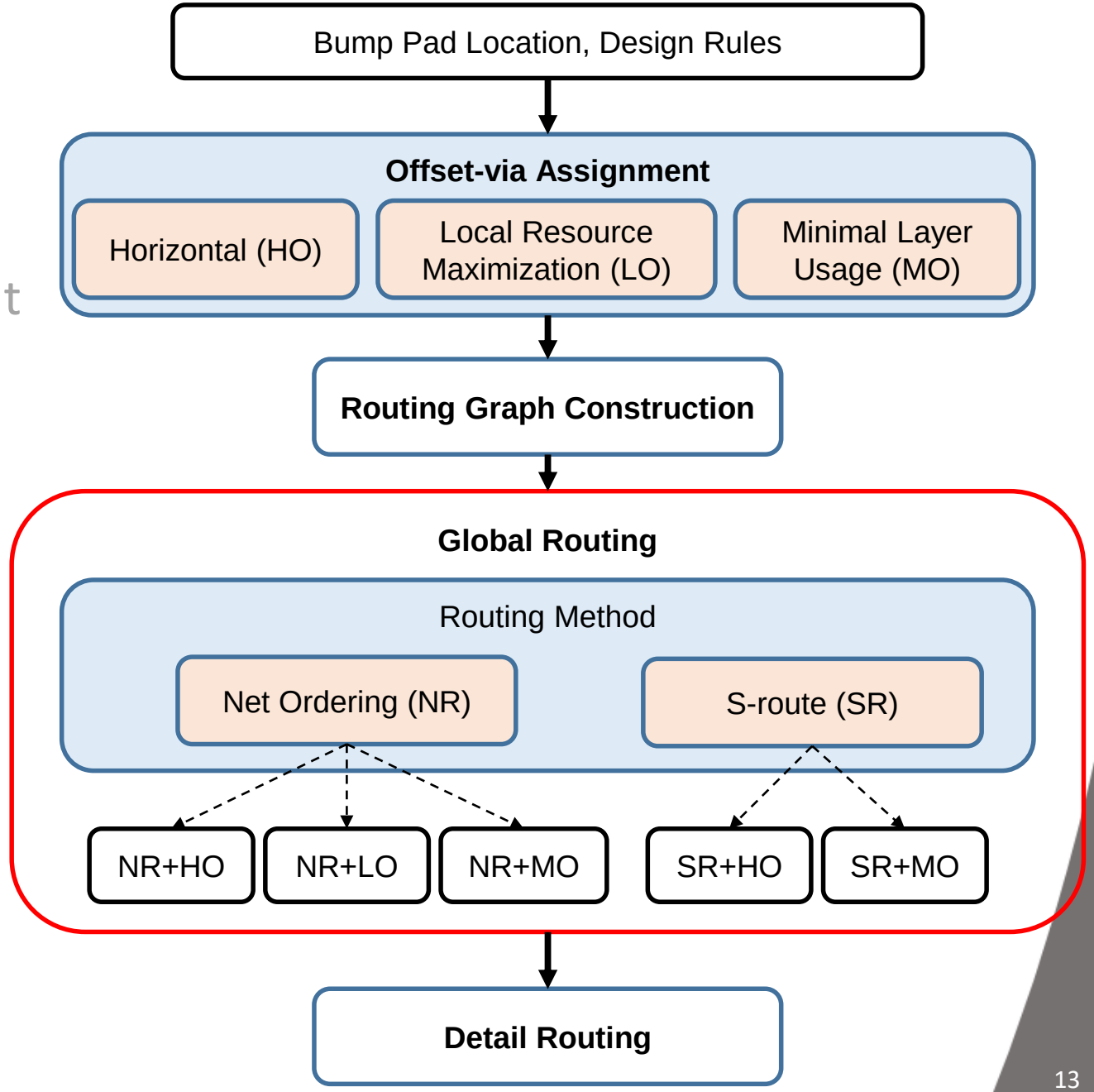
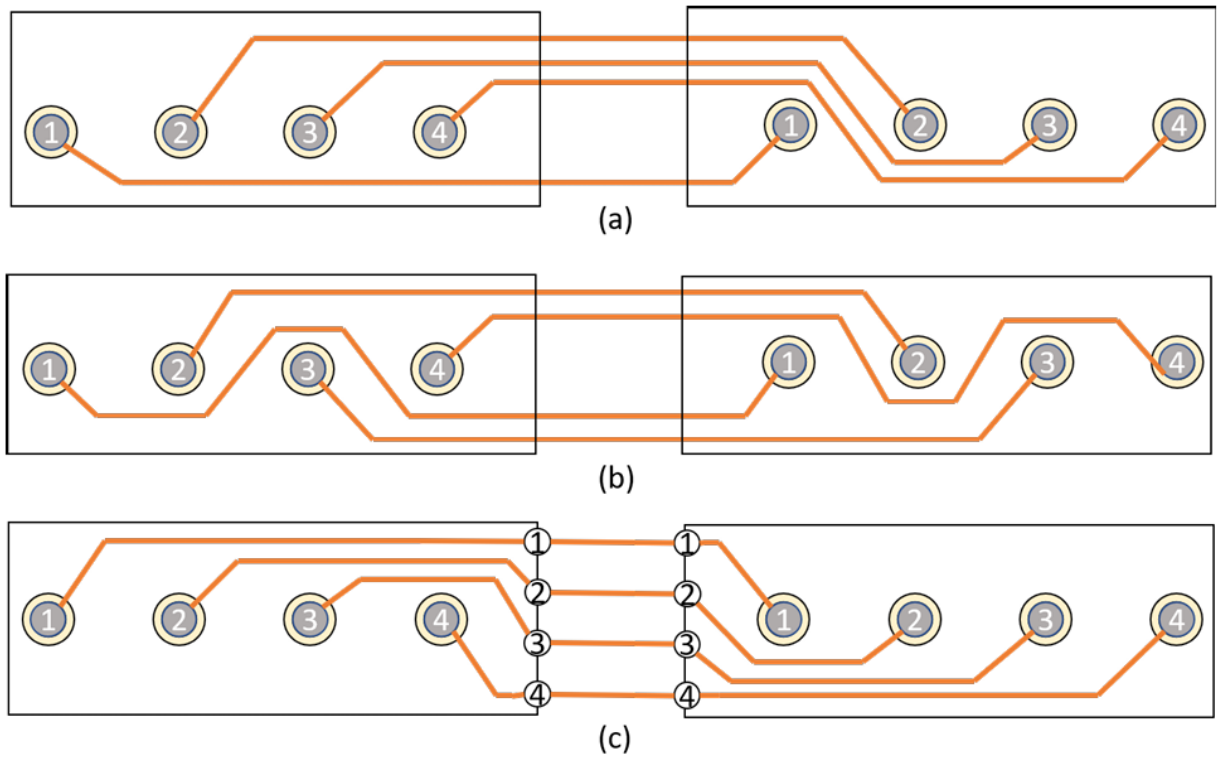


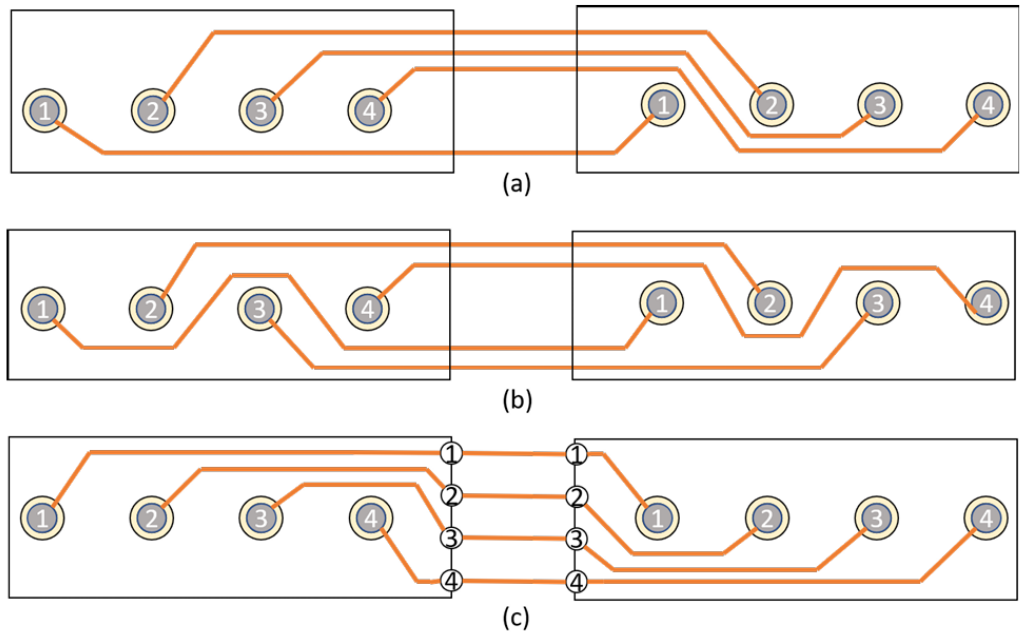
Traditional A* Search

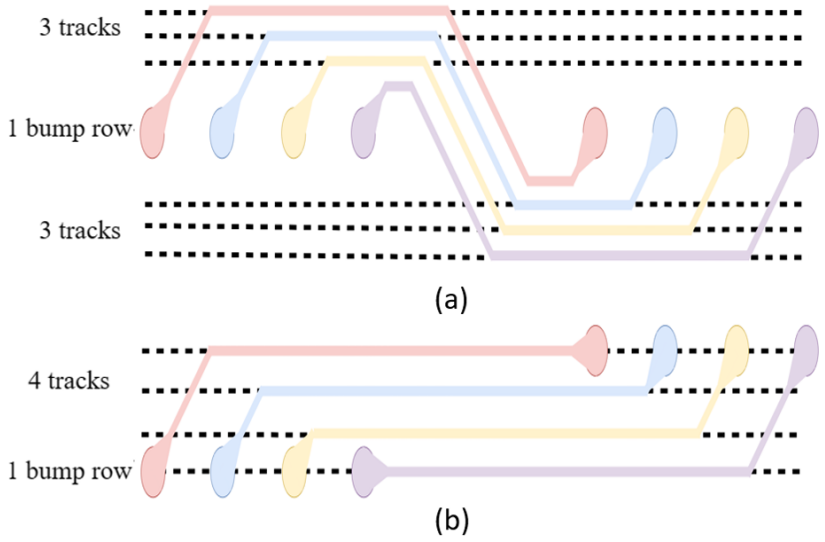
- Normal A* Search follows minimum wire length strategy
- Net ordering issues significantly affect routing performance
- Modifying the net order by ripping up and rerouting
  - Achieve a better routing outcome
  - Time-consuming



S-Route Pattern

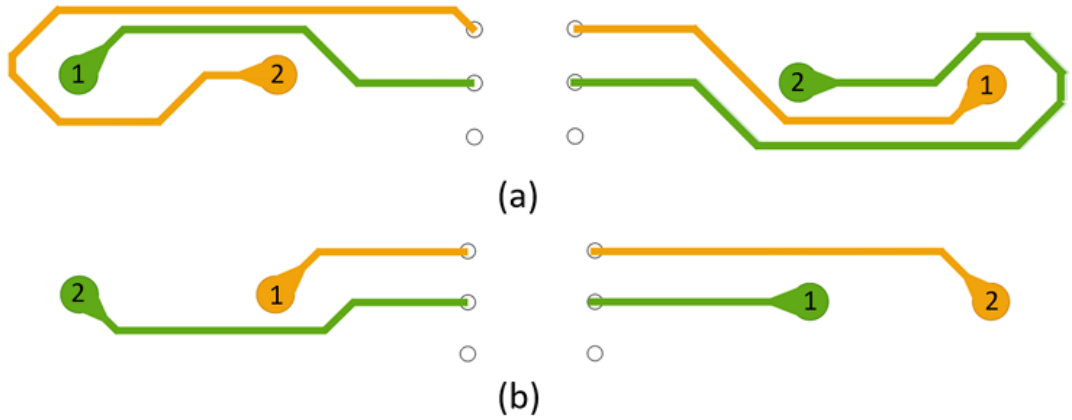
- Apply escape point to create S-Route pattern
- Decrease rip-up and reroute
- Drawback
  - Occupy more tracks
  - Redundant routing space
- Shifting the offset-via by Minimal Layer Usage Assignment
  - Reduce routing track needed
  - Decrease detour
  - Decrease wire length





S-route Net Order

- Follow middle-to-side routing order
- Net far from the escape point route first
  - Make other net detours
- Bumps closer to the escape point are prioritized in the routing order
  - Detour decrease
  - Reduce the wire length



S-route Guided A* Search

- Lines 3-10
  - Organize all via groups
  - Calculate escape point position
- Lines 11-12
  - Determine net priority
- Lines 13-15
  - Construct a routing graph
  - Calculate capacity
- Lines 16-17
  - g(n): distance already traveled
  - h(n): estimate distance to candidate point
  - a(n): accumulate y-axis shift

Algorithm 1 S-route guided A* Search

1: **Input:** VDD, VSS, Bump, Offset-via
2: **Output:** Routing result
3: **Generate escape point**
4: $Sort(V_g, y)$
5: for all V_{gi} in V_g do
6: $B \in V_{gi}$
7: $Sort(B, x)$
8: $Net \bigcup B_i, B_i \in B$
9: end for
10: $E_{i.y} = A_h - V_p - i * (2 * L_s + 2 * L_w), 0 \leq i \leq |Net| - 1$
11: **Apply initial S-route net order**
12: Net priority = $d(B_i, E_i)$
13: **Routing Graph Construction**
14: E = DT(node)
15: $C_i = \lfloor (E_i - 4 * L_s - 4 * L_w)/(3 * L_s + 3 * L_w) \rfloor, E_i \in E$
16: **A* Search for Final Detail Routes**
17: $f(n) = g(n) + h(n) + a(n)$

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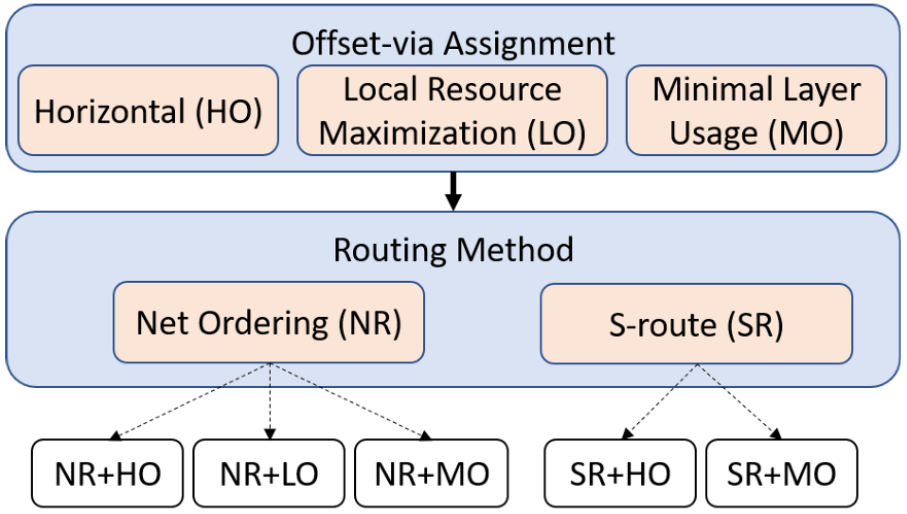
Experimental Result

- Environment
  - Intel Xeon CPU E3-1230 v6 @ 3.50GHz processor
  - Implement in C++14 using g++ version 10
  - Employing version 5.5.1 of the CGAL library [6] to construct Delaunay triangulations routing graph
- The Benchmarks of four test cases

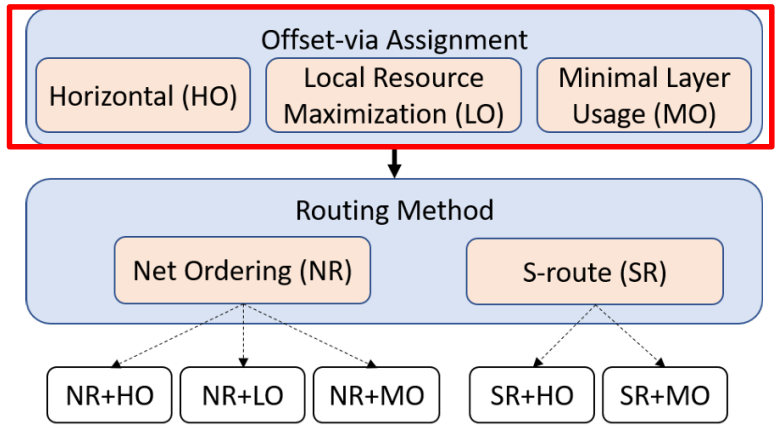
Designs	#Layers	#Rows	#Columns	#Nets
Circuit 1	5	6	16	48
Circuit 2	5	6	12	36
Circuit 3	5	4	24	48
Circuit 4	5	4	18	36

- Experimental setting with offset-via assignment and routing method



Routing Resource Analysis

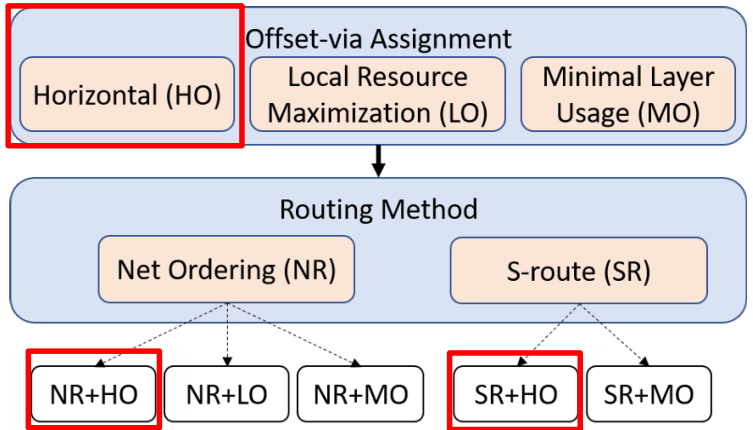
- **The routing resource comparison of different offset-via assignments**
- Horizontal Offset-Via
  - Baseline
- Local Resource Maximization Offset-via Assignment
  - Iterative rotates the offset-via angle to reduce the unused capacity in each layer
  - Enhancing the routing resource by approximately 6%
- Minimal Layer Usage Offset-via Assignment
  - Maximize the routing resources of the entire RDL layer
  - Significantly increase the routing resource in the following layers by 50%



	Circuit1	Circuit2	Circuit3	Circuit4	
Horizontal Offset-Via	2560	1867	2833	1942	1
Local Resource Maximization Offset-via Assignment	2730	1967	2992	2059	1.06
Minimal Layer Usage Offset-Via Assignment	4085	3497	3231	3059	1.51

Routing Algorithm Comparison

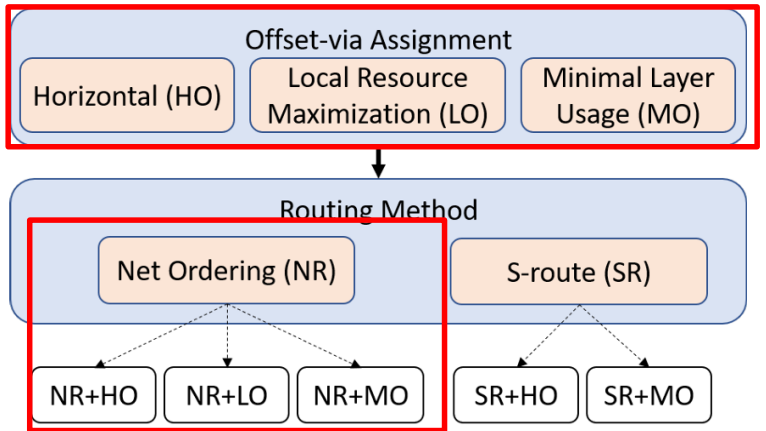
- Comparison of routing algorithms with horizontal offset-via assignment
- NR+HO
  - Uses the net order approach proposed by [2]
  - [2] do not incorporate the offset-via technique, we use horizontal offset-via to preserve routing resources
  - NR needs to change the routing order iteratively, making the run time longer than S-route
- SR+HO
  - S-route can design the direction and guide each net onto its designated channel
  - Reduce at least one RDL for the first two circuits



	Method	Circuit 1	Circuit 2	Circuit 3	Circuit 4	
Average Wire Length(um)	NR+HO[2]*	1071.8	870.2	1651.4	1166.9	1.02
	SR+HO	1054.9	845.5	1613.7	1162.4	1
# Layers	NR+HO[2]*	5	5	6	5	1.17
	SR+HO	4	3	6	5	1
Run Time (s)	NR+HO[2]*	37.6	30.9	239.1	30.6	845.6
	SR+HO	<0.1	<0.1	<0.1	<0.1	1

Offset-Via Structure Comparison

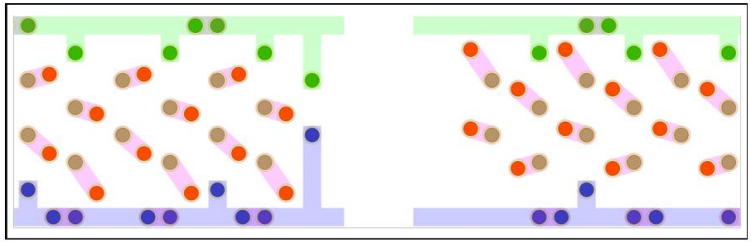
- Comparison of different offset-via assignments with the same routing method
- NR+LO
  - Reduce one RDL layer in Circuit 2
  - Optimized the routing resource by rotating the offset-via
  - LO makes the routing net take a longer path around the offset-via
- NR+MO
  - Carefully assigned channel, we can achieve a shorter net wire length
  - Easier to cross other channels using the NR method
  - The number of layers remains the same as in NR+LO



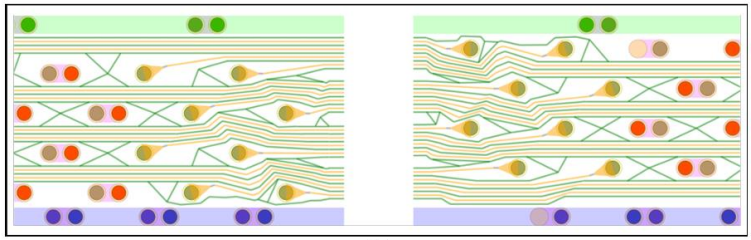
	Method	Circuit 1	Circuit 2	Circuit 3	Circuit 4	
Average Wire Length (um)	NR+HO[2]*	1071.8	870.2	1651.4	1166.9	1.03
	NR+LO	1144.1	942.9	1641.6	1199.1	1.07
	NR+MO	1057.9	830.3	1575	1153.1	1
#Layers	NR+HO[2]*	5	5	6	5	1.05
	NR+LO	5	4	6	5	1
	NR+MO	5	4	6	5	1
Run Time (s)	NR+HO[2]*	37.6	30.9	239.1	30.6	3.34
	NR+LO	90.1	35.6	218.1	54.8	3.93
	NR+MO	35.51	4.74	55.47	5.59	1

Final Result Comparison

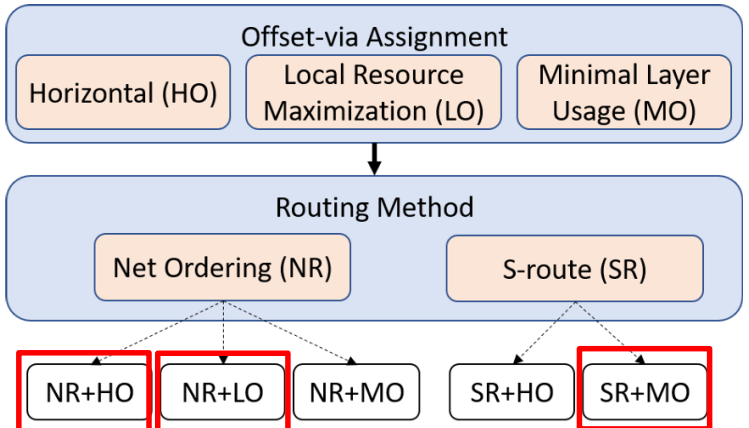
- Comparison of final results that integrate all approaches we propose
- Figure a shows part of MO result in the first layer
  - Find a suitable position for offset-via on the first layer
  - increase the routing resources for the remaining layers
- Figure b shows part of the SR result in the second layer
  - Guide the nets route on their designated channel
  - Benefit from average wire length, number of layers, and run time
- SR+MO method
  - Can reduce 7% wire length and 50% RDL layer usage



(a)



(b)



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	NR+LO	1144.1	942.9	1641.6	1199.1	1.1
	SR+MO	1014.4	815.2	1523.7	1111.4	1
# Layers	NR+HO[2]*	5	5	6	5	1.5
	NR+LO	5	4	6	5	1.43
	SR+MO	3	3	4	4	1
Run Time (s)	NR+HO[2]*	37.64	30.9	239.1	30.6	845.6
	NR+LO	90.1	35.6	218.1	54.8	996.5
	SR+MO	<0.1	<0.1	<0.1	<0.1	1

Routing Result in SI Effectiveness

- Comparison of signal integrity results in circuit 3
- NR+LO
  - The Eye Height/Width has improved by 4.7% and 1.3% in the method
  - More detours in the routing, which makes the routed signal discrete
  - The spacing between signal and ground nets will not be preserved as 2um
- SR+MO
  - Better utilize the routing region and reduce two routing layers
  - Making the nets more dense in each layer
  - The Eye Height/Width has a slight decrease with 0.2% and 0.13%
- SR+MO without shielding
  - The Eye Height/Width significantly reduced by 9.8% and 2.6%

	Ideal 2um spacing Fully Shielding	NR+LO	SR+MO	SR+MO Without Shielding
Average Eye Width (v)	0.721	0.755 (+4.7%)	0.719 (-0.2%)	0.65 (-9.8%)
Average Eye Height (ps)	151	152.95 (+1.3%)	150.8 (-0.13%)	147.04 (-2.6%)

Minimal Layer Usage Offset-Via Discussion

- Routing in first layer
  - The wire length in the first layer is approximately 10% longer than the average wire length
  - Reduces the layer count in circuit 4
- We observe the trade-off in the result with/without having routes in the first layer

	Layer	Routed nets (Average length)				Layer Usage (Average length)
		1	2	3	4	
W/o route on layer-1	Circuit 1	X	24 (1018.0)	24 (1010.7)	-	3 (1014.4)
	Circuit 2	X	24 (817.5)	12 (810.5)	-	3 (815.2)
	Circuit 3	X	16 (1523.4)	16 (1523.4)	16 (1523.4)	4 (1523.7)
	Circuit 4	X	16 (1111.5)	16 (1111.2)	4 (1112.0)	4 (1111.4)
W/ route on layer-1	Circuit 1	6 (1132.9) (+10.1%)	24 (1018.7)	18 (1008.2)	-	3 (1028.7)
	Circuit 2	6 (903.9) (+9.1%)	24 (814.5)	6 (810.8)	-	3 (828.8)
	Circuit 3	4 (1679.9) (+9.4%)	16 (1522.9)	16 (1523.1)	12 (1522.7)	4 (1536.0)
	Circuit 4	4 (1287.5) (+13.8%)	16 (1111.2)	16 (1111.6)	-	3 (1131.0)

Conclusion

- Serious routing resource issue in die-to-die routing problem
  - Apply offset-via and teardrop
  - Consider signal integrity with fully shielding
- Minimal Layer Usage offset-via assignment
  - Maximize the routing resources of the entire RDL layer
- S-route Pattern
  - Reduce routing track, detour, wire length
- According to the experimental results
  - **S-route Pattern only:**
    Already get an improvement in the average wire length
  - **With Minimal Layer Usage offset-via assignment:**
    Significantly reduce the number of RDL layers used

Thanks for Listening