LIBMixer: An all-MLP Architecture for Cell Library Characterization towards Design Space Optimization

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Jaeseung Lee, Sunggyu Jang, Jakang Lee, and Seokhyeong Kang

CONTACT

Pohang University of Science and Technology
Department of Electrical Engineering
CAD and SoC Design Lab.
Tel. +82-54-279-2883
Web. http://csdl.postech.ac.kr

Outline

I. Introduction

II. Proposed Method

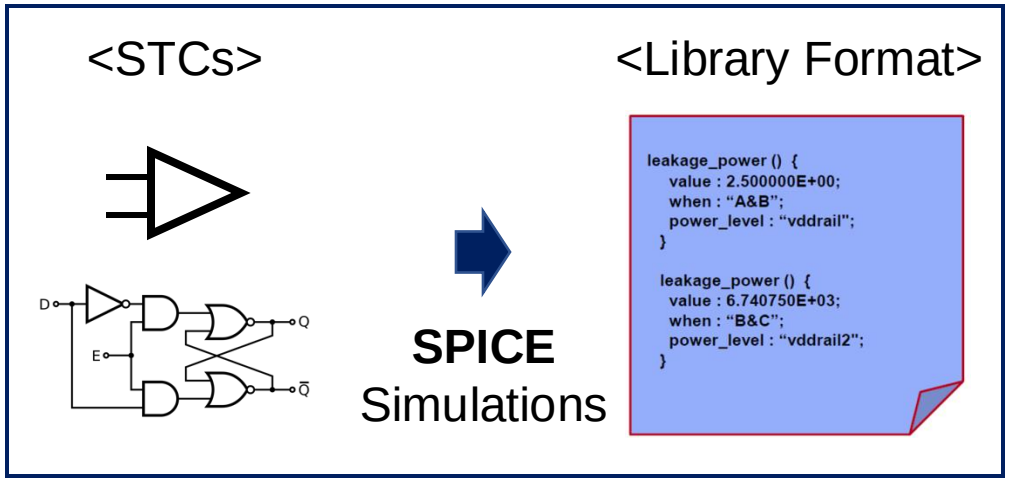
III. Experimental Setup and Results

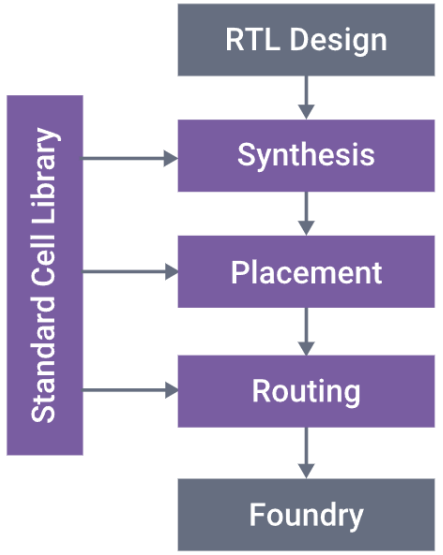
IV. Conclusion

* Appendix.

Cell Library Characterization in Modern EDA

- **Cell library characterization**
  - Determining **electrical characteristics** of standard cells (STCs)
    - With ***SPICE*** simulation: rise and fall delay, power consumption
  - NLDM (LUT), CCS, Several Format **(.lib)**
  - Predefined libraries are processed by the various **tools in the EDA flow** [1]
    - Synthesis
    - PnR
    - Verification



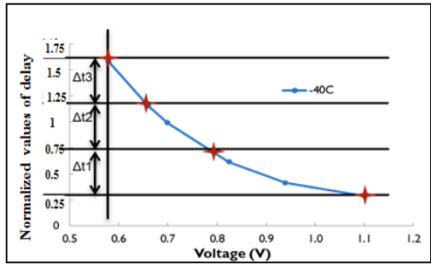


[1] Synopsys Glossary, "What is Library Characterization?"

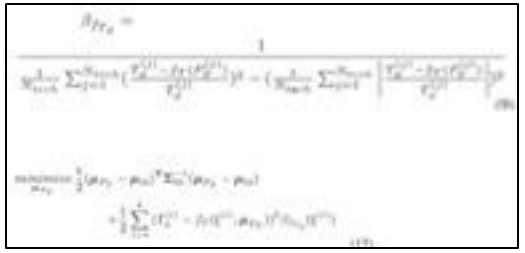
Previous Works and Limitations

- **How to handle growing complexity in advanced nodes due to**
  - **Increasingly expensive** in computational costs & engineering effort
  - Growing complexity of MOSFET, varied behavior scenarios
- Previous approaches
  - Offers advantages in **addressing challenges**
  - But mostly targeted **gate-level view & only for small, simple STCs**

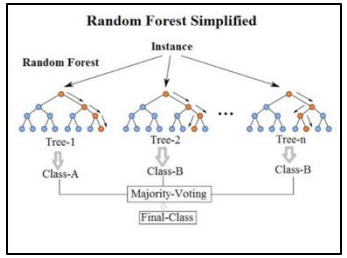
→ Lack of **comprehensive studies** related to **EDA tools and DSO applications**



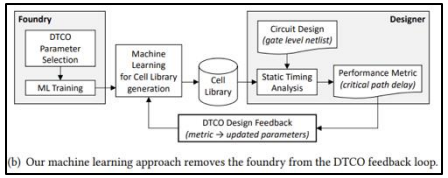
Curve Fitting [2]



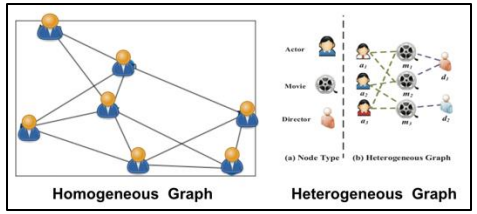
Numerical Analysis [3]



Random Forest [4]



Linear regression [5]



Heterogeneous GNN [6]

[2] K. Charafeddine and F. Ouardi, “Fast timing characterization of cells in standard cell library design based on curve fitting,” Proc. WITS, 2017.
[3] L. Yu et al., “Statistical library characterization using belief propagation across multiple technology nodes,” Proc. DATE, 2015.
[4] G. Jacinto et al., “Fast and Low-Error Prediction of Logic Gate Cell Characterization,” Proc. ICECS, 2023.
[5] F. Klemme et al., “Cell Library Characterization using Machine Learning for Design Technology Co-Optimization,” Proc. ICCAD, 2020.
[6] X. Cheng et al., “Heterogeneous Graph Attention Network Based Statistical Timing Library Characterization with Parasitic RC Reduction,” Proc. ASP-DAC, 2024.

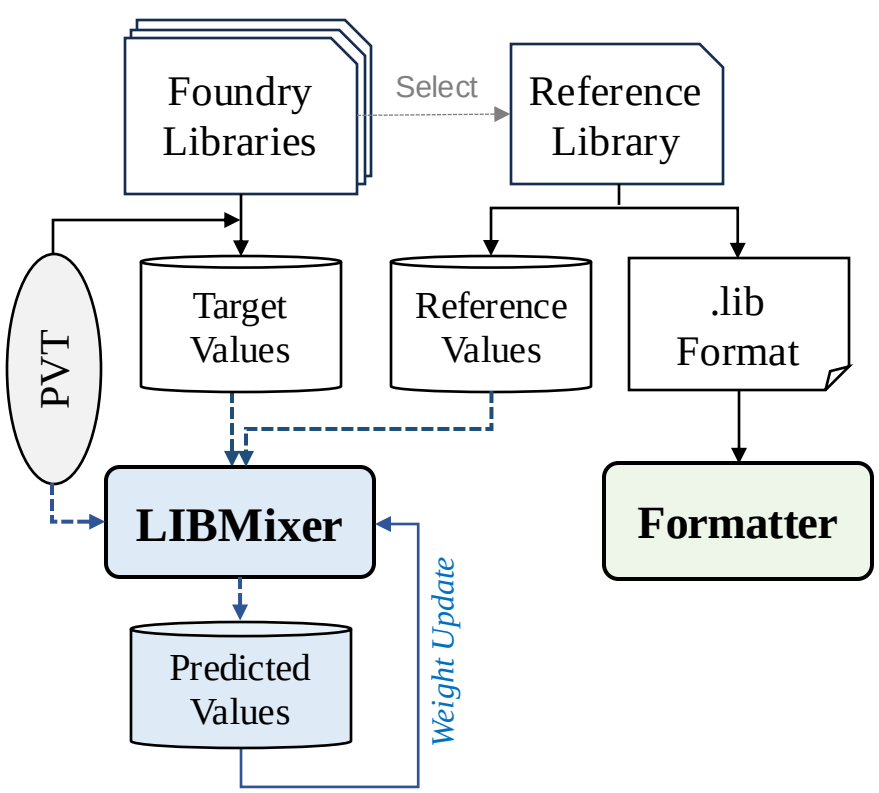
Research Target

- **Our research focus on**
  - Decreasing the **problem complexity** **of characterization**
  - Expanding the scope to include **complex STCs**

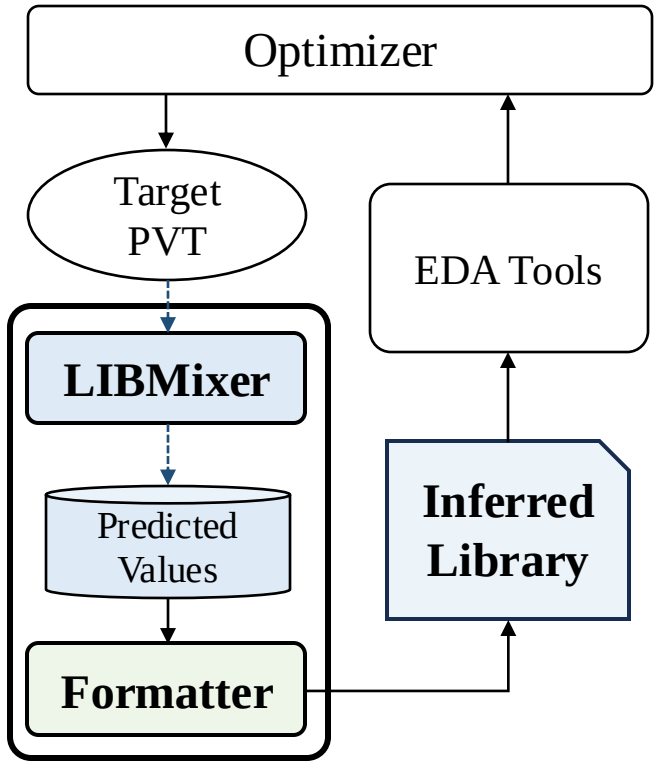
- **DSO approach → PVT Analysis**
  - **Evaluates circuit across** various manufacturing process variations (P), supply voltage fluctuations (V), and operating temperature ranges (T)
  - Ensures **robustness** and **reliability** under diverse conditions

Overall Framework

- (a) The **training stage** and (b) the **DSO stage**



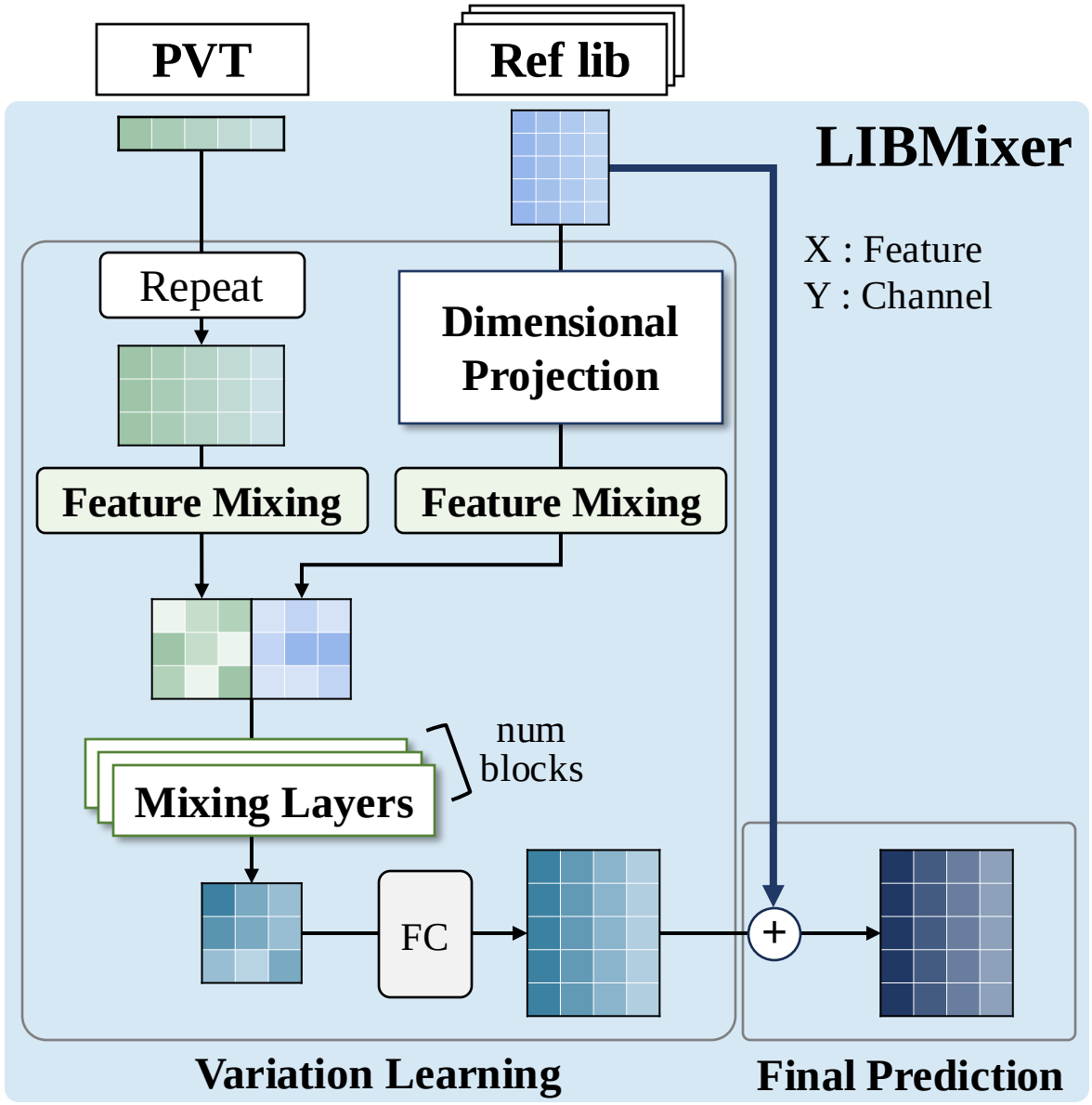
(a) Training Stage



(b) DSO Stage

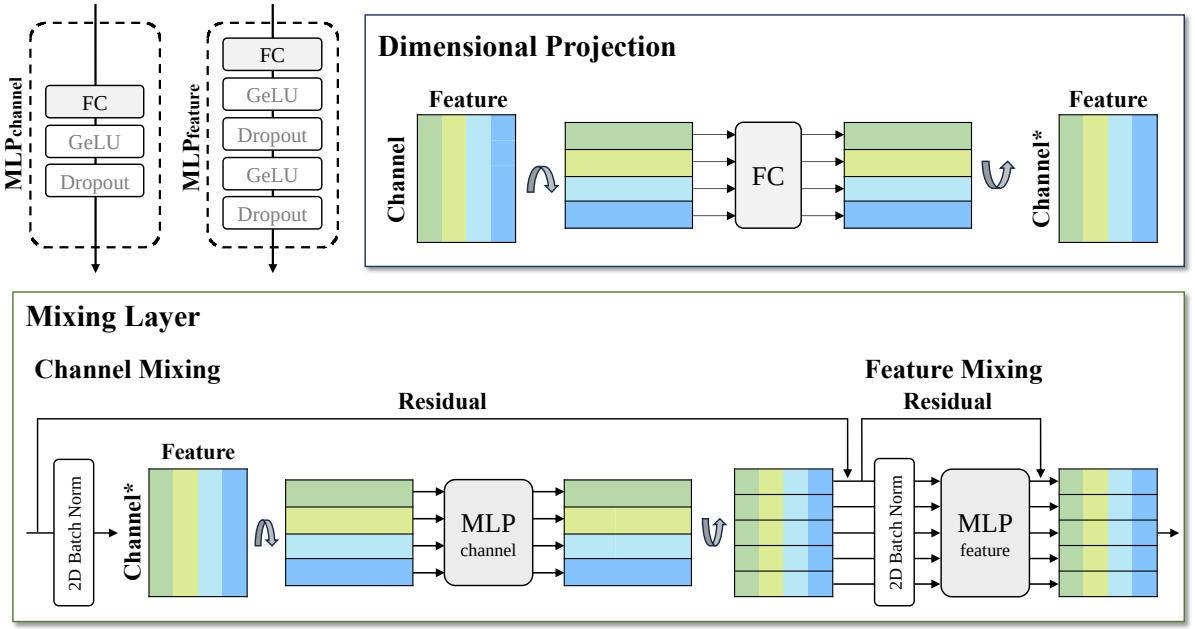
- **LIBMixer**
  - ML-based model
  - Predict **library values** for **target PVT** conditions
- **Formatter**
  - Construct library file **formats (.lib)** based on prediction

Architecture of LIBMixer



- **Input**
  - PVT & library parameter
    - Process, voltage, temperature, index of STC set
  - Reference library table (foundry given)
- **Output**
  - Inferred library table for given PVT
    - Variation learning from reference

Architecture of LIBMixer – Mixer layer

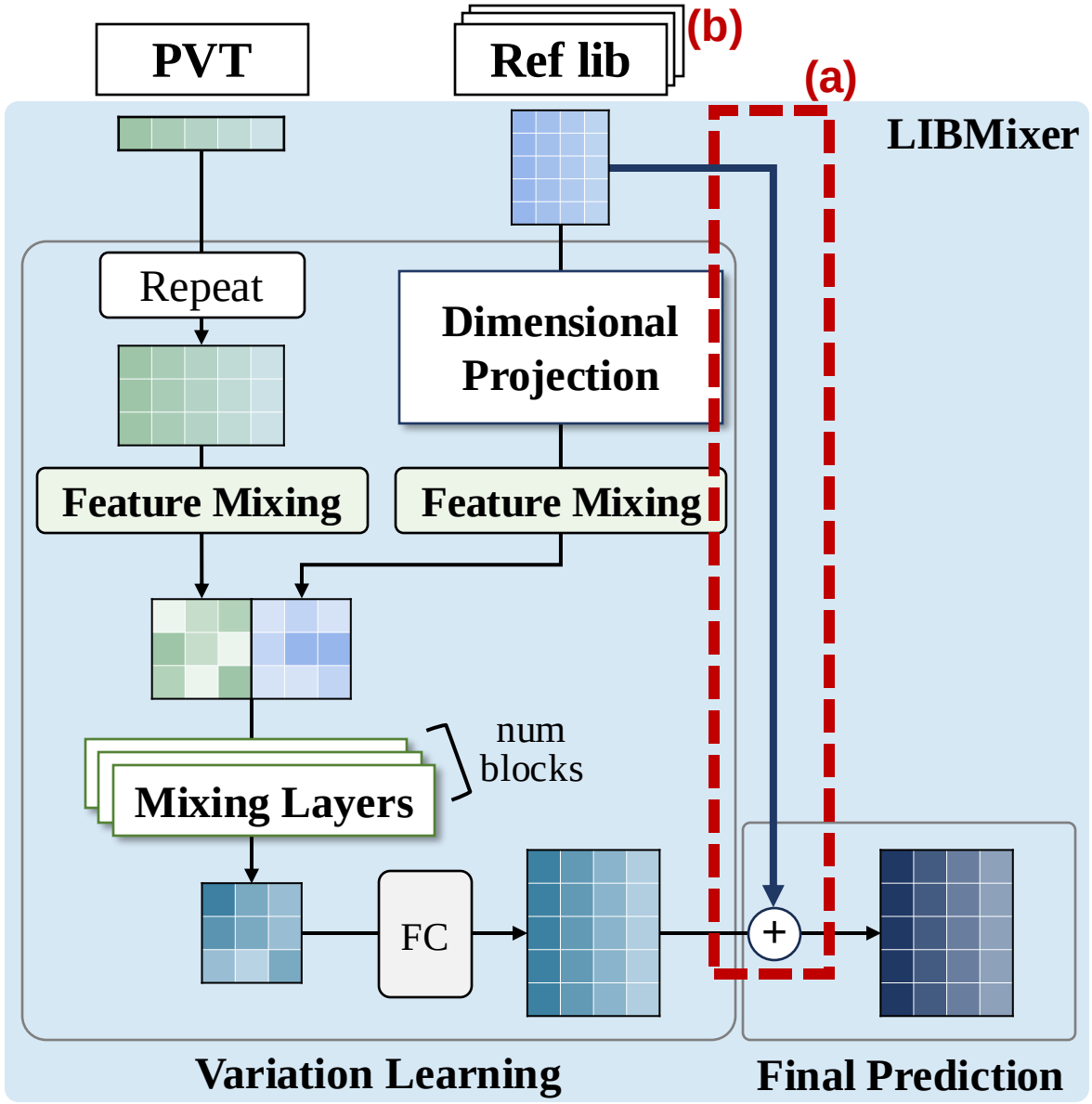


- **Concept**
  - Apply MLPs across two dimensions in an **alternating manner** [7]
- **Defined dimension for library data**
  - **Feature Mixing** layer consider **characteristics** in library tables
  - **Channel Mixing** layer learns the change according to **design conditions**
  - **Mixing Layers** =

    Feature Mixing + Channel Mixing

[7] O.Tolstikhin et al., “Mlp-mixer: An all-mlp architecture for vision,” Proc. NeurIIPS, 2021.

Key structural modifications



(a) Additional residual connection

- Between the output of the variation layer & reference library
- **Match** input dimension = output dimension

(b) Data shape

- To manage the **various shape** of library tables, **LIBMixer** distinguishes them based on their dimensions
  - Dynamic power (2D), leakage power (1D), timing (2D), Area (0D)

Experimental Setup

- **Workstation & implementation**
  - CentOS Linux 7.9 with 2.8 GHz AMD EPYC 7402P CPU and 256 GB RAM, along with an NVIDIA Titan RTX GPU
  - The library dataset was generated by employing the BSIM-CMG [8] model and *Synopsys SiliconSmart [9]*
    - Consider **physical and parasitic** effects, avoid **potential challenges** in advanced nodes (random dopant fluctuation and the gate fringing capacitance)

- **Physical synthesis**
  - Generated using the Synopsys Library Compiler [10] and Synopsys Design Compiler [11]
- **Target designs**
  - OpenCores [12] and RocketChip [13]

The specifications of the circuit designs

Designs	Technology	Clock	# Cells	Design Time [sec]
ibex	*7-nm*	2,500	15K	80
des3		1,000	60K	120
swerv		600	61K	400
ldpc		1,000	42k	1000
rocket core		600	700k	9000

[8] S. Khandelwal et al., "BSIM-CMG 110.0.0: Multi-gate MOSFET compact model: technical manual," 2014.
[9] Synopsys Inc, "SiliconSmart ACE 2021," in Software, 2021.
[10] Synopsys Inc, "Library Compiler 2018," in Software, 2018.
[11] Synopsys Inc, "Design Compiler 2018," in Software, 2018.
[12] OpenCores: "Open Source IP-Cores," http://www.opencores.org.
[13] A. Krste et al., "The rocket chip generator," EECS Department, University of California, Berkeley, Tech., 2016

Dataset & DSO parameters

- To ensure wide application to EDA tools, we selected **198 cells** of the *ASAP7 PDK**
  - Previous methods targeted 31 cells **(6.4×)** and simple STCs

- Considered **PVT corners** are to cover **extreme conditions** of the selected PDK [14]

Symbol	Unit	Min	Max	Step	# of comb.
Φ_g	eV	4.250	4.450	0.005	41
V_{dd}	V	0.55	0.75	0.05	5
T	℃	[-50, 0, 25, 75, 125]			5
Total number of combinations: 1025					
(Train : Validation : Inference = 800 : 180 : 45)					

Φ_g: gate work function of finFet, V_{dd} : Supply voltage, T: Temperature

- **Models for comparison**
  - Ridge+: Revised ML model to handle system-level library characterization from **Ridge[15]**

Name	Ridge [15]	Ridge+	Ours
Base Model	Ridge Regression	Ridge Regression	Mixer
Norm.	Linear Min-max	Log	Log
Residual	No	Yes	Yes

[14] L. Clark et al., "ASAP7: A 7-nm finFET predictive process design kit," Proc. Microelectronics Journal, 2016.
[15] F. Klemme et al., "Cell Library Characterization using Machine Learning for Design Technology Co-Optimization," Proc. ICCAD, 2020.

Experiment Steps

LIBMixer based Library Characterization

Synthesis PPA result with LIBMixer inferred library

DSO & Faster PVT analysis

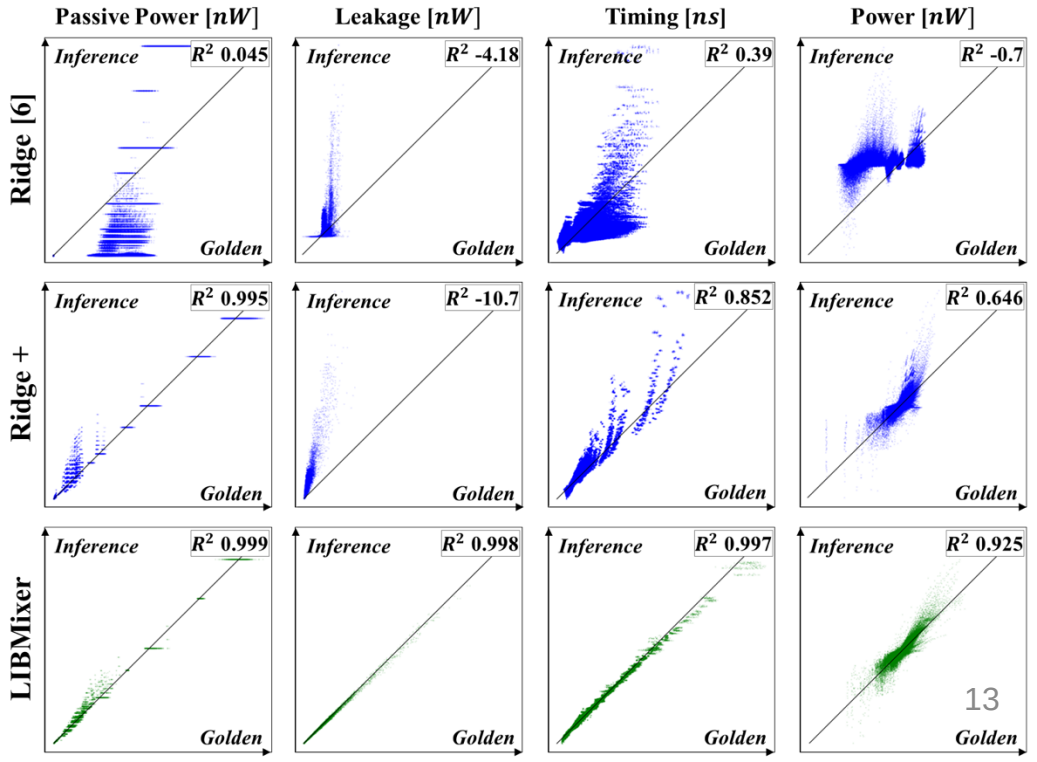
Accuracy of ML-inferred libraries?

Compatibility with conventional EDA tool?

Faster Optimization?

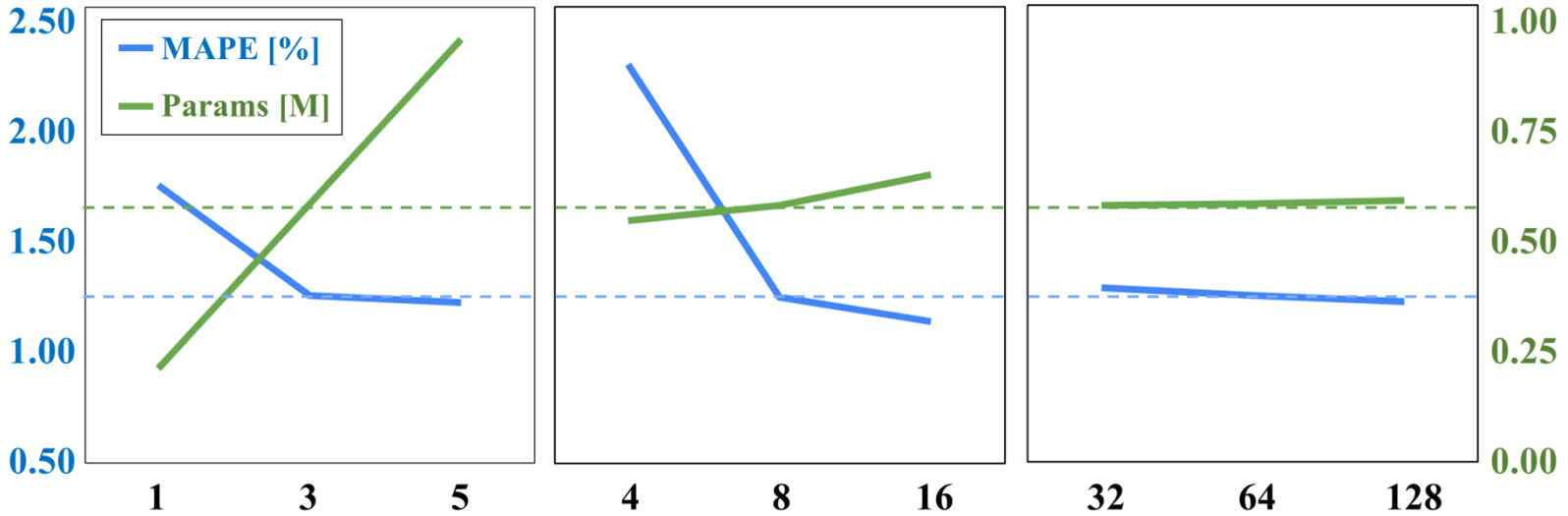
Exp 1. Accuracy of ML-inferred libraries?

- Evaluate the performance of LIBMixer in **predicting library values**
- **Results**
  - **Test error was smallest** than other ML-based method
    - MAE: Ridge (1.0x) > Ridge+ (0.28x) > **LIBMixer (0.04x)**
    - MAPE: Ridge (0%) >> Ridge+ (-3.85%) > **LIBMixer (-4.52%)**
  - **Runtime** of library generation was **similar**
    - Ridge (27.35s) = Ridge+ (27.71s)= LIBMixer (27.73s)
      << Conventional tool (7200s)
    - Because of bottleneck in library file writing
  - **Training error** was not that different
    - Ridge(1.0x) > Ridge+(0.90x) > LIBMixer (0.57x)



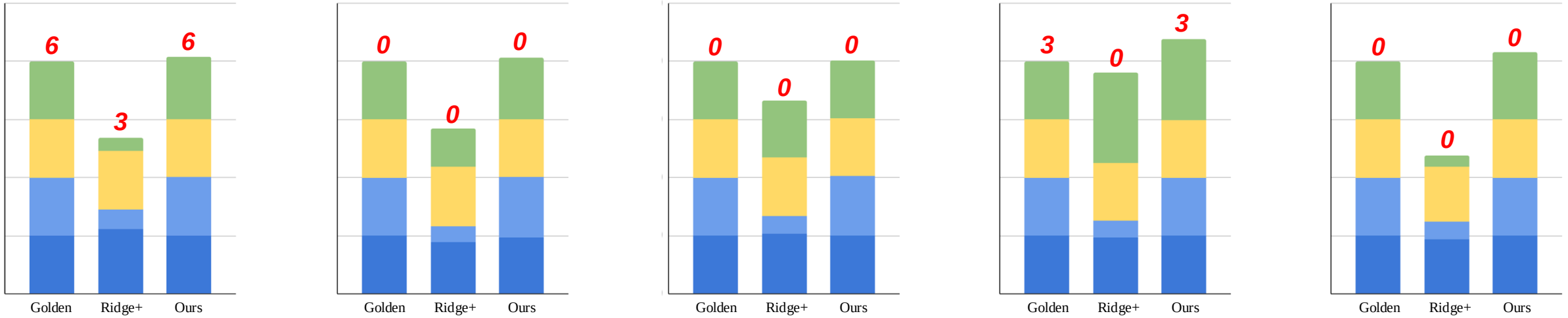
Exp 1a. Ablation Study of LIBMixer

- Regarding structural parameters, including the **number of mixer blocks**, the **size of hidden channels**, and **hidden features, showing performance**
- **Results**
  - In general, each **hyperparameter** ↑ led to **model parameters** ↑ **, error** ↓
  - Important model characteristic - ***num blocks***
    - Improvement becomes negligible after **3 blocks** due to the residual connection of Mixing-layer
    - Prevents **overfitting** and ignores unnecessary operations



Exp 2. Compatibility with conventional EDA tool?

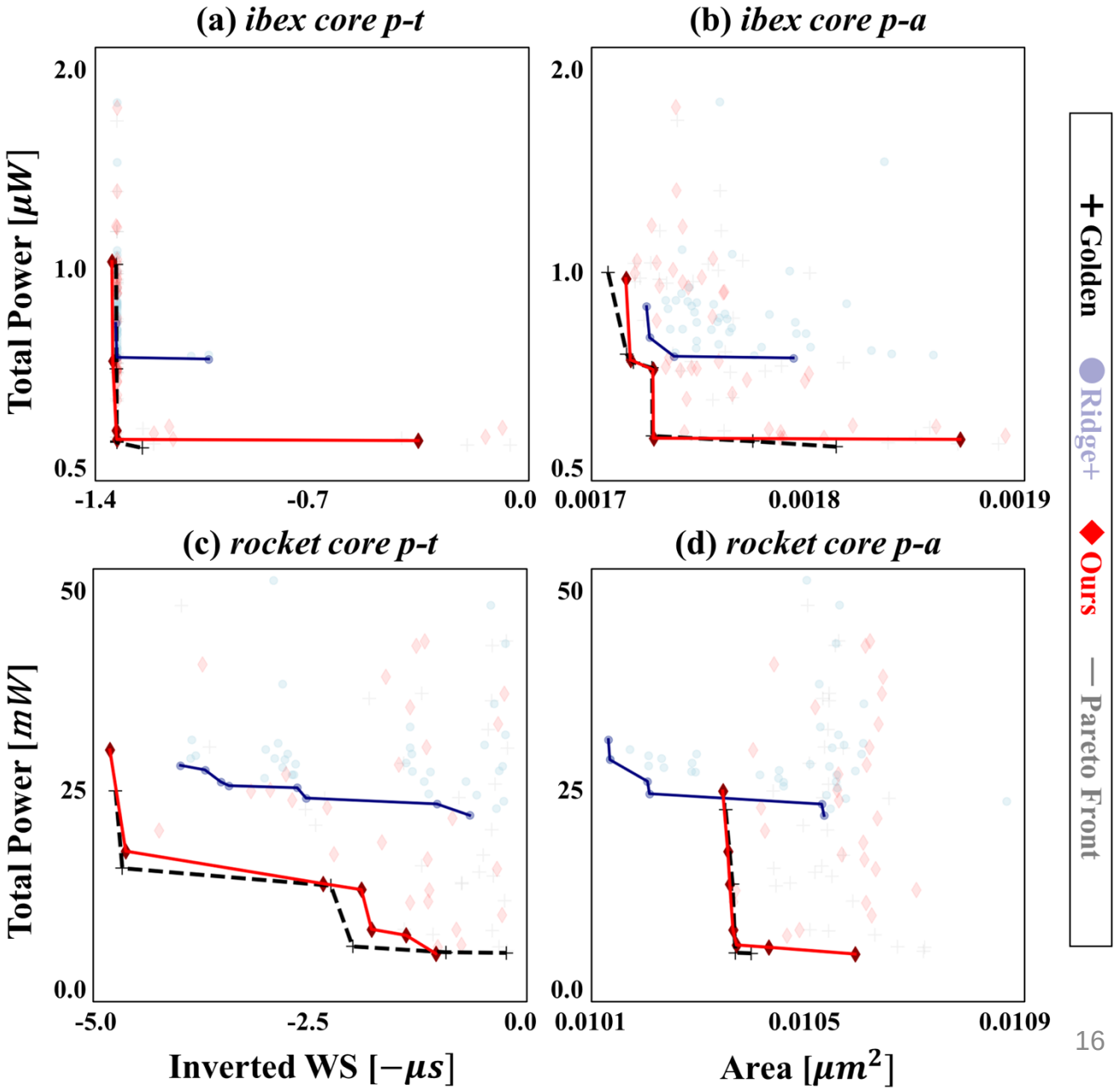
- Evaluate PPA similarity using LIBMixer inferred libraries **applied to the EDA tool** (post-synthesis)
- **Results**
  - Demonstrate the **same violation PVT cases** as foundry libraries
    - For every benchmarks, same PVT violation
  - Achieving **high accuracy** in evaluation metrics: Dynamic power, leakage power, area



Ratio of PPA outcomes. Every golden value of each benchmark and each metric is set 1.0
# of violated corners are highlighted in ***N***

Exp 3. Design Space Optimization

- **Power-area** and **power-timing** Pareto fronts of two designs
  - (a) *ibex core*, (b) *rocket core*
- Design results with LIBMixer inferred library **show close Pareto fronts** to those of using the foundry library
- **Usages of ML-based library characterization in PVT analysis and DSO**



Conclusion

- We introduce the efficient **ML-based framework** for accurate library characterization named **LIBMixer**
  - **LIBMixer** efficiently generates **a wide range of standard cells** based on **only PVT information**, covering all **essential data** including timing and power
- We demonstrate the **compatibility of libraries** inferred by LIBMixer with conventional EDA tools
  - We reveal a **strong correlation** between design outcomes obtained from inferred libraries and those from foundry libraries
- We highlight that the **Pareto fronts** of synthesis design results using LIBMixer-inferred libraries correspond well to those from foundry files
  - The LIBMixer-inferred library serves as a **swift foundation** for **PVT analysis**

Appendix A. Target STCs

- we selected **198 cells** of the *ASAP7 PDK**

Table 2: Target standard cells

Types	# of Cells	Prefix	Sizes
AO	42	AO2	1x1/2, 11x2, 2x1/2, 21x1/2, 22x2
		AO3	1x2, 2x1/2, 22x2, 3x2, 31x1/2, 32x1/2, 33x1/2
		AOI2	1x1/xp33/xp5, 11x1/xp5, 2xp5/33, 21x1/xp5, 22xp33/x1
		AOI3	1/11/2/21/22/3/31/32/33xp33, 1xp67
		Others	A2O1A1Ixp33 A2O1A1O1Ixp25
INVBUF	37	BUF	x2/3/4/4f/5/6f/8/10/12/12f/16f/24 / HB1/2/3/4xp67
		CKINVDC	x5p33/6p67/8/9p33/10/11/12/14/16/20
		INV	x1/2/3/4/5/6/8/11/p33/p67
OA	34	OA2	1x2, 11x2, 2x2, 21x2, 22x2
		OA3	1x2, 3x2, 31x1/2, 32x1/2, 33x1/2
		OAI2	1x1/p5/p33, 11xp5, 2x1/p5/p33, 21xp5, 22xp33
		OAI3	1/11/2/21/22/3/31/32/33xp33, 1xp67
		Others	O2A1O1Ixp33/p5
SEQ	33	D F/F	DFFASRHQNx1, DFFHQNx1/2/3/4 DFFLQNx1/2/3/4
		D Latch	DHLx1/2/3 DLLx1/2/3
		ICG	x1/2/2p67DC/3/4/4DC/5/5p33DC/6p67DC/8DC
		Scan D F/F	SDFHx1/2/3/4 SDFLx1/2/3/4
SIMPLE	52	AND	2x2/4/6, 3x1/2/4, 4x1/2, 5x1/2
		NAND	2x1/1p5/2/p33/p5/p67, 3x1/2/p33, 4xp25/p75, 5xp2
		NOR	2x1/1p5/2/p33/p67, 3x1/2/p25/p33/p75, 5xp2
		OR	2x2/4/6, 3x1/2/4, 4x1/2, 5x1/2
		Others	XNOR2x1/2/5 MAJIx2/3/p5 XOR2x1/2/p5
Total	**198**		

Appendix C. Experiment 1

- Comparative analysis with state-of-the-art machine learning-based library characterization

Table 5: Comparative analysis with state-of-the-art machine learning-based library characterization

Metric	Golden	Passive Power [nW]			Leakage [nW]			Timing [ns]			Power [nW]		
		Ridge [6]	Ridge+	Ours	Ridge [6]	Ridge+	Ours	Ridge [6]	Ridge+	Ours	Ridge [6]	Ridge+	Ours
Train MSE	0.00E+00	3.20E-04	3.13E-04	2.27E-04	2.33E-03	2.25E-03	2.04E-03	31.0E-04	14.7E-04	7.40E-04	3.70E-03	4.40E-03	1.69E-03
MAE	0.00E+00	7.54E+00	8.03E-02	**3.39E-02**	3.11E+04	1.89E+04	**8.76E+02**	5.77E+01	2.07E+01	**3.25E+00**	1.06E+00	1.71E-01	**6.75E-02**
MAPE [%]	0.00	7.05	1.19	**0.69**	1.14	1.33	**0.05**	1.77	0.24	**0.11**	10.39	2.18	**1.42**
R2	1.000	0.0449	0.9945	**0.9989**	-4.180	-10.704	**0.9980**	0.3870	0.8516	**0.9967**	-0.078	0.6465	**0.9253**
Runtime	3,500 ±1,000	27.346	27.313	27.645	27.736	27.713	27.682	27.363	27.761	27.824	27.359	27.723	27.784

The best results are highlighted in **bold** for each metric.

Appendix D. Experiment 2

- Logic synthesis results for power, worst slack, and area

Bench	Metric	Dynamic Power [μW]				Leakage Power [μW]				Area [μm^2]			
		Golden	Ridge [6]	Ridge+	Ours	Golden	Ridge [6]	Ridge+	Ours	Golden	Ridge [6]	Ridge+	Ours
ibex core	Mean	927.63	169003.26	1031.60	**928.77**	148.53	831.53	50.81	**149.59**	1783.68	3085.92	1785.85	**1780.65**
	MAE	-	168075.63	928.77	**21.12**	-	683.00	149.59	**2.90**	-	1302.24	1780.65	**9.79**
	SE	-	2132.80	36.07	**2.86**	-	99.38	65.39	**1.45**	-	60.26	4.55	**1.29**
	MAPE [%]	-	19200.75	24.54	**2.41**	-	6764624.63	40562.65	**3.00**	-	73.06	1.32	**0.54**
des3	Mean	17897.06	1751695.45	15827.31	**17293.59**	625.12	3619.58	174.39	**653.33**	6409.15	10446.89	6579.95	**6410.06**
	MAE	-	1733798.40	17293.59	**1873.02**	-	2994.46	653.33	**29.05**	-	4037.74	6410.06	**22.33**
	SE	-	32682.81	1086.28	**215.12**	-	432.40	288.00	**16.50**	-	97.06	4.90	**3.54**
	MAPE [%]	-	10299.34	18.87	**11.59**	-	2395032.52	30837.54	**5.51**	-	63.00	3.87	**0.35**
swerv	Mean	2482.21	601281.04	2557.43	**2490.78**	1025.84	4298.87	320.84	**1045.04**	12069.23	20684.03	**12065.36**	12047.40
	MAE	-	598798.83	2490.78	**168.44**	-	3290.91	1045.04	**28.13**	-	8614.80	12047.40	**32.78**
	SE	-	7927.94	130.68	**26.82**	-	508.11	459.57	**14.89**	-	607.79	**2.98**	3.98
	MAPE [%]	-	25845.50	8.38	**6.66**	-	380102.68	18730.34	**2.70**	-	71.35	**0.26**	0.27
ldpc	Mean	8240.45	429495.68	7718.25	**8233.07**	611.29	1281.80	189.33	**613.09**	5687.79	7252.59	5390.50	**5731.26**
	MAE	-	421255.22	1008.72	**820.08**	-	964.44	423.53	**11.14**	-	1601.17	339.82	**91.38**
	SE	-	7577.89	**132.52**	158.01	-	145.17	189.48	**4.96**	-	173.69	34.36	**18.81**
	MAPE [%]	-	5643.57	15.28	**9.95**	-	328164.90	23076.28	**4.43**	-	28.51	5.91	**1.60**
rocket core	Mean	32518.45	4364300.00	31529.97	**32438.07**	10538.28	25188.10	3100.36	**10470.62**	105738.26	143488.95	104766.97	**105678.41**
	MAE	-	4331781.55	11680.01	**1215.61**	-	18789.08	7479.72	**255.81**	-	37750.69	1577.32	**816.01**
	SE	-	55333.70	1738.80	**203.59**	-	2656.14	3411.89	**104.60**	-	2196.57	214.71	**85.82**
	MAPE [%]	-	16602.46	39.49	**4.09**	-	2910.60	88.61	**4.43**	-	35.71	1.49	**0.77**

Metric	Worst Slack [ns]			
	Golden	Ridge [6]	Ridge+	Ours
Mean	-87.08	-6707.31	-19.59	**-92.98**
MAE	-	6620.23	92.99	**8.96**
SE	-	240.34	47.05	**3.16**
# V	6	44	3	**6**
Mean	60.44	-2233.24	39.87	**63.47**
MAE	-	2293.68	**63.47**	64.42
SE	-	80.31	12.15	**10.89**
# V	0	44	**0**	**0**
Mean	446.6	411.8	441.9	**446.7**
MAE	-	49.85	446.68	**7.02**
SE	-	4.69	3.43	**1.49**
# V	0	**0**	**0**	**0**
Mean	-8.99	-2005.18	1.64	**-10.39**
MAE	-	1996.19	11.59	**3.78**
SE	-	93.44	6.14	**1.56**
# V	3	44	0	**3**
Mean	101.49	-104.95	157.09	**142.02**
MAE	-	206.44	108.53	**62.61**
SE	-	22.76	14.66	**8.75**
# V	0	25	**0**	**0**

The best results are highlighted in bold for each metric. # V stands the number of violated designs.