PC-Opt: Partition and Conquest-based Optimizer using Multi-Agents for Complex Analog Circuits

2025.01.22

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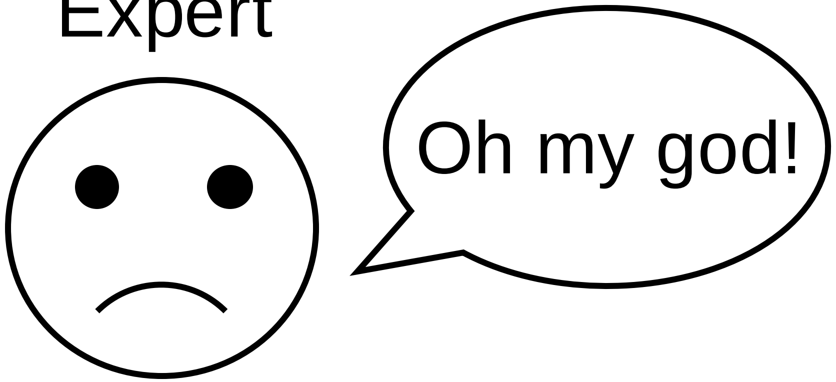
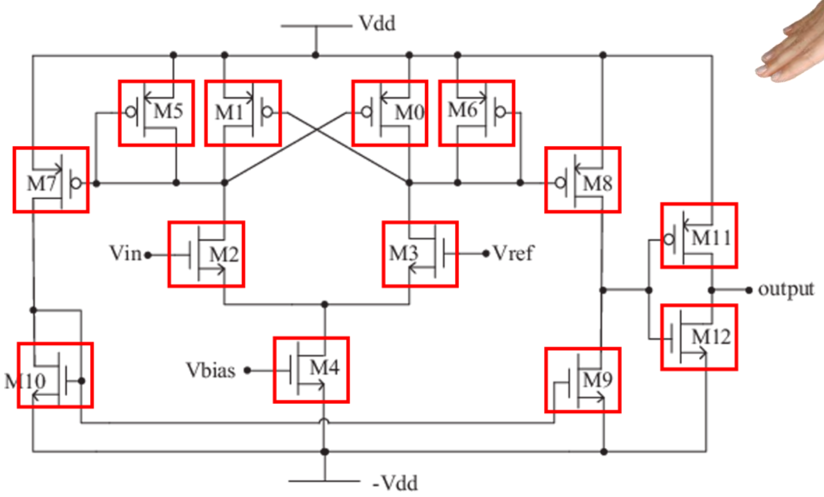
Outline

I. Introduction

- **Challenges for Analog Circuit Design**
  - Traditionally relies on human expertise

Expert



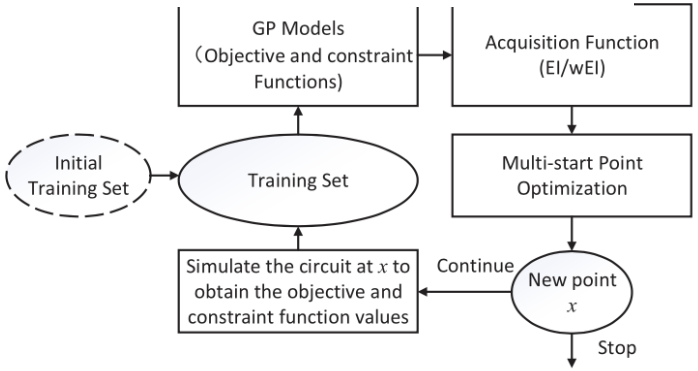


As technology of transistors becomes ***more advanced***, sizing circuits becomes ***more difficult***.

I. Introduction

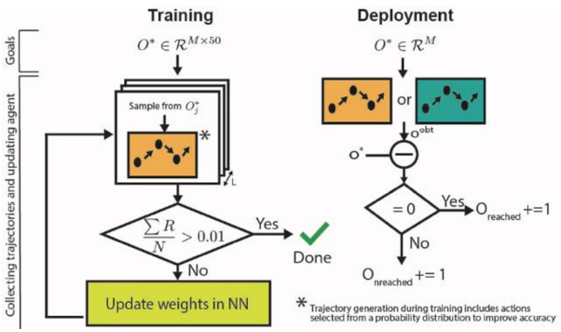
- **Application of Artificial Intelligence (AI)**
  - Application of AI to sizing AMS circuits
    - Bayesian Optimization (BO) [1]
    - Reinforcement Learning (RL) [2, 3, 4]
  - Previous research typically overlooks ***the optimization of complex analog circuits***.

Bayesian Optimization

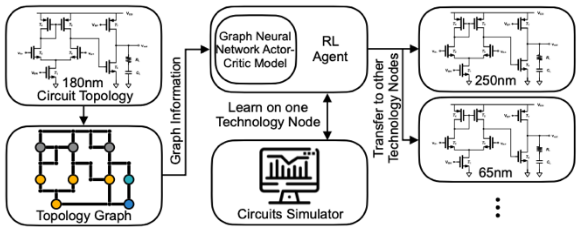


- WEIBO, TCAS-I, 2018 [1]

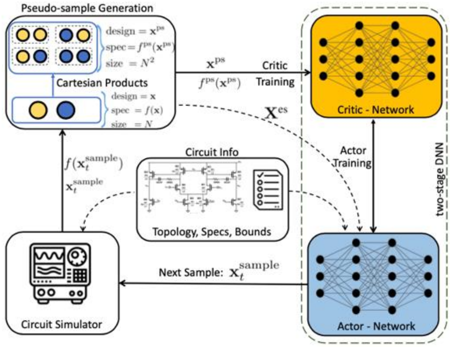
Reinforcement Learning



- AutoCkt, DATE, 2020 [2]



- GCN-RL, DAC, 2020 [3]



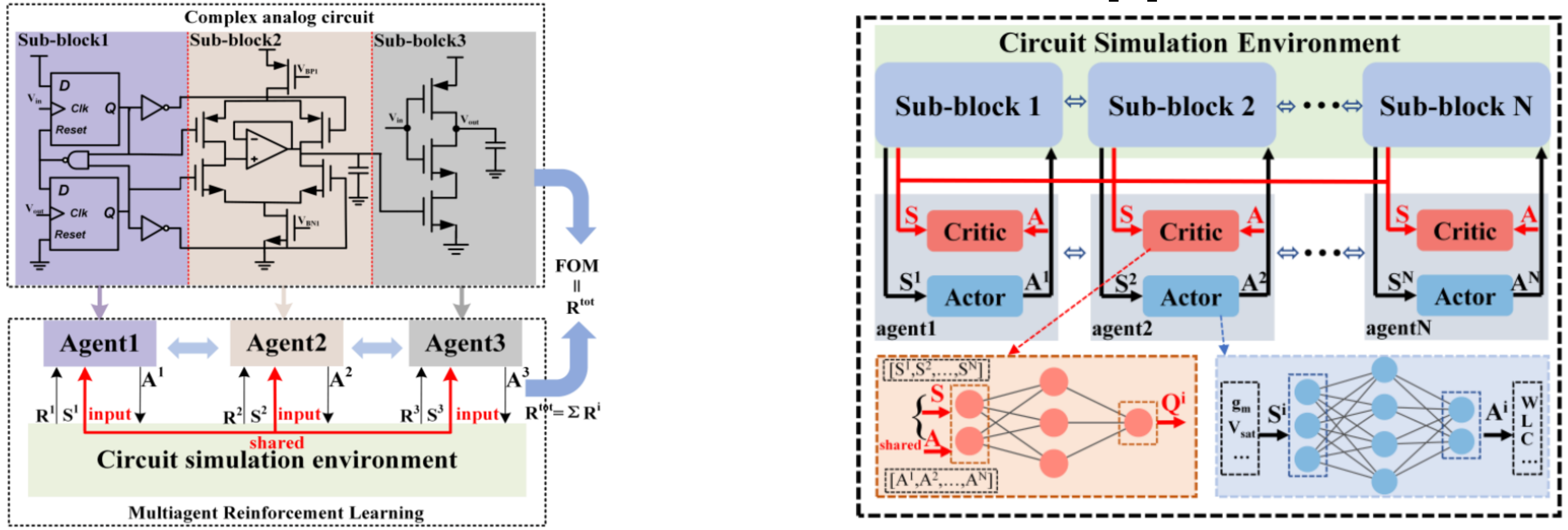
- DNN-Opt, DAC, 2021 [4]

[1] W. Lyu *et al*., “An efficient bayesian optimization approach for automated optimization of analog circuits”, TCAS-I, 2017.
[2] K. Settaluri *et al*., “Autockt: Deep reinforcement learning of analog circuit designs”, DATE, 2020.
[3] H. Wang *et al*., “Gcn-rl circuit designer: Transferable transistor sizing with graph neural networks and reinforcement learning”, DAC, 2020.
[4] C. Ding *et al*., “Dnn-opt: An RL inspired optimization for analog circuit sizing using deep neural networks”, DAC, 2021.

I. Introduction

- **Optimizing complex analog circuits**
  - Applying MADDPG framework [5] handle this issue.
    - States, actions, and rewards are shared.
    - DDPG requires extensive simulations, ***increasing overall optimization time.***

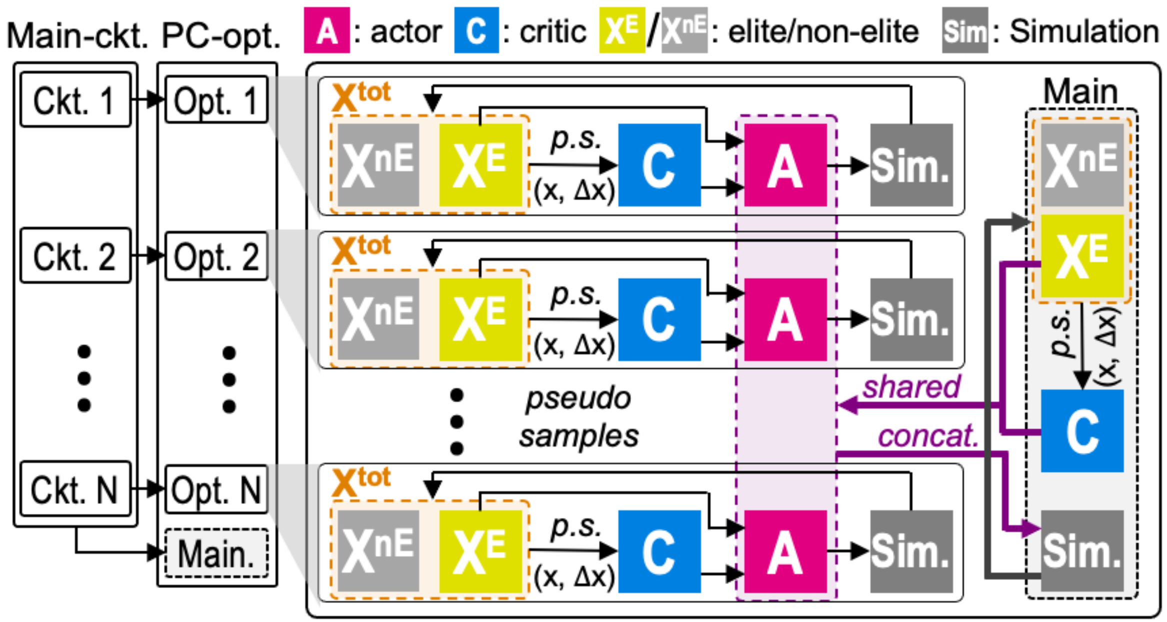
MADDPG framework, DAC, 2023 [5]



[5] Zhang et al., "Automated design of complex analog circuits with multiagent based reinforcement learning," DAC, 2023.

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **RL-inspired framework**
  - **Partition and conquer strategy**
  - **Multi-agent systems**
  - **Concentrated sampling method**

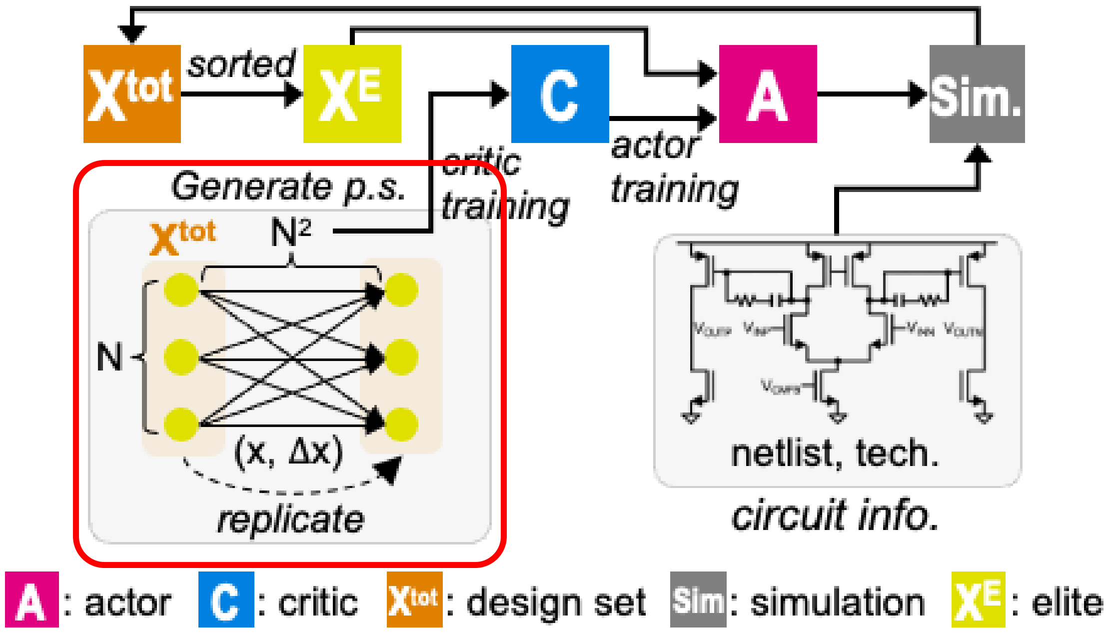


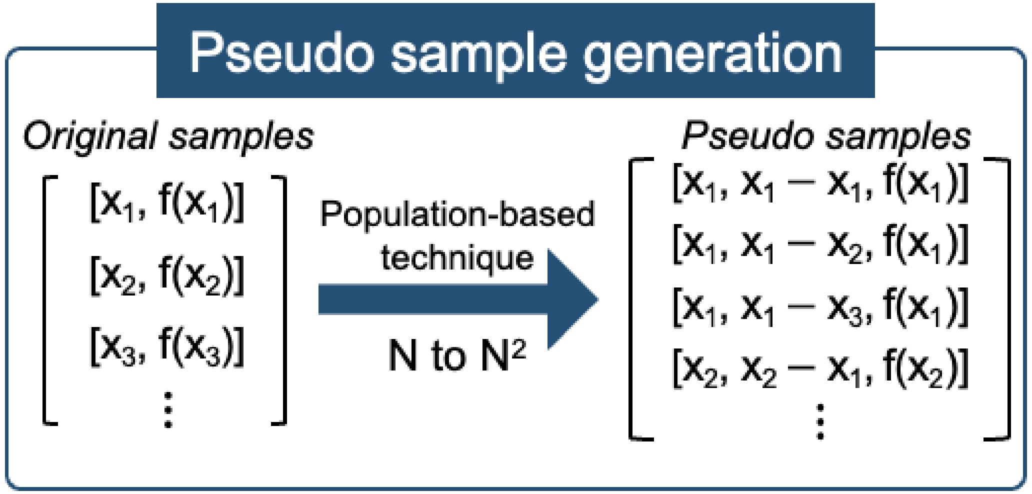
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **RL-inspired framework**
    - ***optimizes circuits within a few simulations*.**

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **RL-inspired framework [4, 6, 7]**
    - Pseudo samples are generated for critic training.





[4] C. Ding *et al*., "Dnn-opt: An RL inspired optimization for analog circuit sizing using deep neural networks", DAC, 2021.
[6] A. Budak et al., "APOSTLE: asynchronously parallel optimization for sizing analog transistors using DNN Learning," ASP-DAC, 2023.
[7] Y. Choi et al., "MA-opt: Reinforcement Learning-based analog circuit optimization using multi-actors," TCAS-I, 2023.

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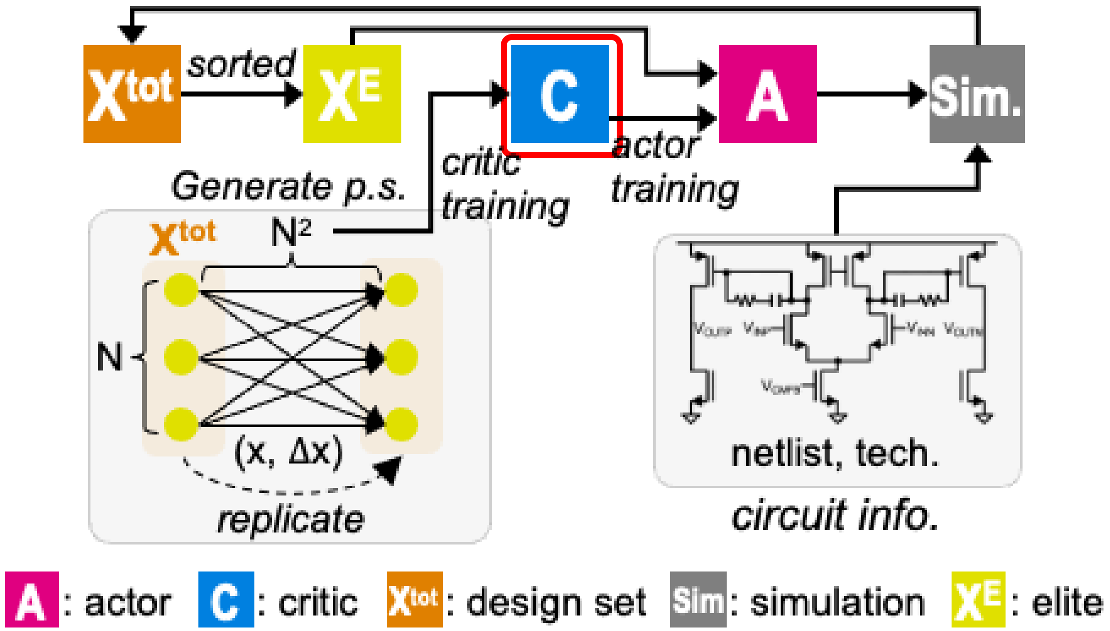

Critic network

- Mimic of a SPICE simulator
- Loss function ($L(\theta^Q)$)

$$= \frac{1}{N_b(m+1)} \sum_{k=1}^{N_b} \sum_{l=1}^{m+1} \left| \underbrace{Q(x_k, \Delta x_k)^l}_{\text{Critic network predictions}} - \underbrace{f(x_k + \Delta x_k)^l}_{\text{Simulation results}} \right|^2$$

[4] C. Ding *et al.*, "Dnn-opt: An RL inspired optimization for analog circuit sizing using deep neural networks", DAC, 2021.
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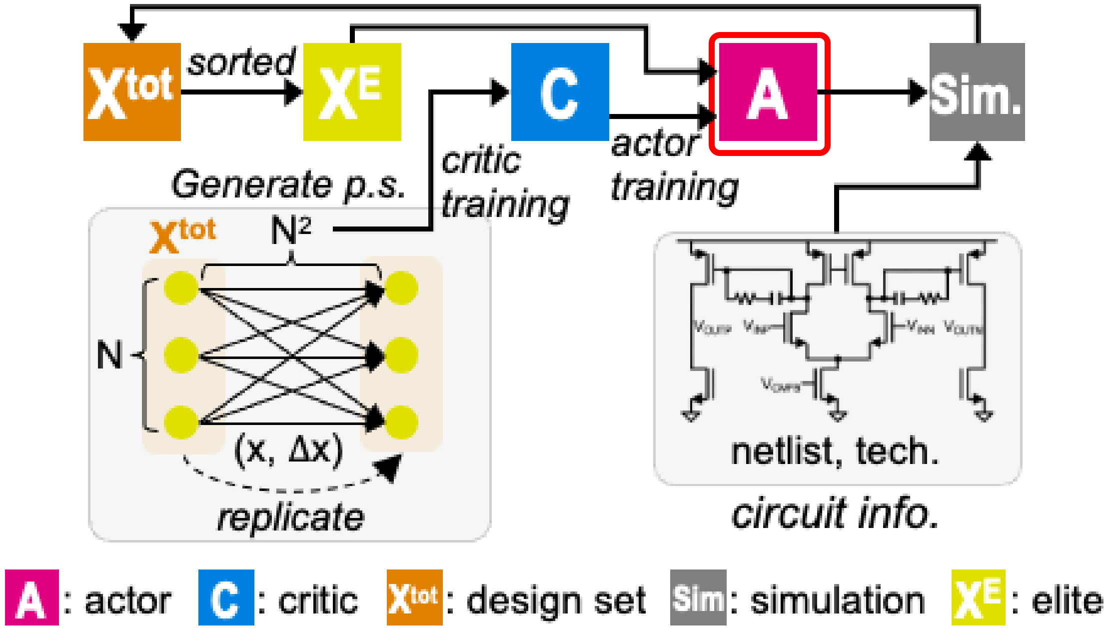

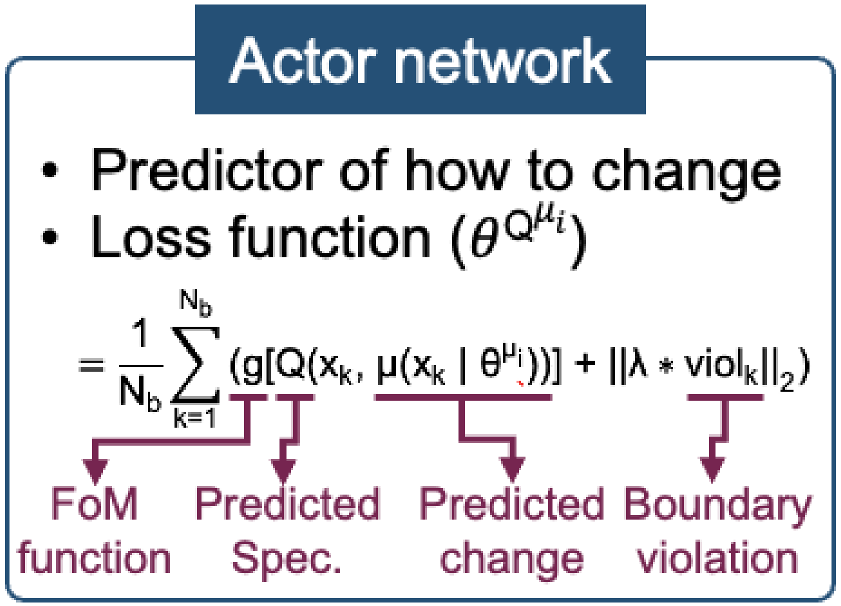

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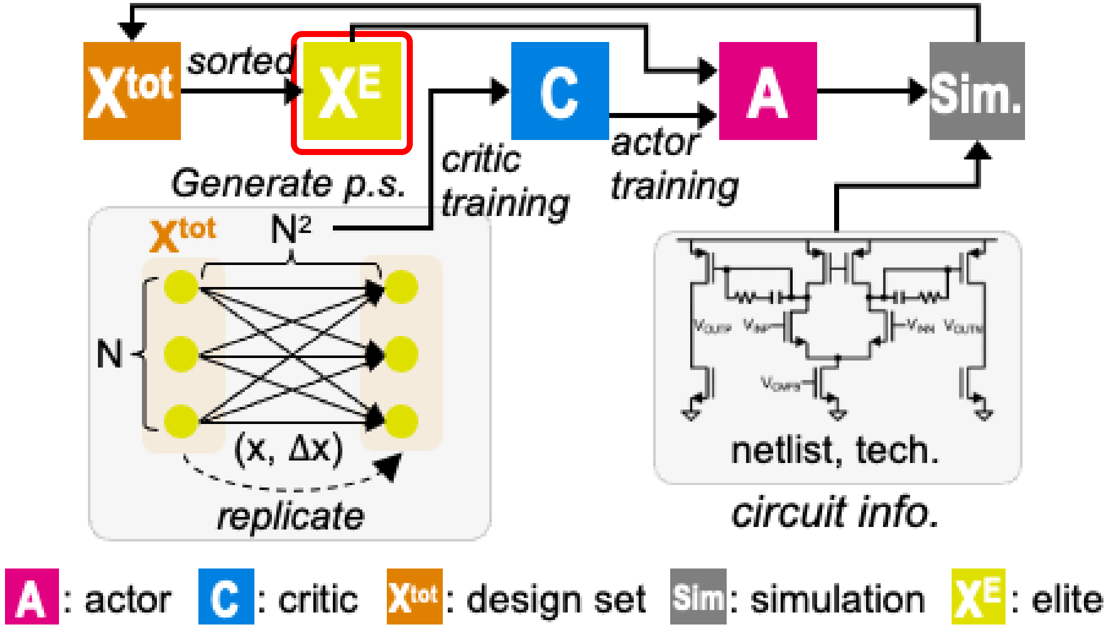
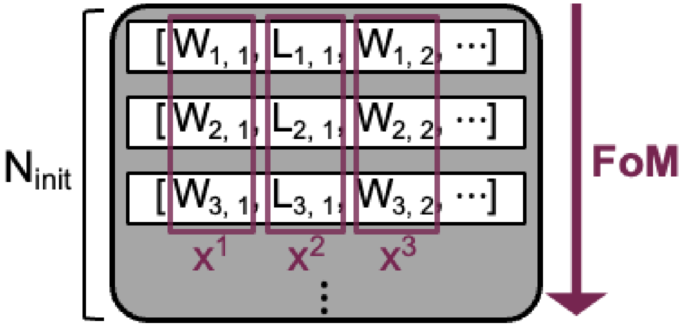
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **RL-inspired framework [4, 6, 7]**
    - Elite solution set stores the best N_{es} designs depending on FoM.
    - Help actor training by applying the elite boundary





$$\mathrm{viol}_k = \max(0, lb_{rest} - (\mathbf{x}_k + \Delta\mathbf{x}_k)) + \max(0, (\mathbf{x}_k + \Delta\mathbf{x}_k) - ub_{rest})$$

$$lb = min(\mathbf{X}^E,\ axis = 0)$$

$$ub = max(\mathbf{X}^E,\ axis = 0)$$

[4] C. Ding *et al.*, "Dnn-opt: An RL inspired optimization for analog circuit sizing using deep neural networks", DAC, 2021.
[6] A. Budak et al., "APOSTLE: asynchronously parallel optimization for sizing analog transistors using DNN Learning," ASP-DAC, 2023.
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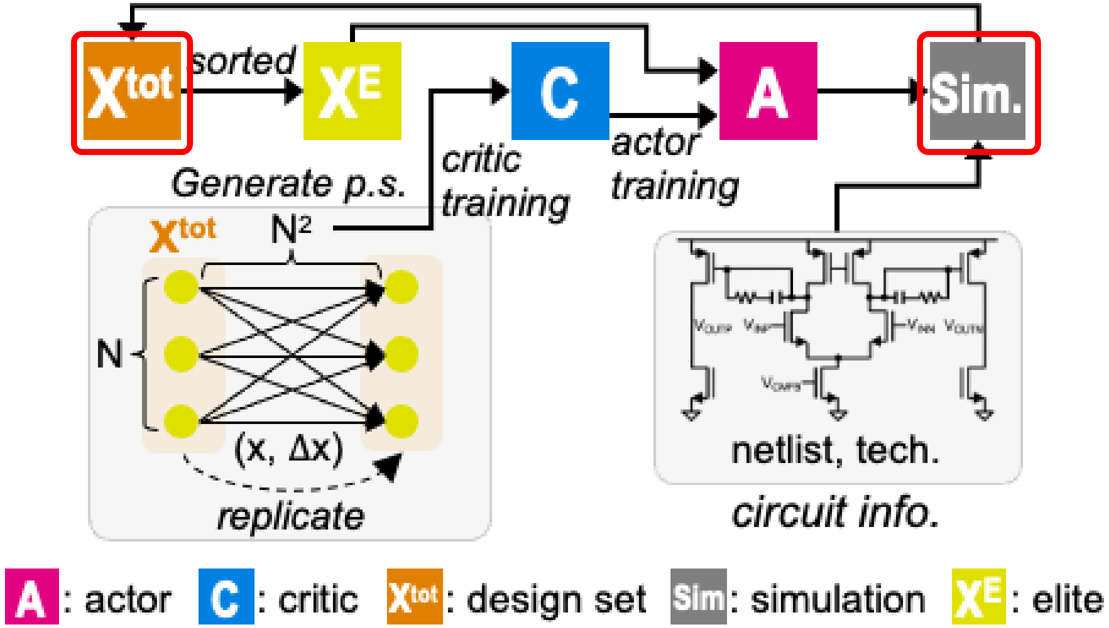
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **RL-inspired framework [4, 6, 7]**
    - After prediction, circuit simulation is executed.
    - Predicted designs are stored.



[4] C. Ding *et al.*, “Dnn-opt: An RL inspired optimization for analog circuit sizing using deep neural networks”, DAC, 2021.
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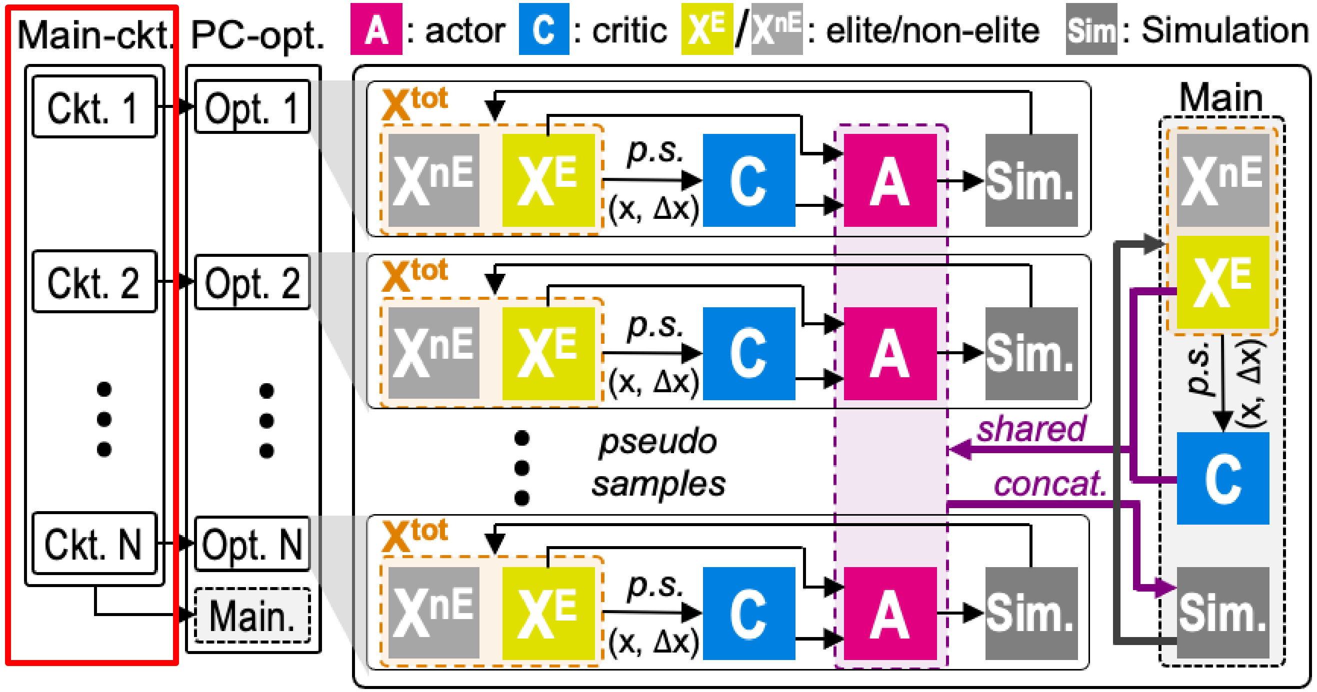
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Partition and conquer strategy**
    - Partition complex analog circuits into ***evaluable circuits***



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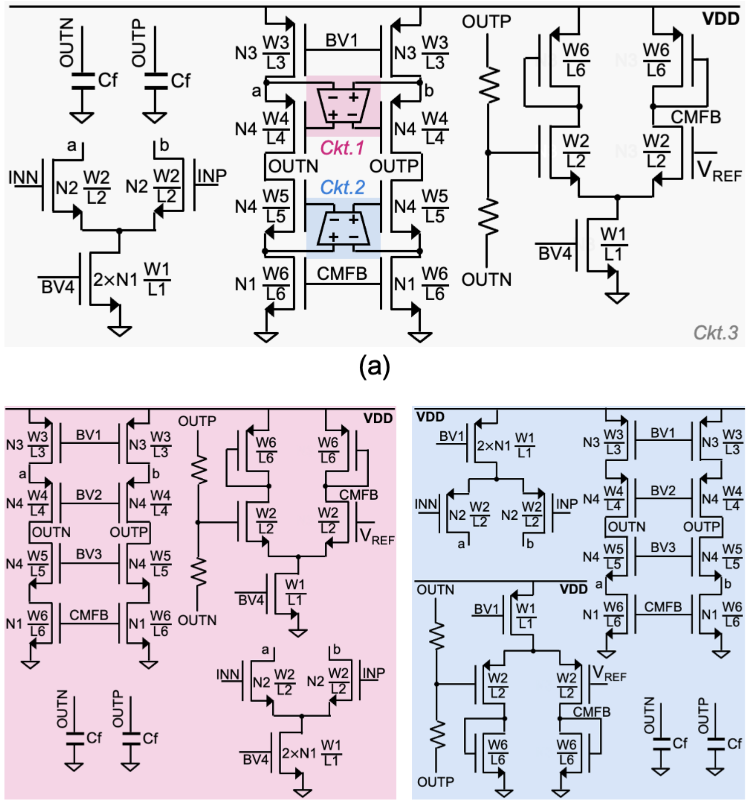
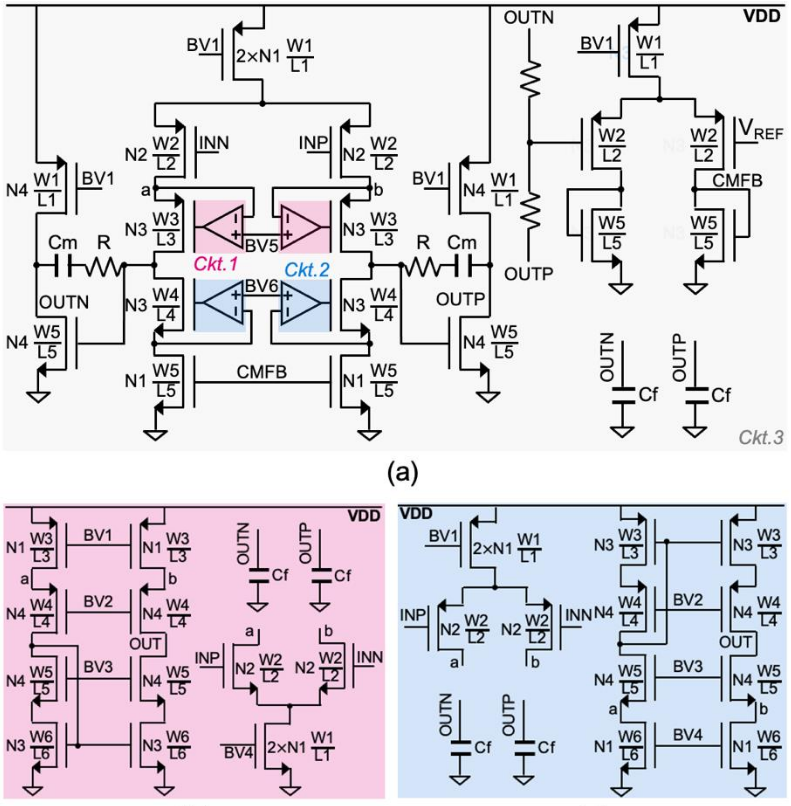
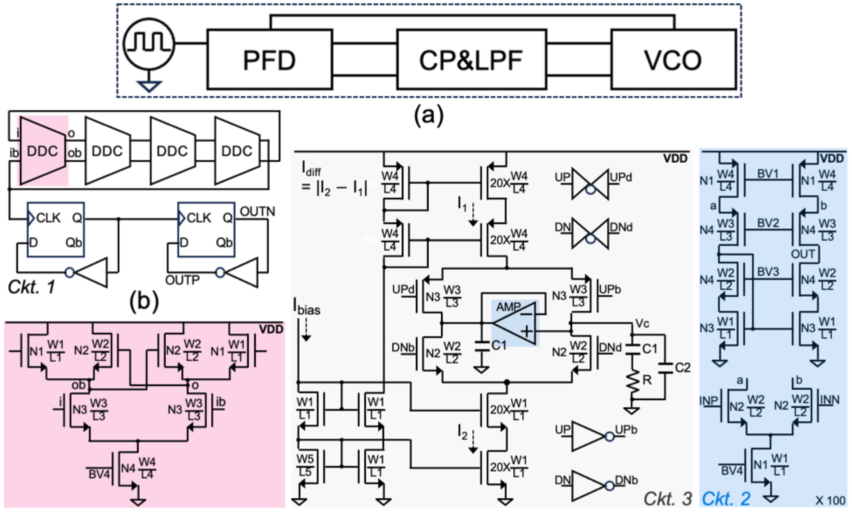


(a) (b) (c)



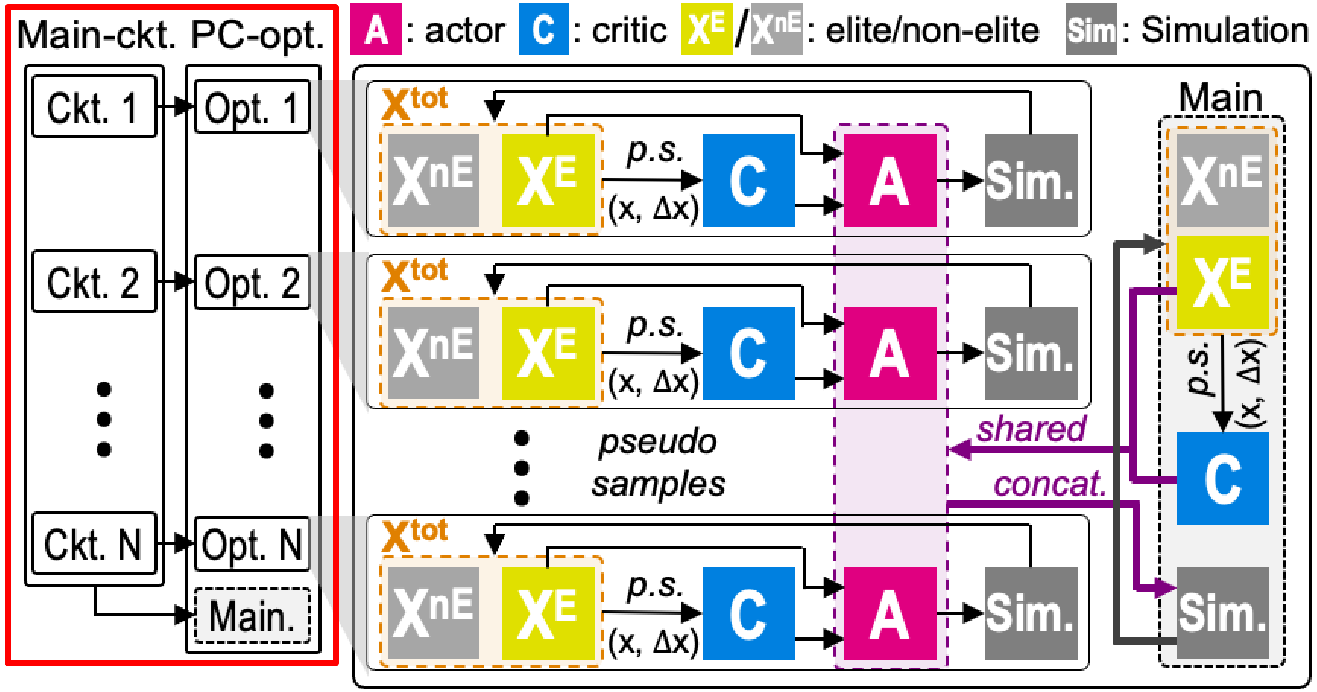
(a) (b) (c)



(a) (b) (c) (d) (e)

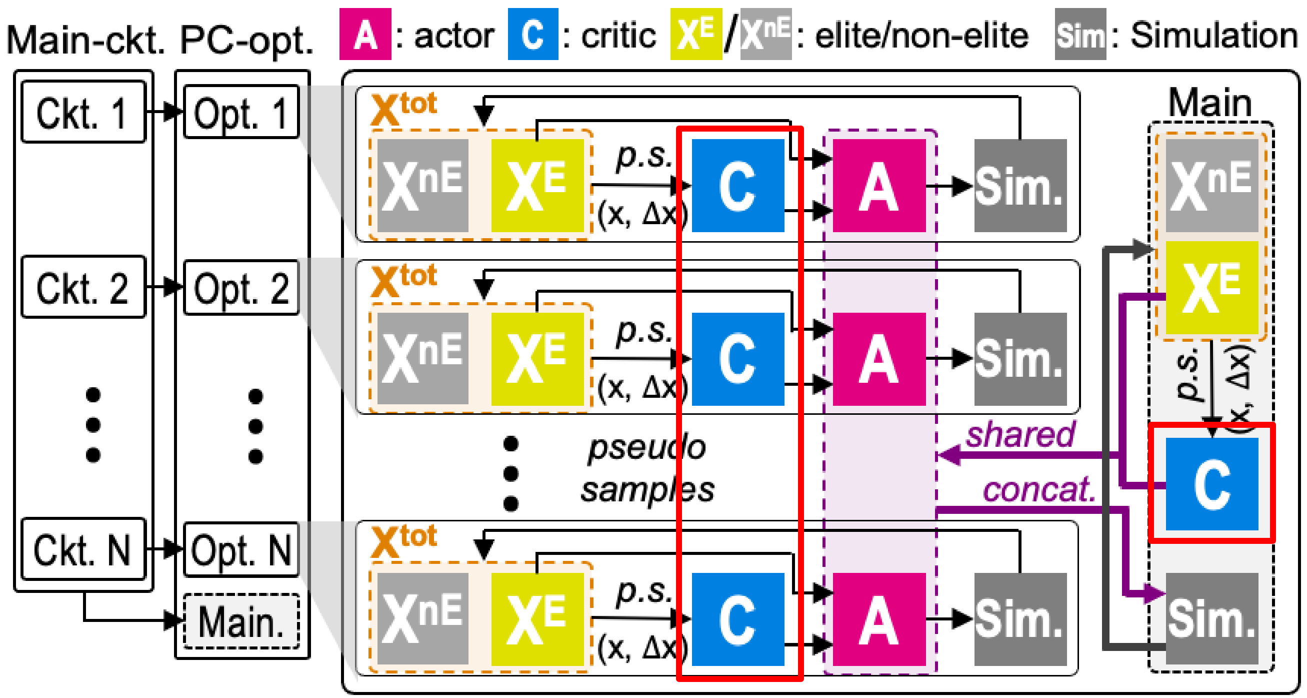
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Partition and conquer strategy**
    - Partitioned sub-circuits are assigned to each sub-process



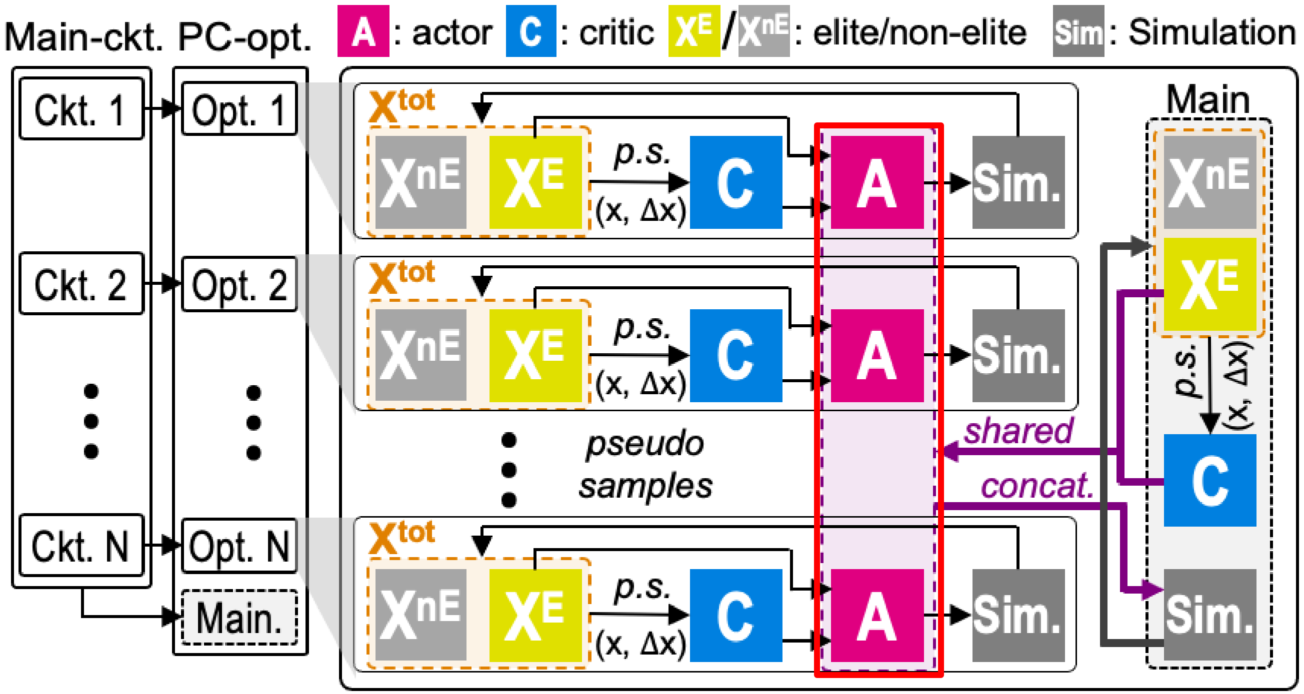
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (critic)**
    - For sub-processes, critics predict each circuit's specs.
    - Global critic predicts the main circuit's specs.



II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - Each actor is trained by using ***partial differential training***.



II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (loss function)**
      - For the actor training, ***the FoM predictions (sub-circuit, main-circuit)*** are used.

$$L_a(\theta^{\mu_i}) = \frac{1}{N_b}\sum_{k=1}^{N_b}[\underline{\underline{FoM_i^*(\mathbf{x}_{i,k}, \mu_i(\mathbf{x}_{i,k} \mid \theta^{\mu_i}))}}$$
$$+ ||\lambda * V_i(\mathbf{x}_{i,k})||_2 + \underline{\underline{FoM_g^*(\overline{\mathbf{x}_{opt,i,k}}, \Delta\overline{\mathbf{x}_{opt,i,k}})}}]$$

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (loss function)**
      - Applying the FoM prediction of the main circuit, sub-circuits are trained ***considering the optimizations of the main circuit.***

$$L_a(\theta^{\mu_i}) = \frac{1}{N_b} \sum_{k=1}^{N_b} [\underline{\underline{FoM_i^*(\mathbf{x}_{i,k}, \mu_i(\mathbf{x}_{i,k} \mid \theta^{\mu_i}))}}$$
$$+ ||\lambda * V_i(\mathbf{x}_{i,k})||_2 + \underline{\underline{FoM_g^*(\overline{\mathbf{x}_{opt,i,k}}, \Delta\overline{\mathbf{x}_{opt,i,k}})}}]$$

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (loss function)**
      - Critics (sub-circuit, main circuit) are applied to the FoM predictions.
      - ***Global critic is shared*** with actor training of sub-processes.

Sub-circuit

$$FoM_g^*(\mathbf{x}_g, \Delta\mathbf{x}_g) = g_g[\underline{\underline{Q_g}}(\mathbf{x}_g, \Delta\mathbf{x}_g)]$$

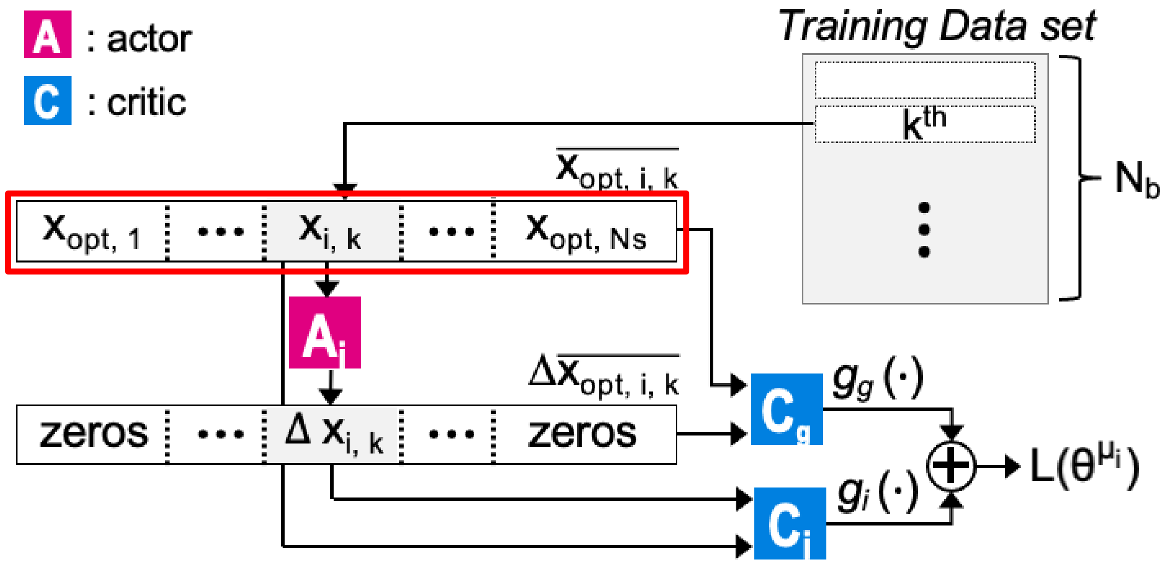
$$FoM_i^*(\mathbf{x}_{i,k}, \mu_i(\mathbf{x}_{i,k} \mid \theta^{\mu_i})) = g_i[\underline{\underline{Q_i}}(\mathbf{x}_{i,k}, \mu_i(\mathbf{x}_{i,k} \mid \theta^{\mu_i}))]$$

Main circuit, shared!

$$g[f(x)] = w_0 \times f_0(x) + \sum_{i=1}^{m} \min(1, \max(0, w_i \times |\frac{f_i(x) - c_i}{c_i}|))$$

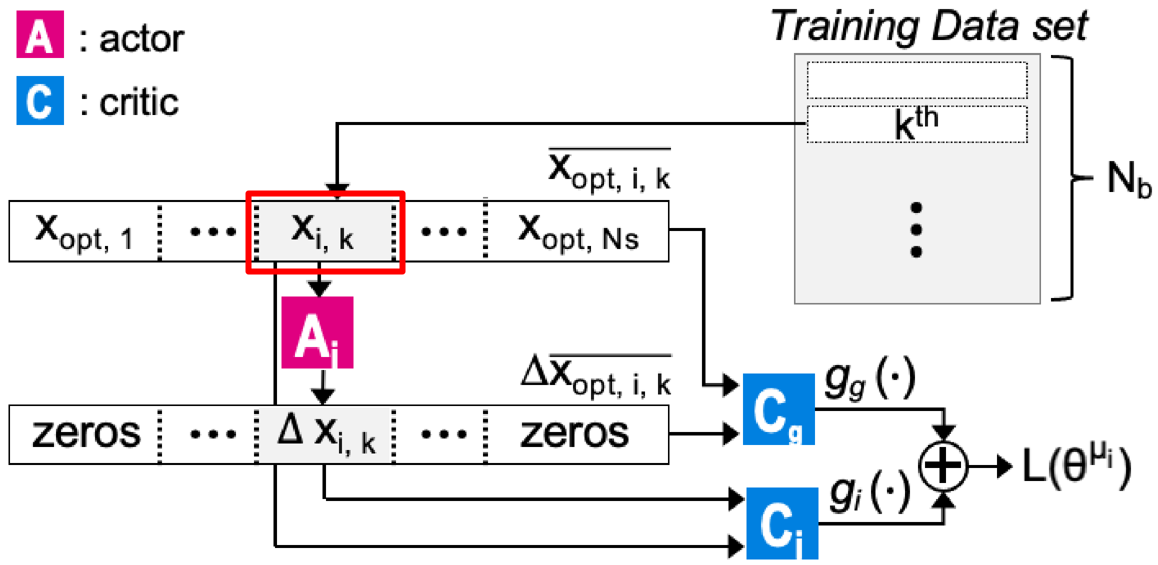
II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (training data set)**
      - Applying the best design of the main circuit, $\mathbf{x}_{opt}$



II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (training data set)**
      - The training data set is applied to the part of the sub-circuit.

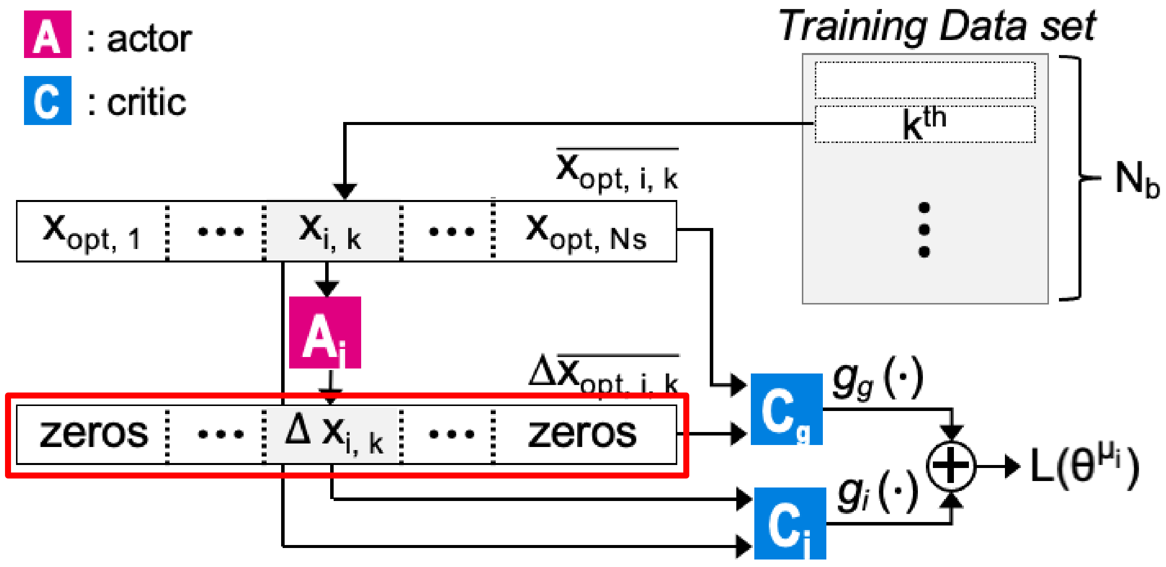


Partially converted design

$$\overline{\mathbf{x}_{opt,i,k}} = concat(\mathbf{x}_{opt}[0 : \sum_{k=1}^{i} d_k],\ \underline{\underline{\mathbf{x}_{i,k}}},\ \mathbf{x}_{opt}[\sum_{k=1}^{i+1} d_k : \sum_{k=1}^{N_s} d_k])$$

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (training data set)**
      - The ***partial change*** is defined by applying the actor's prediction.

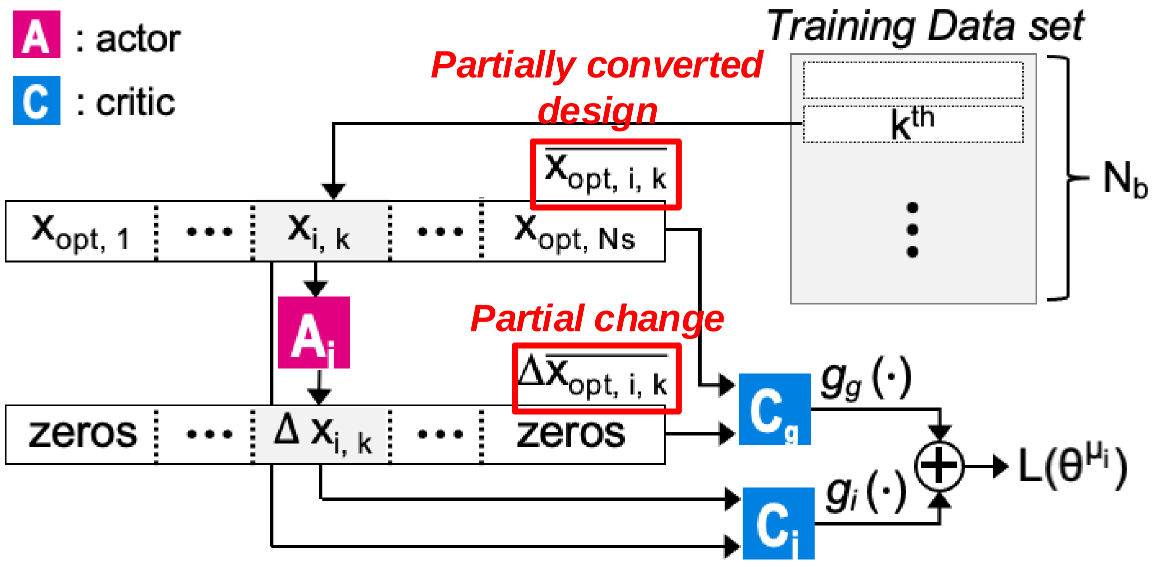


Partial change

$$\Delta\overline{\mathbf{x}_{opt,i,k}} = concat(zeros(\sum_{k=1}^{i} d_k), \Delta\mathbf{x}_{i,k}, zeros(\sum_{k=1}^{i+1} d_k))$$

II. Proposed Method

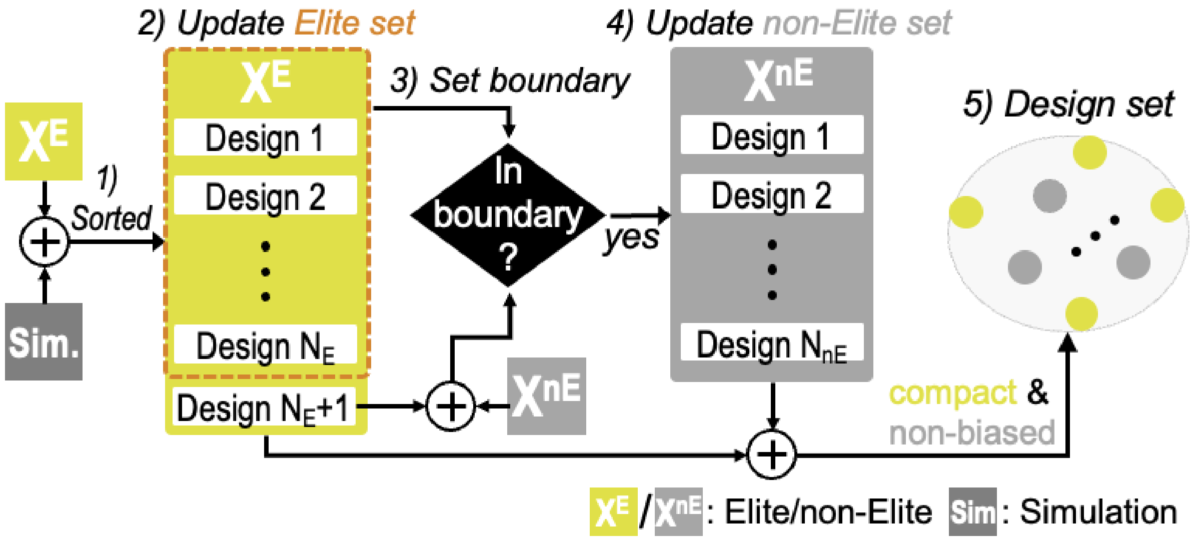
- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Multi-agent systems (actor)**
    - **Partial differential training (training data set)**
      - These are utilized to the FoM prediction of the main circuit.



$$L_a(\theta^{\mu_i}) = \frac{1}{N_b}\sum_{k=1}^{N_b}[FoM_i^*(\mathbf{x}_{i,k}, \mu_i(\mathbf{x}_{i,k} \mid \theta^{\mu_i})) + ||\lambda * V_i(\mathbf{x}_{i,k})||_2 + \underline{FoM_g^*(\overline{\mathbf{x}_{opt,i,k}}, \Delta\overline{\mathbf{x}_{opt,i,k}})}]$$

II. Proposed Method

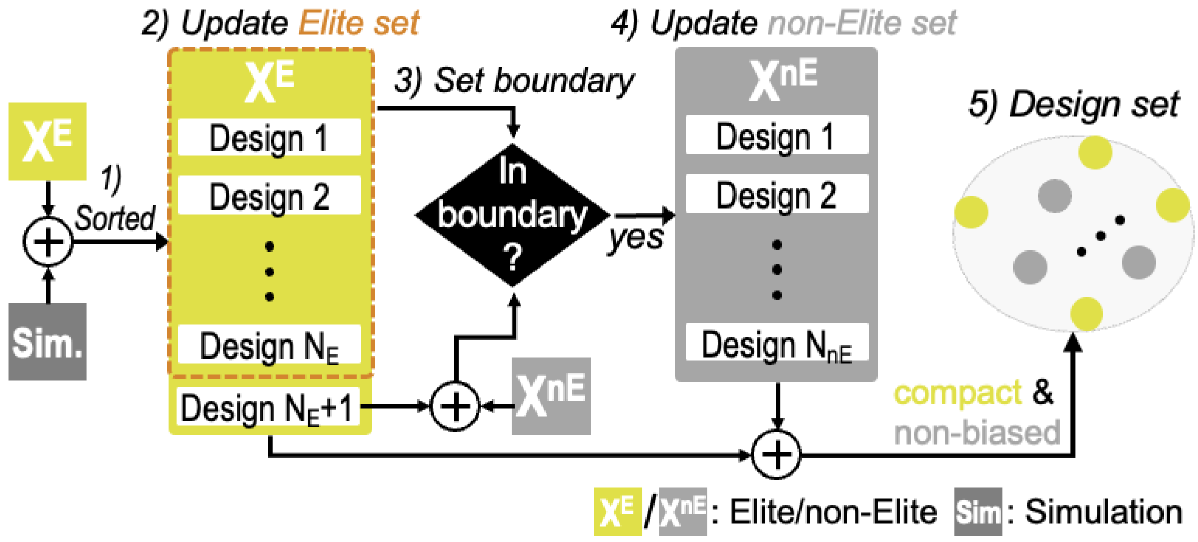
- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Concentrated sampling method**
    - Creating balanced dataset for network training is crucial [8, 9].
    - Devised for efficient critic training.



[8] J. Laurikkala, "Improving identification of difficult small classes by balancing class distribution," Proceedings of the 8th Conference on AI in Medicine in Europe: Artificial Intelligence Medicine, pp. 63-66, 2001.
[9] D. Mease $et\ al.$, "A multiple resampling method for learning from imbalanced data sets," Computational Intelligence, vol. 20, pp. 18-36, 2004.

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Concentrated sampling method**
    - Using the entire data in the elite boundary
      - Not only the elite data but also non-elite data



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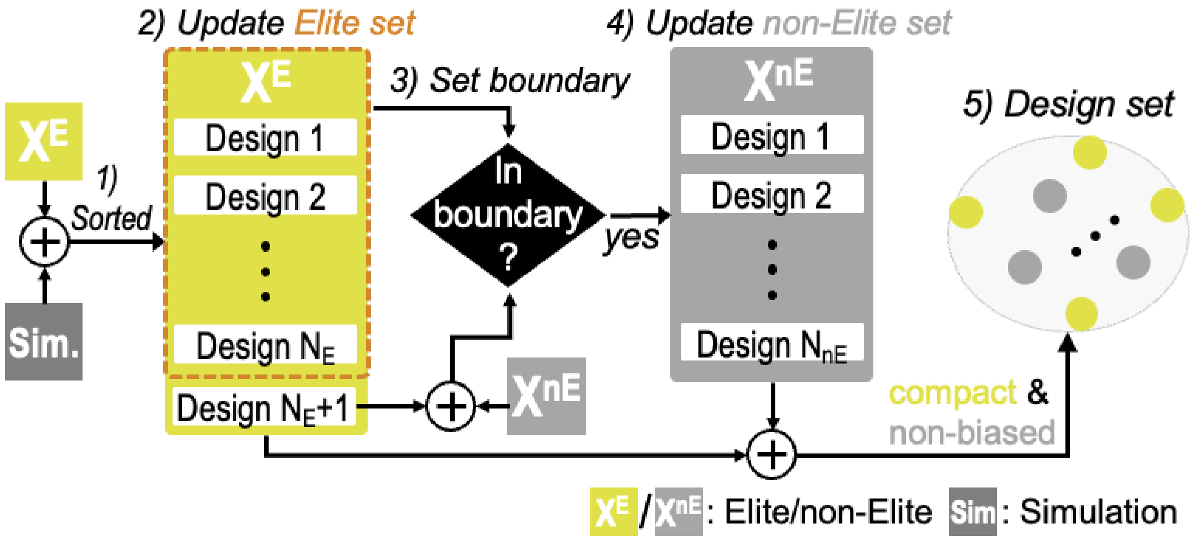
$$+ ||\lambda * V_i(\mathbf{x}_{i,k})||_2 + FoM_g^*(\overline{\mathbf{x}_{opt,i,k}}, \Delta\overline{\mathbf{x}_{opt,i,k}})]$$

II. Proposed Method

- **Partition-and-conquest-based optimizer (PC-Opt)**
  - **Concentrated sampling method**
    - Providing a ***compact and non-biased dataset*** for critic training



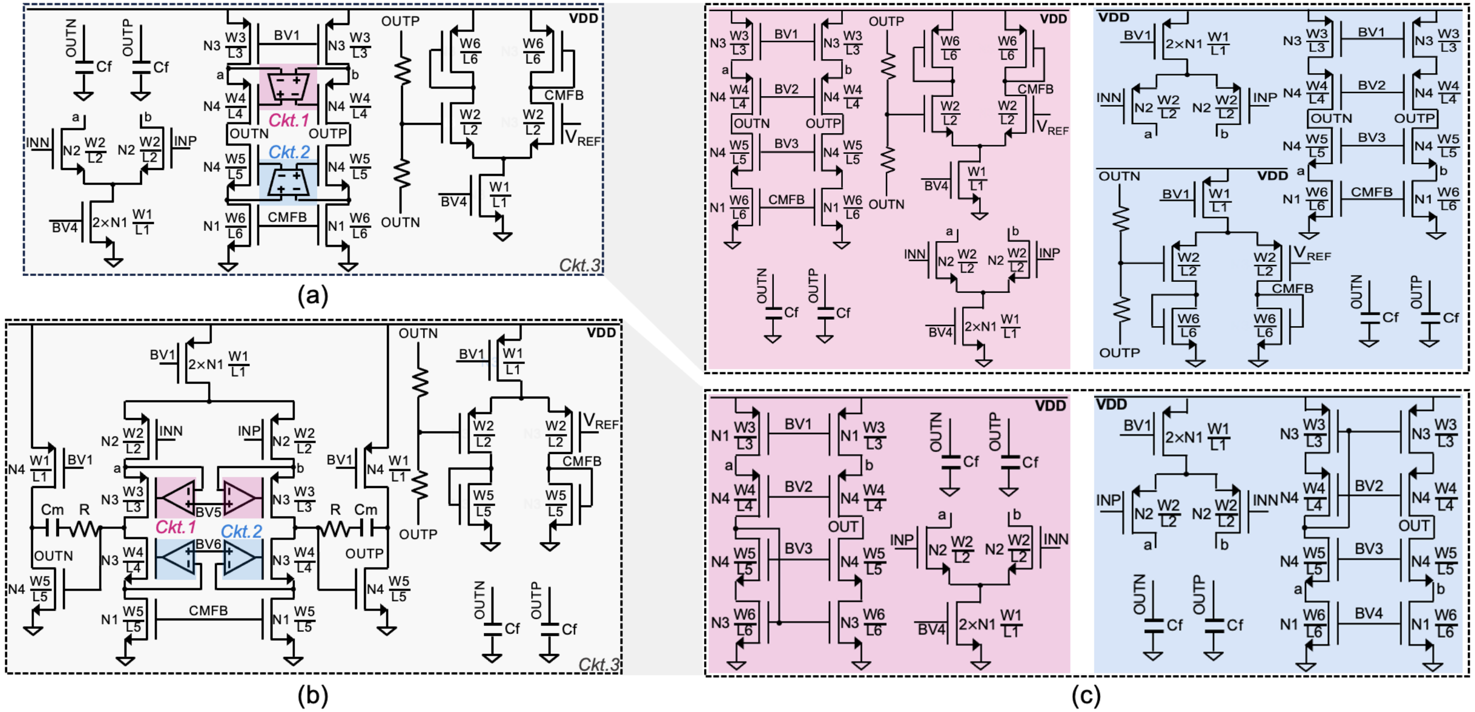
III. Experimental Setup and Results

- **Experimental setup**
  - Intel(R) Xeon(R) Gold 6132 CPUs operation at a clock frequency of 2.60 GHz
  - Synopsys HSPICE, Cadence Open Command Environment for Analysis (OCEAN)
  - A commercial 28nm technology for the gain-boost amplifiers
  - A commercial 180nm technology for the Phase locked loop (PLL)

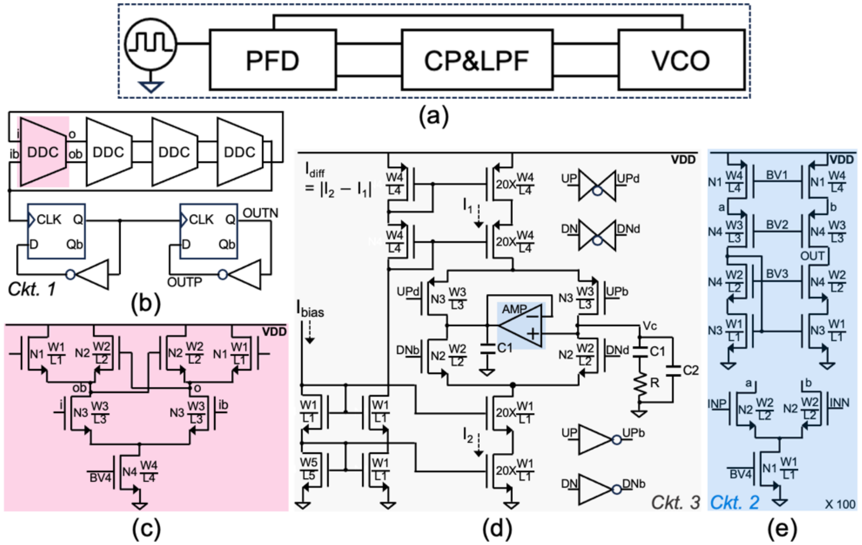
III. Experimental Setup and Results

- **Circuits for experiments**
  - **Schematics**

Two types of gain-boost amplifiers



PLL



III. Experimental Setup and Results

- **Circuits for experiments**

Types and ranges of design parameters

(a) Gain Boost Amplifier 1

Types of parameters	Unit	Ranges
$W1_1, \ldots, W7_1$, $W1_2, \ldots, W7_2$, and $W1_3, \ldots, W7_3$	μm	[0.08, 40]
$L1_1, \ldots, L7_1$, $L1_2, \ldots, L7_2$, and $L1_3, \ldots, L7_3$	μm	[0.03, 1]
$N1_1, \ldots, N4_1$, $N1_2, \ldots, N4_2$, and $N1_3, \ldots, N3_3$	integer	[1, 10]
Cf_1, Cf_2, and Cf_3	fF	[30, 3000]

The notation p_{i_s} represents the parameter p of the i_s^{th} sub-circuit.

(b) Gain Boost Amplifier 2

Types of parameters	Unit	Ranges
$W1_1, \ldots, W7_1$, $W1_2, \ldots, W7_2$, and $W1_3, \ldots, W5_3$	μm	[0.08, 40]
$L1_1, \ldots, L7_1$, $L1_2, \ldots, L7_2$, and $L1_3, \ldots, L5_3$	μm	[0.03, 1]
$N1_1, \ldots, N4_1$, $N1_2, \ldots, N4_2$, and $N3_3, \ldots, N3_3$	integer	[1, 10]
Cf_1, Cf_2, Cf_3, and Cm_3	fF	[30, 3000]
R_3	KΩ	[0.1, 100]

The notation p_{i_s} represents the parameter p of the i_s^{th} sub-circuit.

(c) Phase Locked Loop

Types of parameters	Unit	Ranges
$W1_1, \ldots, W4_1$, $W1_2, \ldots, W4_2$, and $W1_3, \ldots, W4_3$	μm	[0.22, 5]
$L1_1, \ldots, L4_1$, $L1_2, \ldots, L4_2$, and $L1_3, \ldots, L4_3$	μm	[0.18, 1]
$N1_1, \ldots, N4_1$, $N1_2, \ldots, N4_2$, and $N1_3, \ldots, N3_3$	integer	[1, 10]
$C1_3$ and $C2_3$	fF	[30, 3000]
R_3	KΩ	[1, 100]

The notation p_{i_s} represents the parameter p of the i_s^{th} sub-circuit.

Types of specs and targets

(a) Gain Boost Amplifier 1

Types of specs	Targets
Unity gain freq.$_s$	$>$ 100 MHz
Phase margin$_s$	$>$ 60°
DC gain$_s$	$>$ 60 dB
CMRR$_s$	$>$ 90 dB
PSRR$_s$	$>$ 90 dB
Unity gain freq.$_g$	$>$ 100 MHz
Phase margin$_g$	$>$ 60°
DC gain$_g$	$>$ 90 dB
CMRR$_g$	$>$ 120 dB
PSRR$_g$	$>$ 120 dB
Power$_s$, Power$_g$	Minimize

(b) Gain Boost Amplifier 2

Types of specs	Targets
Unity gain freq.$_s$	$>$ 100 MHz
Phase margin$_s$	$>$ 60°
DC gain$_s$	$>$ 60 dB
CMRR$_s$	$>$ 90 dB
PSRR$_s$	$>$ 90 dB
Unity gain Freq.$_g$	$>$ 50 MHz
Phase margin$_g$	$>$ 60°
DC gain$_g$	$>$ 120 dB
CMRR$_g$	$>$ 150 dB
PSRR$_g$	$>$ 150 dB
Power$_s$, Power$_g$	Minimize

The notation s_s and s_g represent the spec s of the sub-circuits and the main circuit, respectively.

(c) Phase Locked Loop

Types of specs	Targets
Minimum freq.$_1$	$<$ 100 MHz
Maximum freq.$_1$	$>$ 300 MHz
DC gain$_2$	$>$ 60 dB
CMRR$_2$	$>$ 90 dB
PSRR$_2$	$>$ 90 dB
Power$_2$	Minimize

Types of specs	Targets
Lock time$_3$	Minimize
Current diff.$_3$	Minimize
Power$_3$	Minimize
Lock time$_g$	Minimize
Zitter$_g$	Minimize
Phase diff.$_g$	Minimize
Power$_g$	Minimize

The notation s_{i_s} and s_g represent the spec s of the i_s^{th} sub-circuit and the main circuit, respectively.

III. Experimental Setup and Results

- **Experimental Setup**
  - BO [10], DDPG [11], MA-Opt [6, 7] were compared to PC-Opt.
  - Ablation experiments for the concentrated sampling method was conducted (NC-Opt).

[6] A. Budak et al., "APOSTLE: asynchronously parallel optimization for sizing analog transistors using DNN Learning," ASP-DAC, 2023.
[7] Y. Choi et al., "MA-opt: Reinforcement Learning-based analog circuit optimization using multi-actors," TCAS-I, 2023.
[10] F. Nogueira., "Bayesian Optimization: open source constrained global optimization tool for python," https://github.com/fmfn/BayesianOptimization, 2014.
[11] A. Hill $et\ al.$, "Stable Baseline3," https://github.com/DLR-RM/stable-baselines3, 2023.

III. Experimental Setup and Results

- **Experimental Setup**
  - Each method was executed five to six times ***to analyze the results statistically***.
  - For the gain-boost amplifiers, the execution time of each method ***was restricted based on the time*** when PC-Opt was terminated.
  - For the PLL, the number of simulations was set to 100 for all optimization methods.
    - Circuit simulation time was dominant.

III. Experimental Setup and Results

- **Experimental Results**
  - For the test circuits, ***PC-Opt obtained the best*** average FoM, success rate, and minimum target metric.
  - The effectiveness of the concentrated sampling method was demonstrated.

(a) Gain Boost Amplifier 1

Algorithm	BO	DDPG	MA-Opt	NC-Opt	PC-Opt
Success rate	0/6	1/6	0/6	3/6	**6/6**
Min. power (μW)	–	883.0	–	178.5	**121.0**
Avg. log_{10}(FoM)	−0.683	−0.585	−0.832	−1.717	**−3.808**
Total runtime (h)	483*	2740*	557*	2.1	2.17

*: The number of simulations conducted within the execution time when PC-Opt was performed 200 times.

(b) Gain Boost Amplifier 2

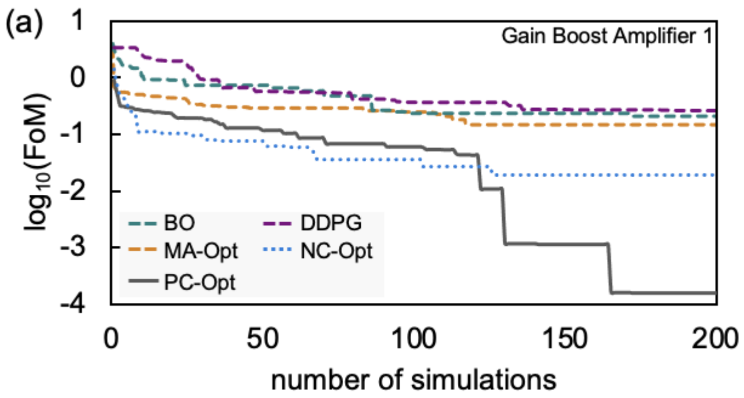
Algorithm	BO	DDPG	MA-Opt	NC-Opt	PC-Opt
Success rate	3/6	**6/6**	2/6	2/6	**6/6**
Min. power (μW)	132.8	131.0	112.0	112.5	**93.8**
Avg. log_{10}(FoM)	−1.434	−3.492	−1.282	−1.125	**−3.914**
Total runtime (h)	1200*	2350*	600*	2.25	2.33

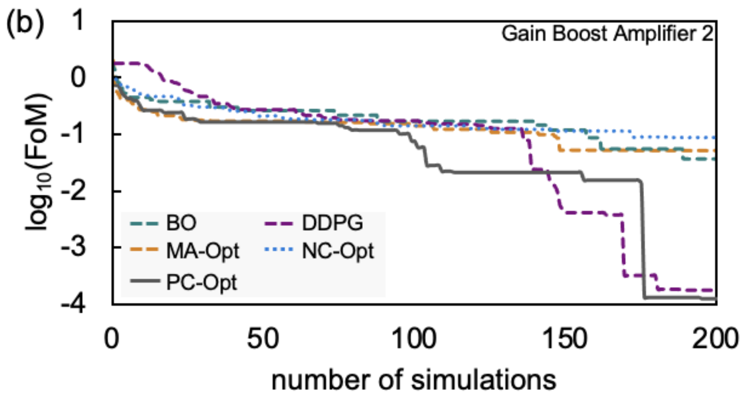
*: The number of simulations conducted within the execution time when PC-Opt was performed 200 times.

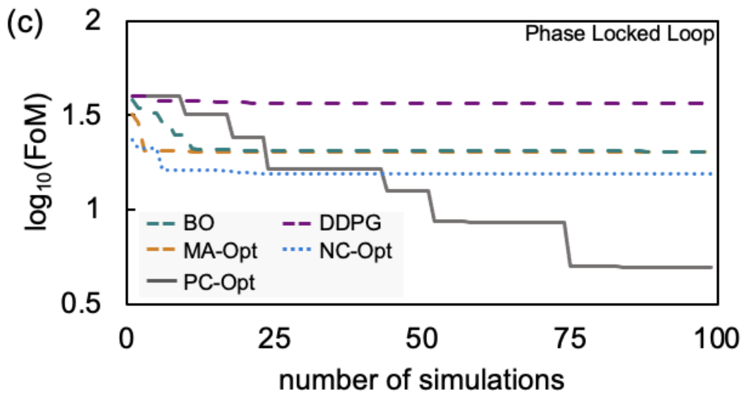
(c) Phase Locked Loop

Algorithm	BO	DDPG	MA-Opt	NC-Opt	PC-Opt
Success rate	0/5	0/5	0/5	1/5	**4/5**
Min. FoM	–	–	–	0.67	**0.46**
Avg. log_{10}(FoM)	1.308	1.564	1.303	1.191	**0.697**

FoM: 1e6 × Lock time$_g$ [s] + 1e5 × Zitter$_g$ [s] + 1e9 × Phase diff.$_g$ [s] + le2 × Power$_g$ [W]







IV. Conclusion

- We proposed ***PC-Opt*.**
  - a partition-and-conquest-based
  - multi-agent actor-critic framework
  - applying the RL-inspired method

- We defined the proper roles of the multi-agent actor-critic framework.
  - Partial differential training

- Concentrated sampling method for generating a balanced dataset

Thank you!

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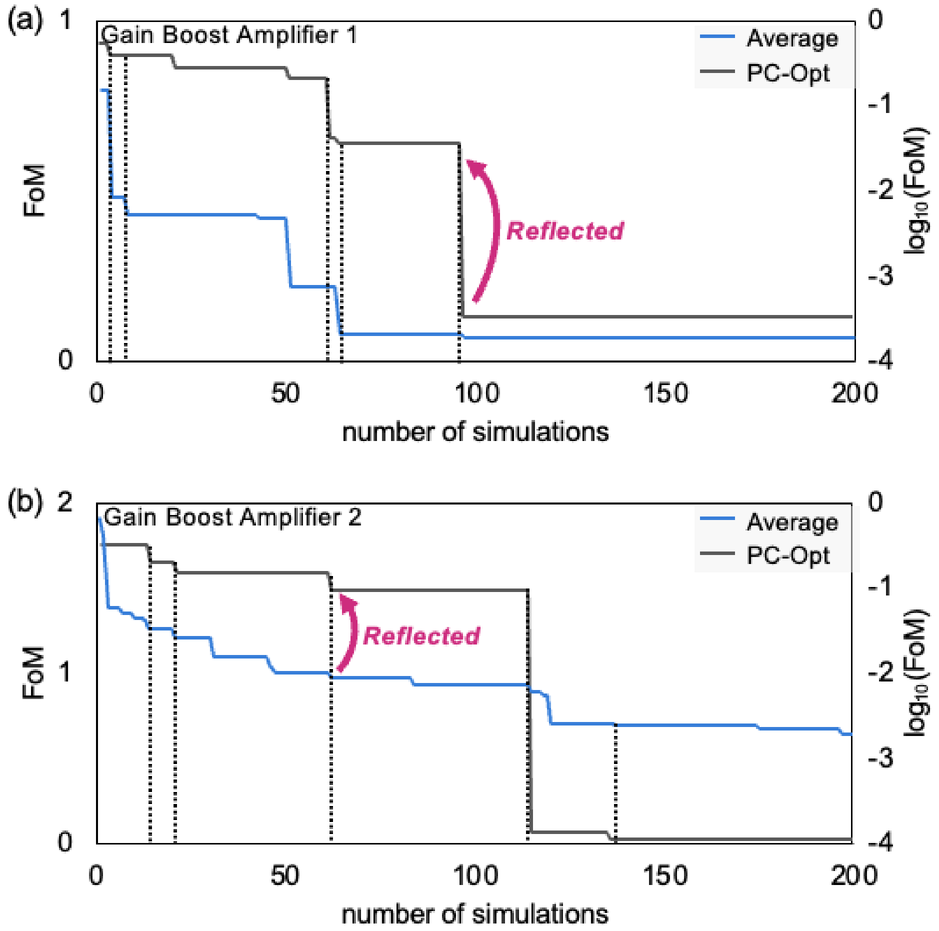
Appendix A.

- **Reflection of the sub-process for the main circuit optimization**
  - The average and FoM_g are changed at the same time



Average: $$\frac{1}{N_s}\sum_{i=1}^{N_s}(FoM_i + FoM_g) = \frac{1}{N_s}\sum_{i=1}^{N_s}(g_i[f_i(\mathbf{x})])$$

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[4] C. Ding *et al*., “Dnn-opt: An RL inspired optimization for analog circuit sizing using deep neural networks”, DAC, 2021.
[5] Zhang et al., “Automated design of complex analog circuits with multiagent based reinforcement learning,” DAC, 2023.
[6] A. Budak et al., ”APOSTLE: asynchronously parallel optimization for sizing analog transistors using DNN Learning,” ASP-DAC, 2023.
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