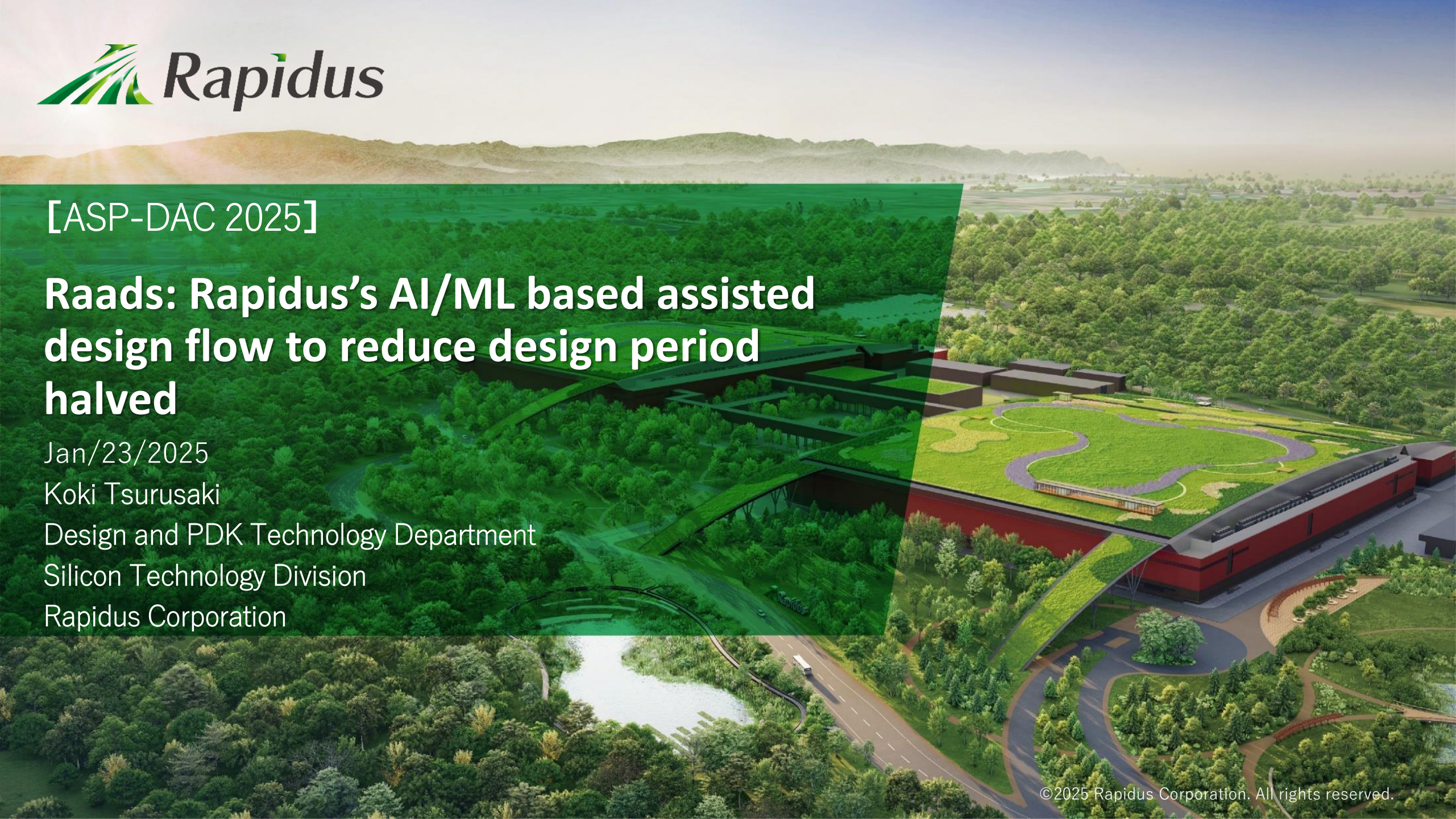


[ASP-DAC 2025]

Raads: Rapidus's AI/ML based assisted design flow to reduce design period halved

Jan/23/2025

Koki Tsurusaki
Design and PDK Technology Department
Silicon Technology Division
Rapidus Corporation

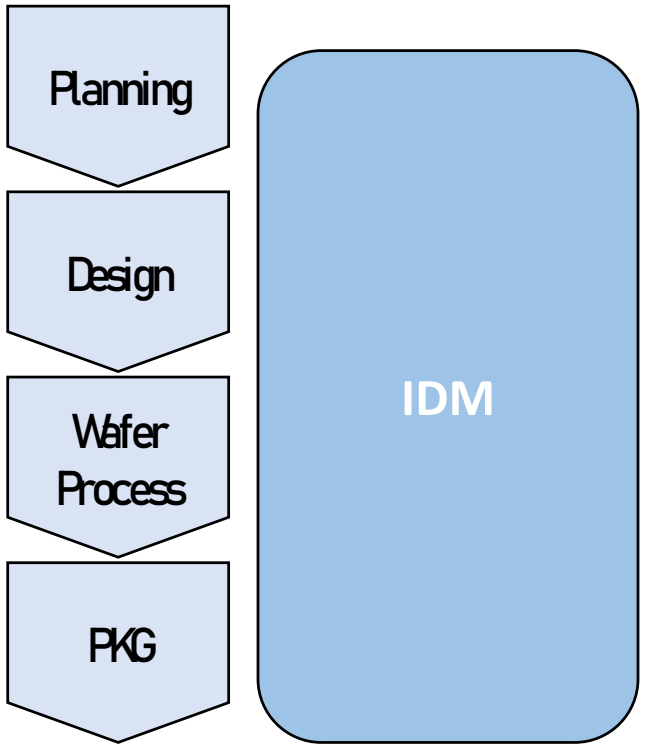
Rapidus *differentiates in speed.*

World's Shortest Total Cycle-Time

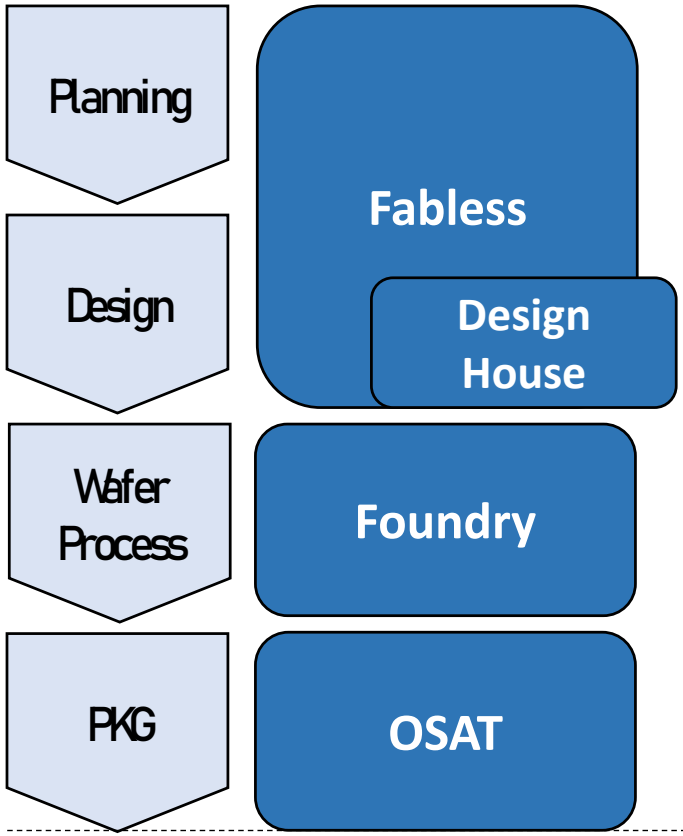
"RUMS" – True Requirement for the Age of AI

1 2 3

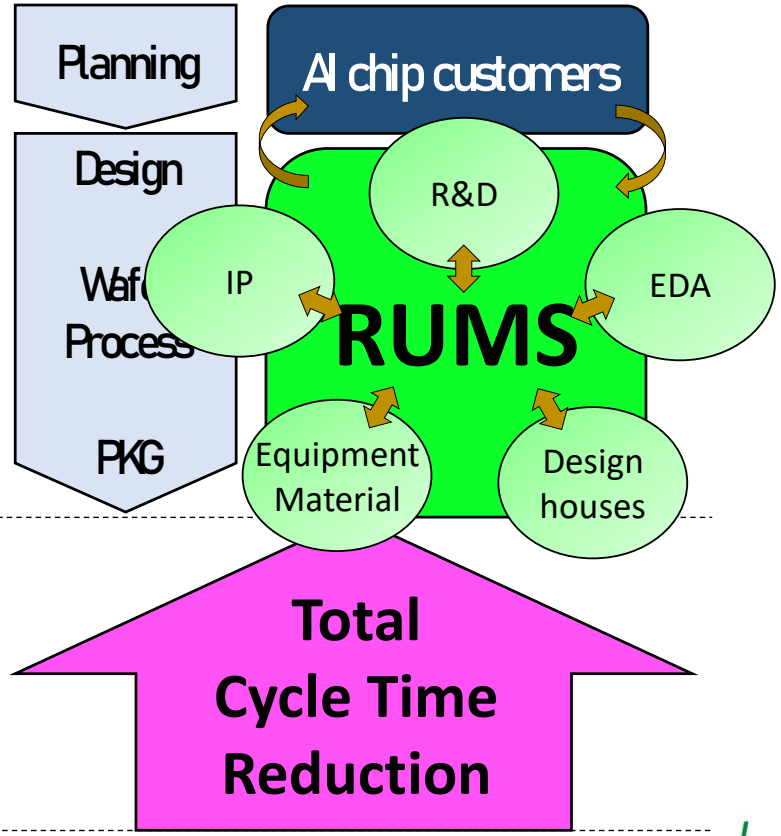
Vertical Integration



Horizontal Specialization

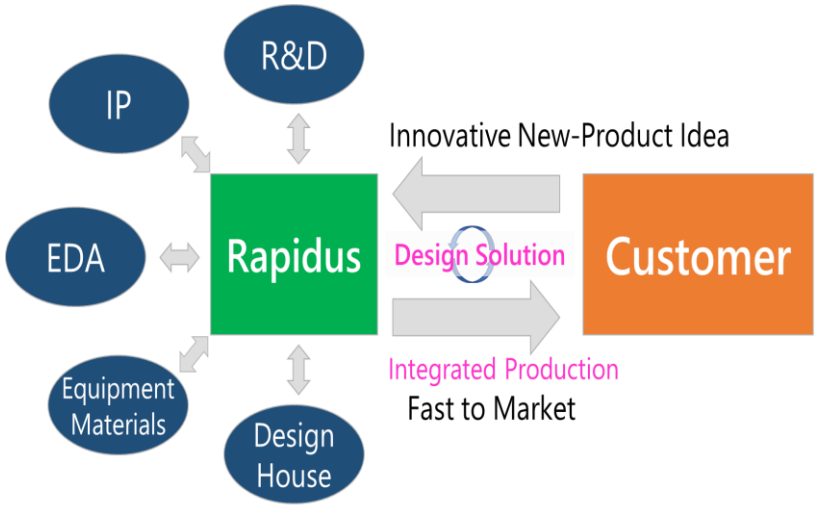


Integrative Co-Creation



RUMS Innovation Challenge

Concept: *Integrative Co-creation*



What: *Customer's Benefit*

1. **Integrated Development Environment between Silicon & 3D PKG**
   - Unified and integrated design reference flow support
2. **ML+AI Assisted Development**
   → Paradigm Change for Speed and Quality
   - ML+AI Assisted Technology Data Model
   - Digital=Twin Environment
3. **Precise Manufacturing Data & AI Analysis**
   → Quick Feedback to Design
   - Feedback to Next Development (Rapidus + Customer + Partner)

How: *Rapidus' Solution*

- **Raads: Rapidus AI-Assisted Design Solutions**
- **DMCO**: Design & Mfg Co-Optimization
- **ADK**: Assembly Design Kit

Outline

1. Raads Concept and Components
2. How to utilize GenAI for chip design
3. Importance of early PPA prediction
4. AI-based physical prototyping

1

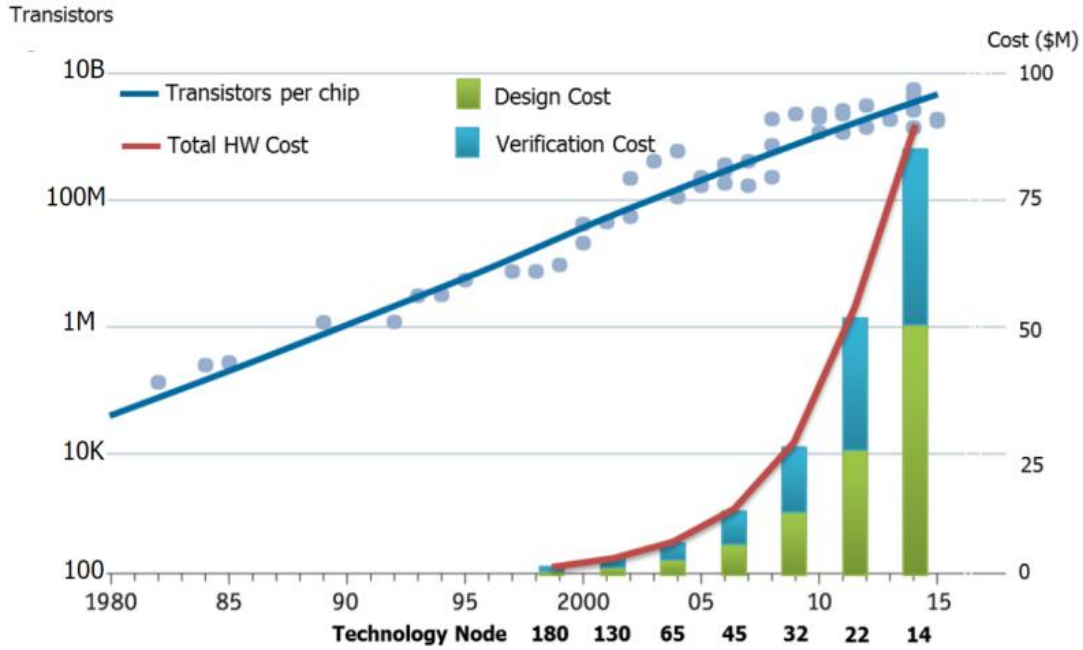
Raads Concept and Components

Raads concept and motivation

Challenges for large scale advanced node design :
- design cost, eda tool cost, design period

Barriers :
- designer expertise and resource

Solution :
- Active use of ML/AI in chip design flow for both productivity improvement and fast design convergence



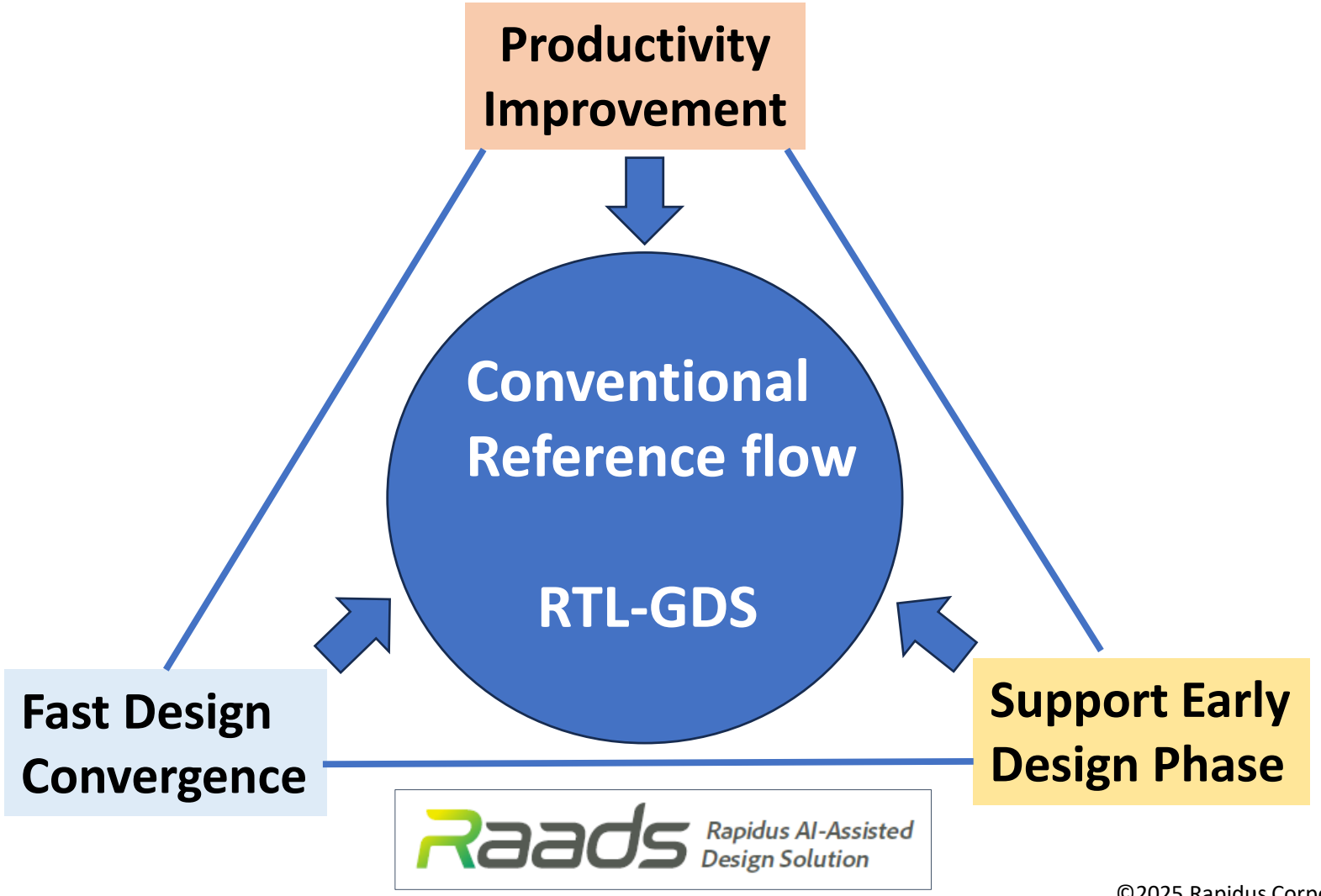
Andreas Olofsson, keynote, Intl. Symp. on Physical Design, March 2018

- Rapidus develop Raads (Rapidus AI-Assisted Design Solution) as option of Reference flow
- Raads is designed for Rapids 2nm design optimization.
- Raads utilize both productivity improvement and fast design convergence -> Less design cost

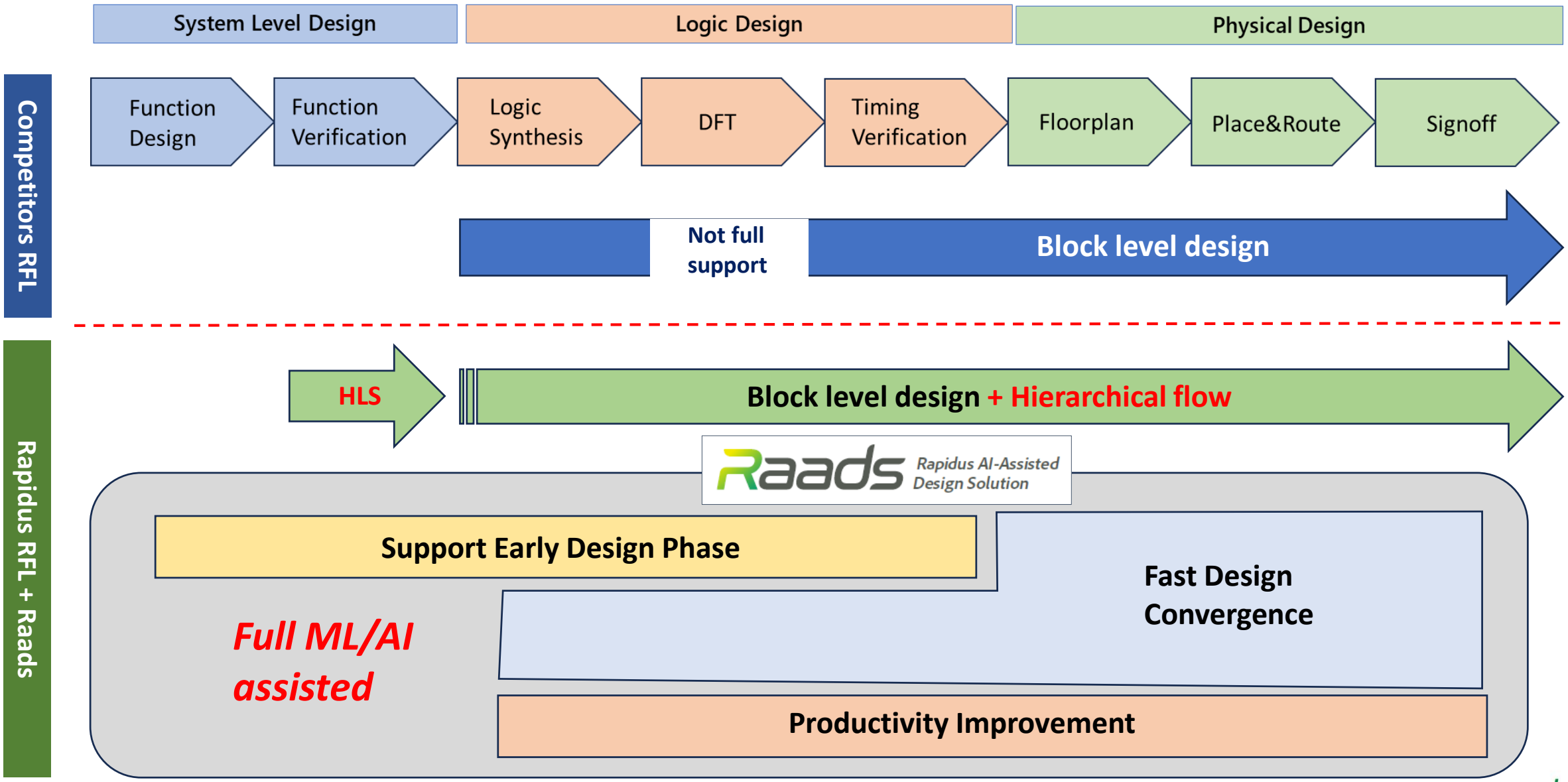
Raads Rapidus AI-Assisted Design Solution

Conventional Reference Flow and Raads

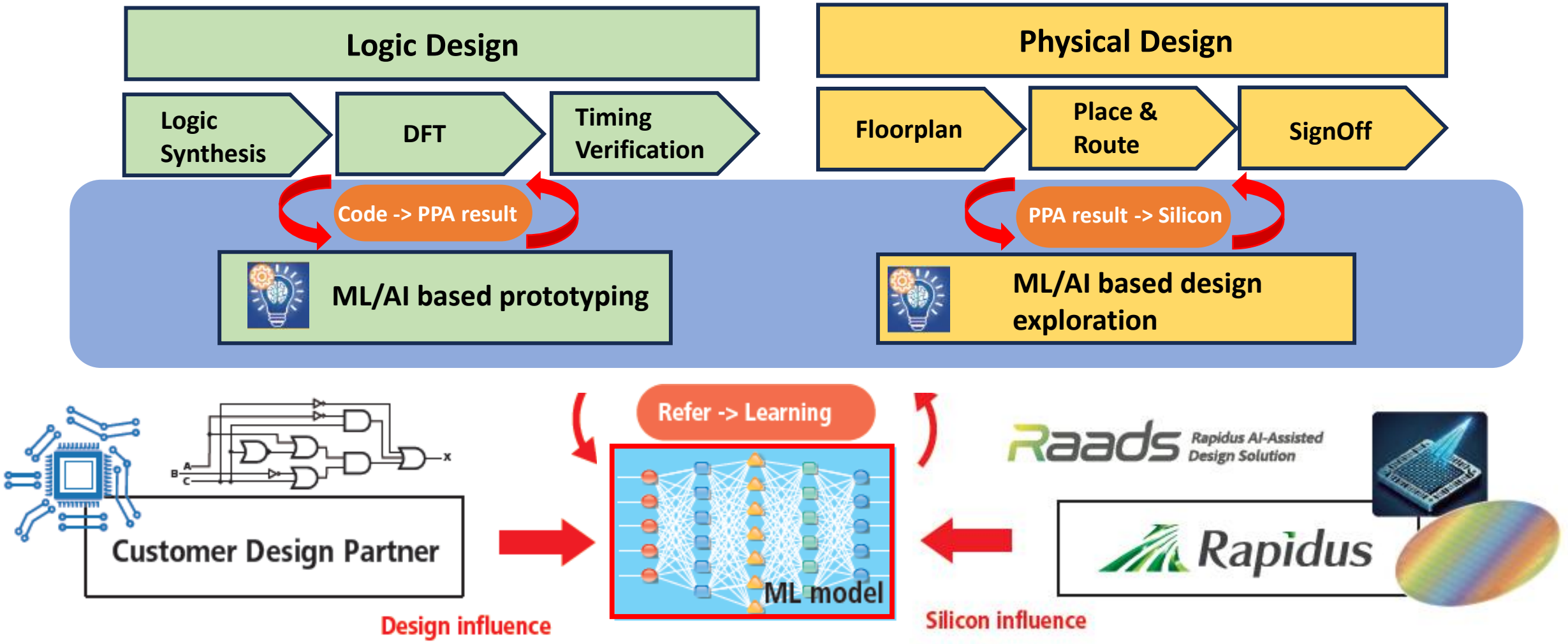
- Raads (Rapidus AI-Assisted Design Solution) is support 3 areas to reduce design cycle time 50%
- Raads is the additional option of conventional reference flow



Rapidus Reference flow and Raads components



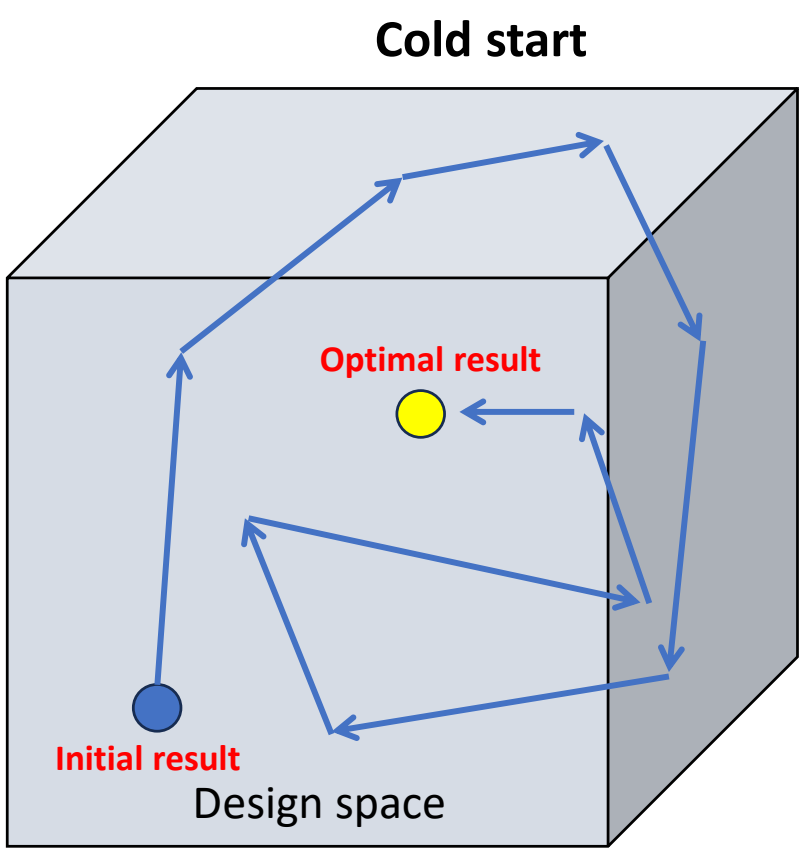
Raads can push PPACt with ML model improvement

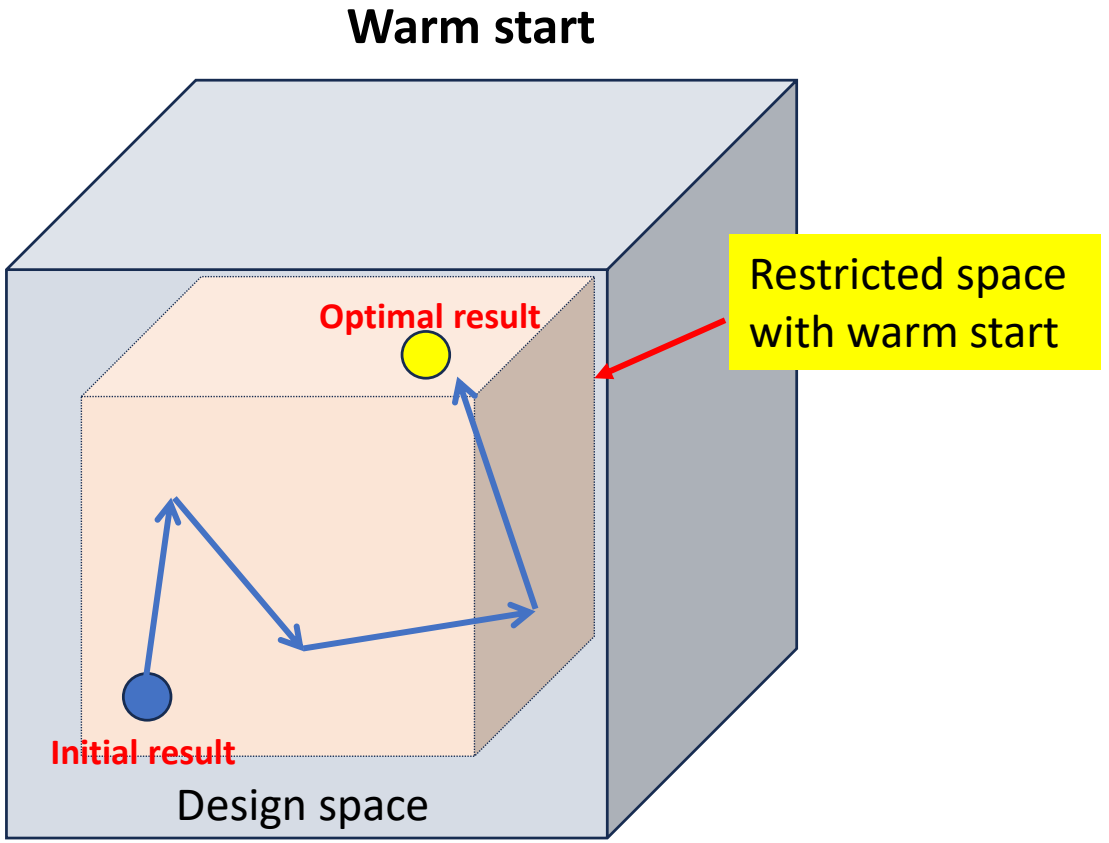


Target : 50% design TAT reduction

ML model, Cold start or Warm start ?

Cold needs to start parameter exploration without initial recommended range of parameter.
Warm start will start better start point for parameter exploration



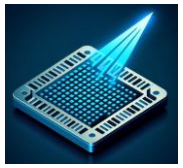


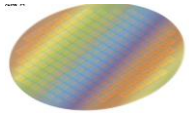
Warm start will find the optimal result earlier than cold start

How to utilize ML model for PPA exploration

Rapidus

Rapidus
Rapidus ML model





Design Specific Data

Process Specific Data

Release from Rapidus

Customer design

Rapidus ML model Achieve **better design convergence**

ML model is trained with design experience

Raads Rapidus AI-Assisted Design Solution

Updated ML model

Next Customer design

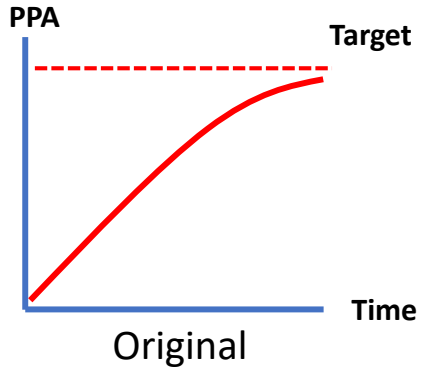
Updated ML model provides **further design convergence** advantage

ML model is **trained more** with design experience

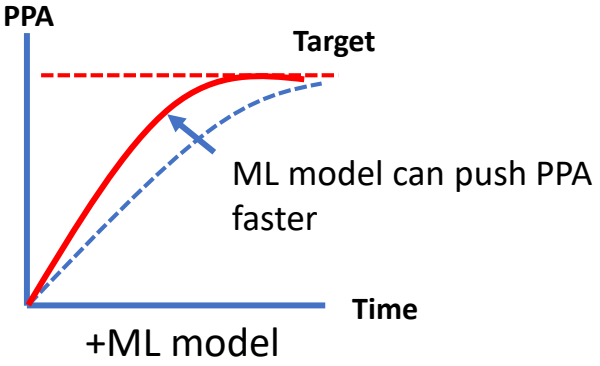
Raads Rapidus AI-Assisted Design Solution

Updated ML model2

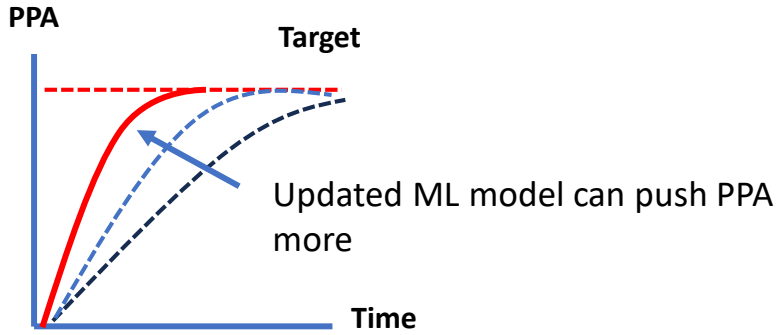
Further Next design



Original



+ML model



+updated ML model

ML model can grow up -> Customer get more benefit

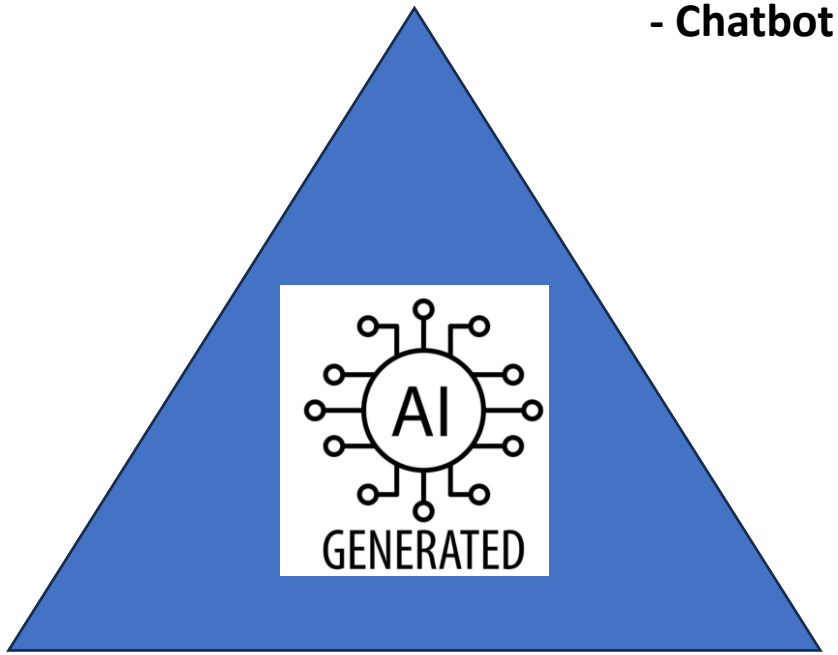
2

How does GenAI contributes chip design?

How does GenAI contributes chip design ?

Support expertise

- Designer / design knowledge
- Show guidance / prescription
- Chatbot based advisor



- Script generation
- Code generation
- Flow generation

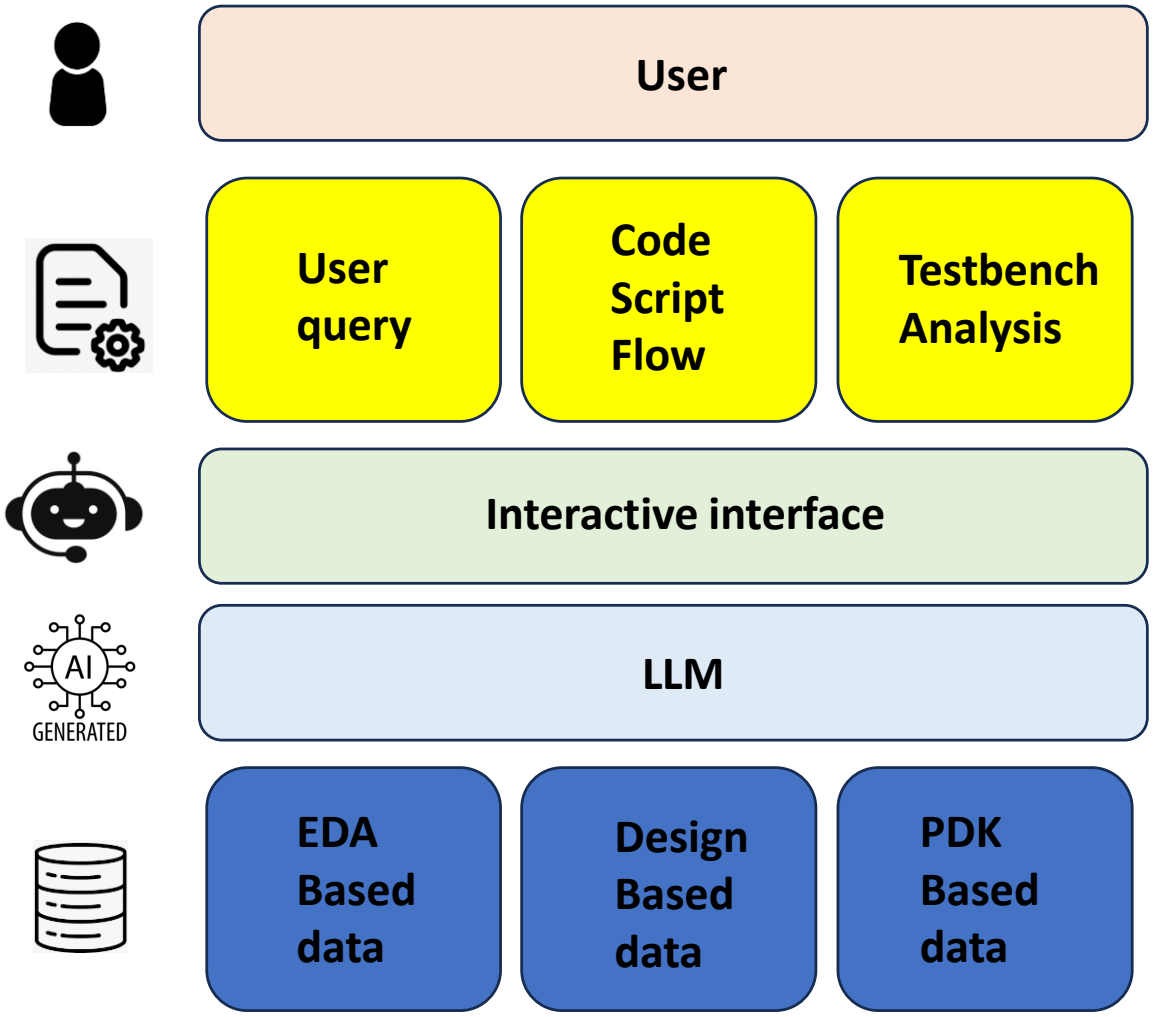
Support design

Support verification

- Testbench generation
- Check correctness
- Result analysis

Support expertise is effective because 100% correctness is not required.
How can we make confidence for GenAI based design ?

GenAI EDA side, design side, foundry side ?



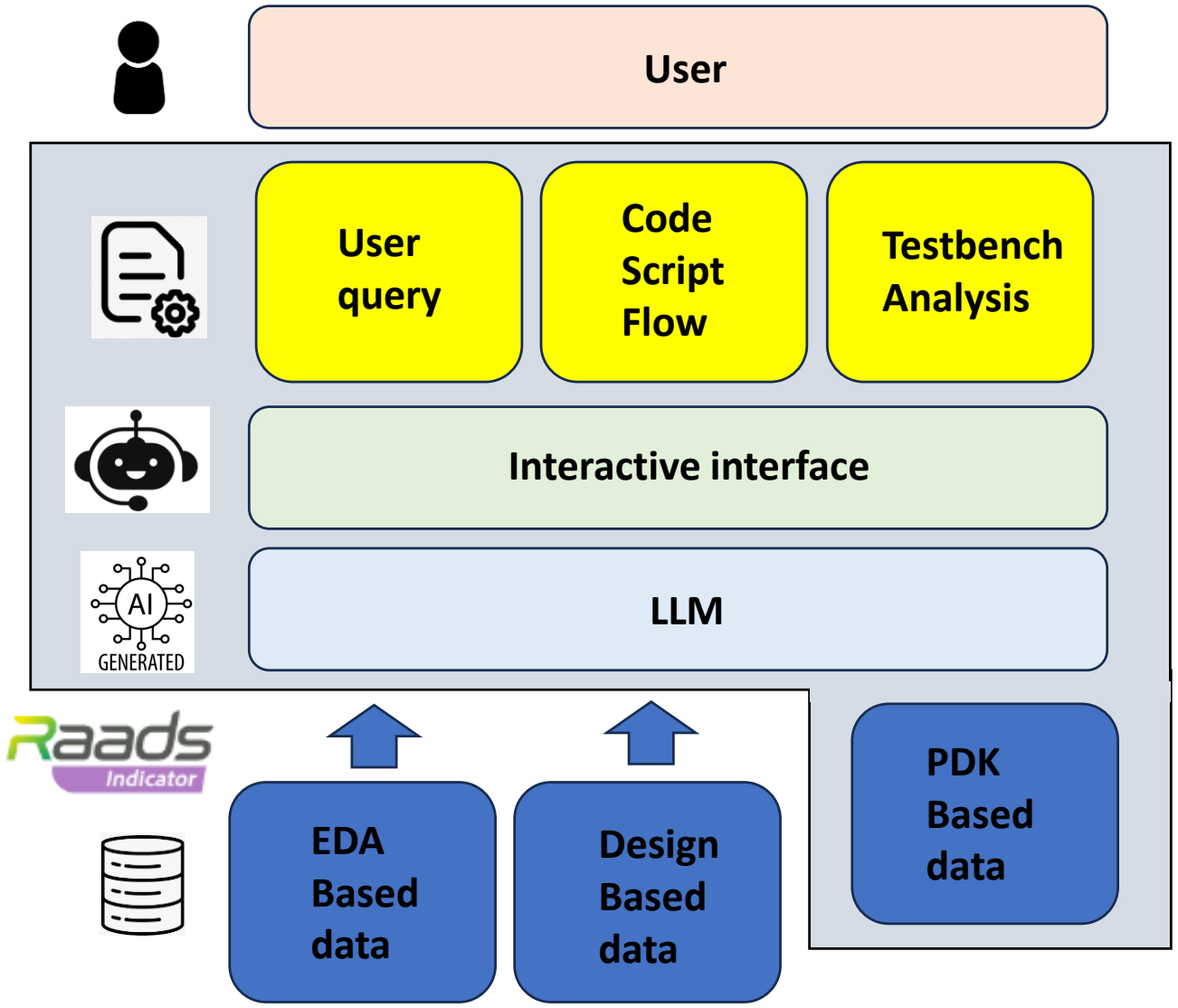
Contents for LLM learning

Foundry side :
- PDK related documents (Design manual)
- Process node related design knowhow
- Process node related design article

EDA side :
- EDA tool manual
- EDA tool knowhow / article
- EDA too user guide

Design side :
- Design specification
- Design knowhow / article
- Design related documents (Review document / Lesson & Learnt)

GenAI EDA side, design side, foundry side ?



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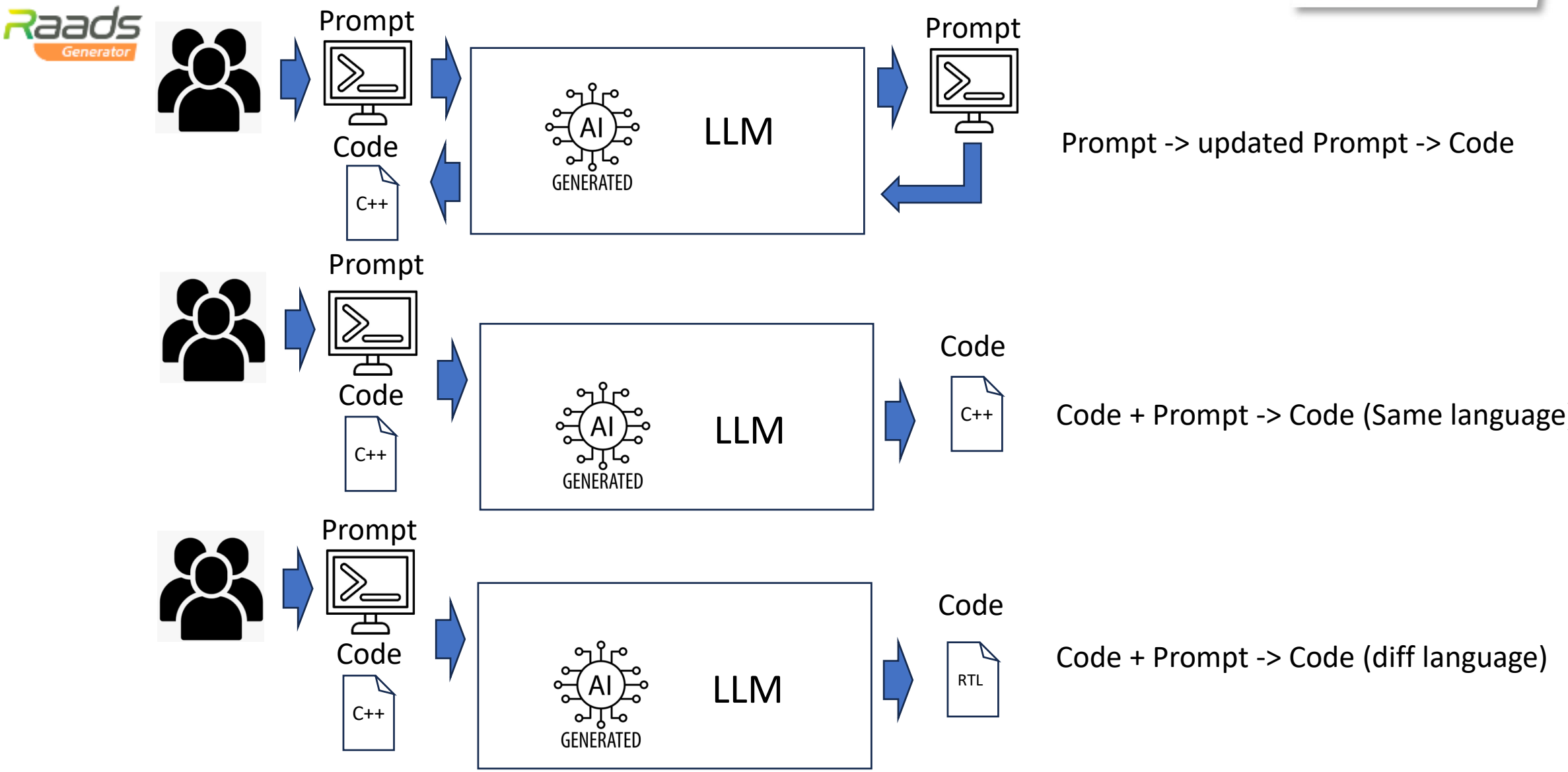
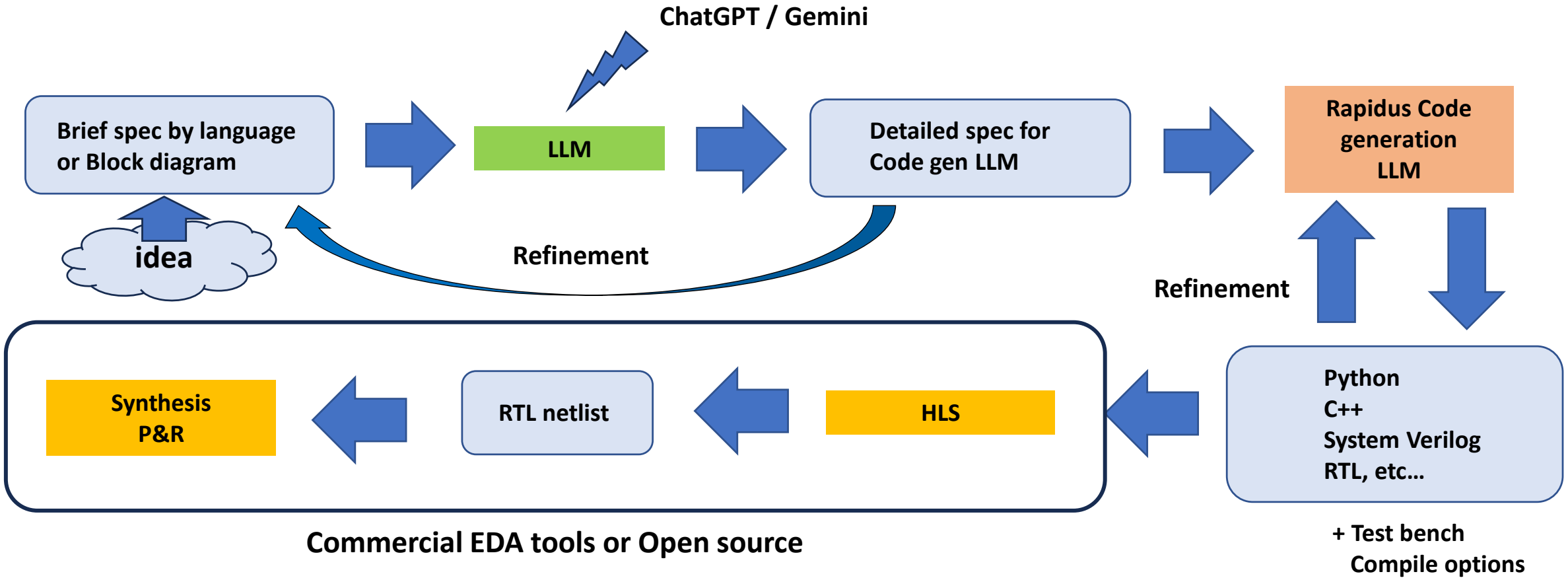
AI code generators for semiconductor



Many use cases are considered. Which is the most useful for designer ?

Raads.Genertor - use case

Opensource code generation LLM can be used academic / our partners -> Learned by many test cases
Other language LLM (ChatGPT / Gemini) can be used for specification improvement



Raads.Generator supports many types of interface, file format

3

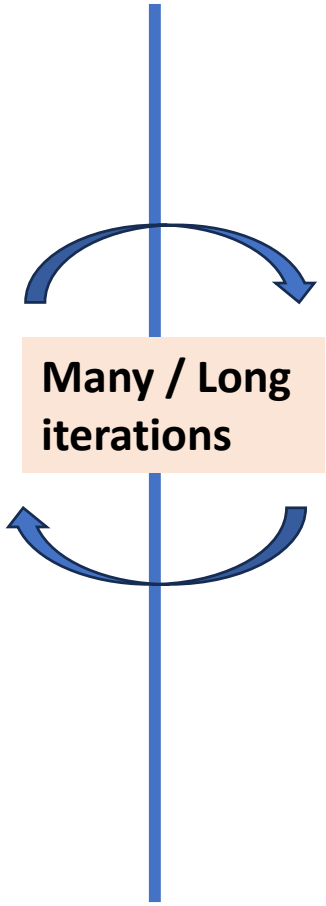
Importance of early PPA prediction

Importance of early PPA prediction

“Wide river” between logic and physical designers

Logical Designer

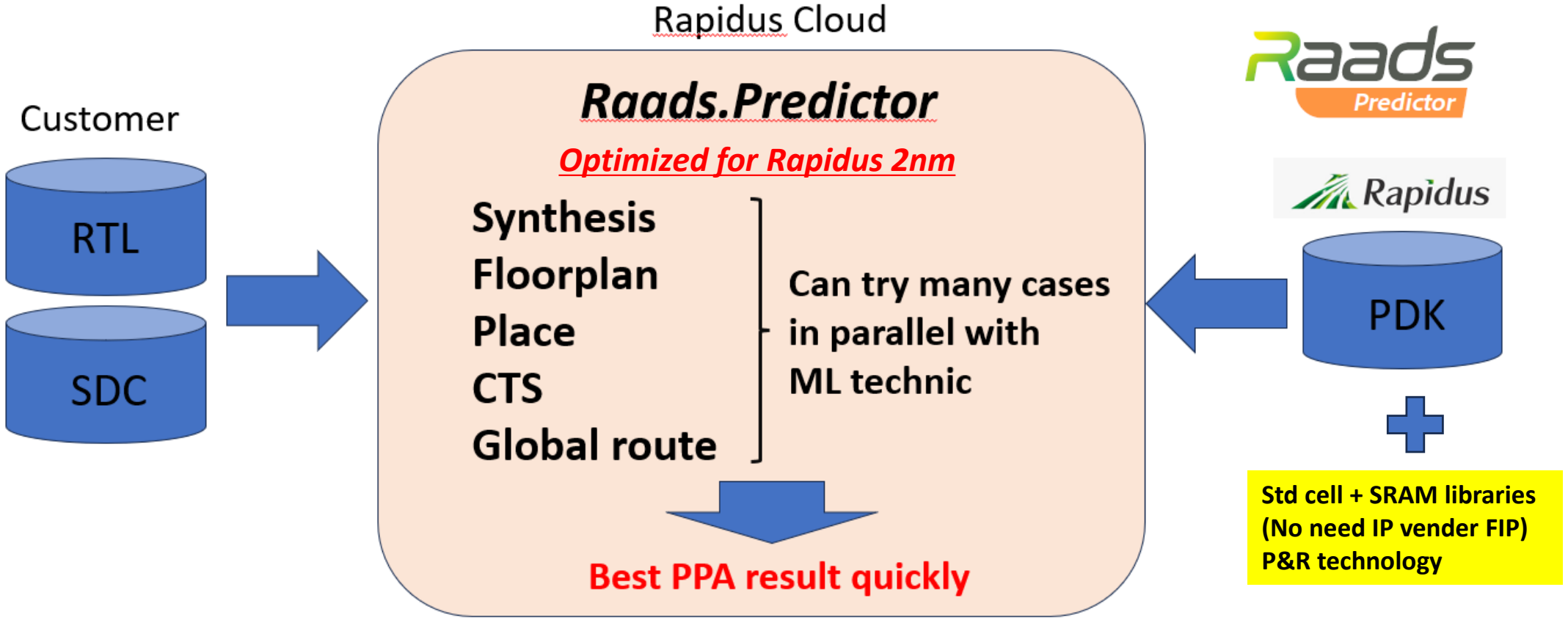
No way to confirm PPA with physical aware
Concern for long turn around time
Difficult to estimate the impact for physical Design
How to improve PPA ?
- Re-Synthesis with updated parameter
- Modify RTL
- Modify memory configuration



Physical Designer

Need time for setup trial PnR environment
- FIP (foundation IP)
- Tool license
- Setup tool environment
- Pipe clean the flow
- Try PnR with the data from logic designer
- Need exploration to find the best result

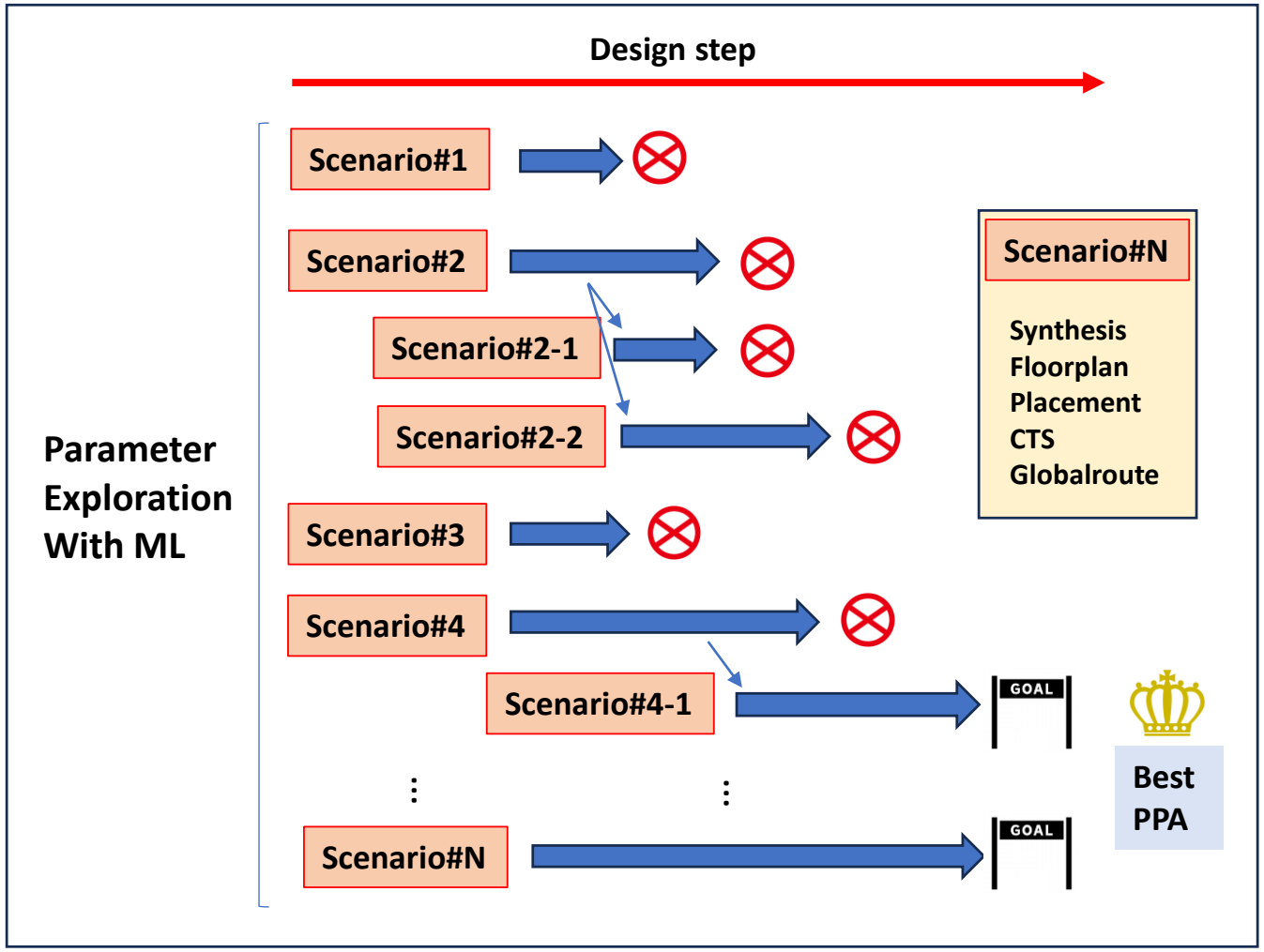
What is Raads.Predictor – early PPA prediction ?

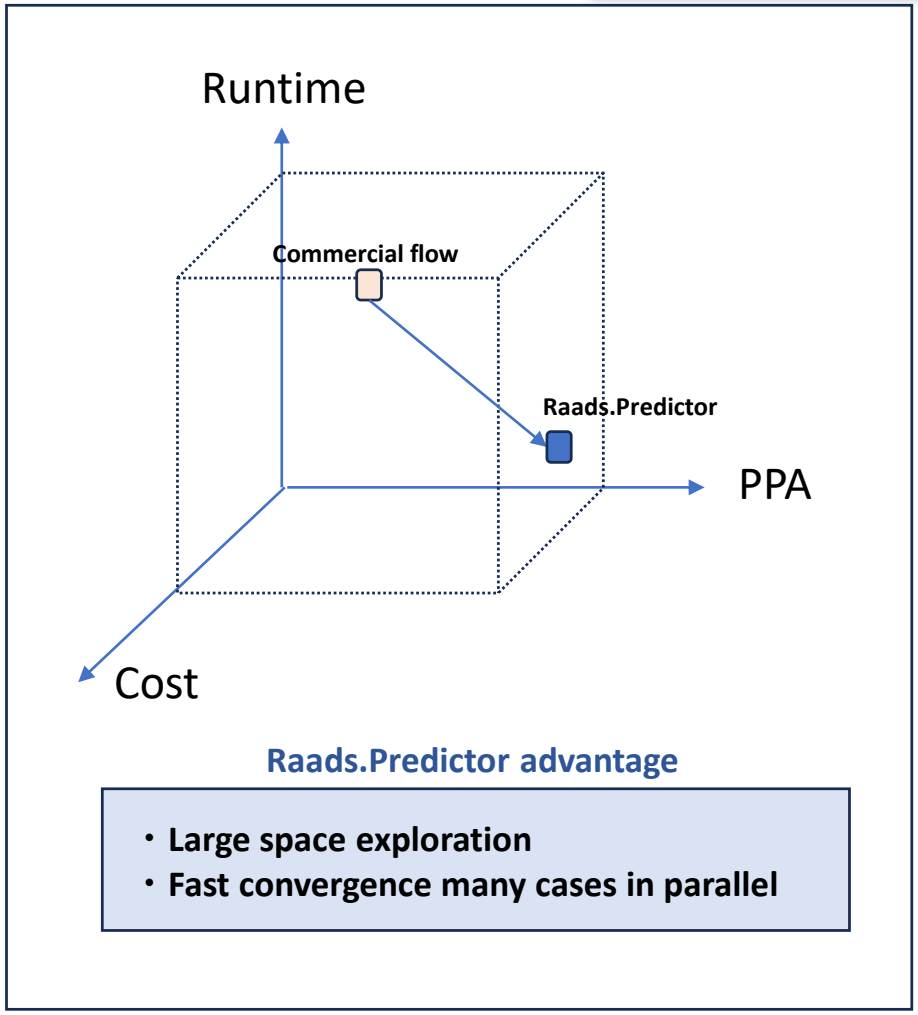


Features

Out of box environment for PPA prediction → No physical design experience
Physical aware easy and quick RTL quality improvement at logic designer side

ML/AI contribution for design space exploration





Raads.Predictor advantage

- Large space exploration
- Fast convergence many cases in parallel

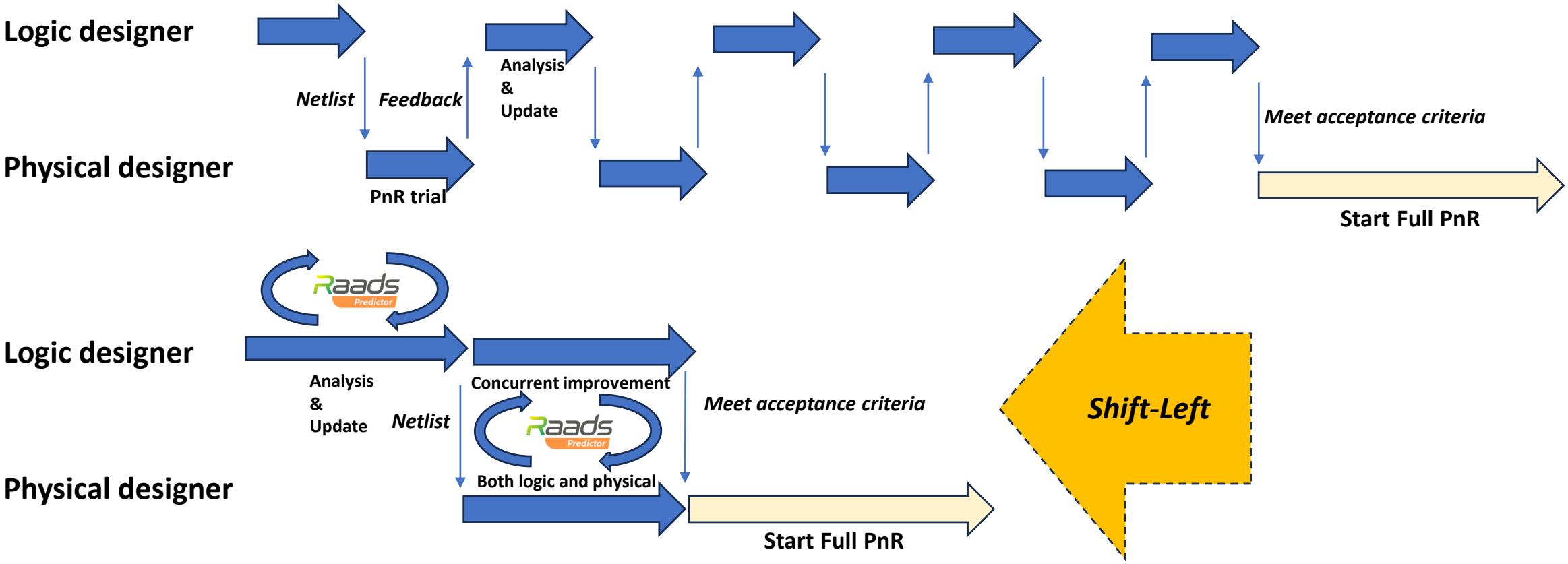
Early PPA prediction derives best PPA result with short TAT

- Easy to find logic performance at logic designer side

- Fast pathfinding with large space exploration

Early PPA prediction benefits between logic and physical designers

- Can be utilized physical aware analysis at logic designer side
- Provides same infrastructure to communicate between logic and physical designer



Achieve “Shift-Left” approach for large scale chip design

4

AI-based physical prototyping

Importance of AI-based physical prototyping – Logic hierarchy and partition

Raads Manager

The determination of Logical hierarchy and corresponding physical partition is key point for large scale SoC design.

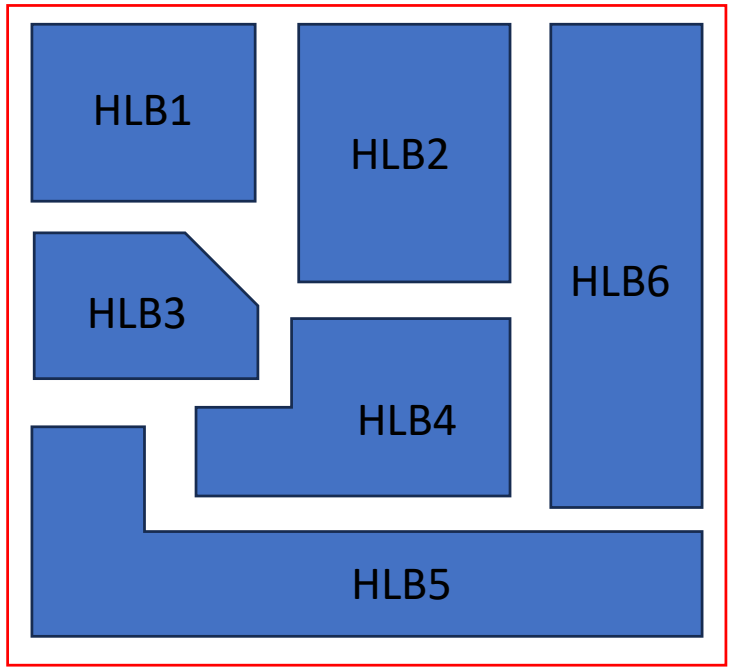
- Many trials are, many resource are consumed
- Physical designer needs negotiation with logic designer for logic hierarchy update

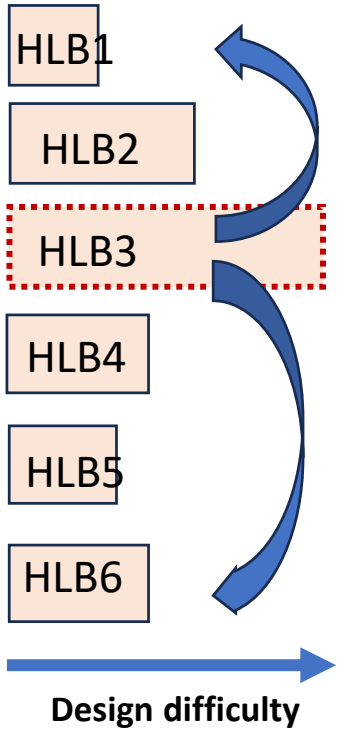
But, is this the best partition to achieve short design cycle ?

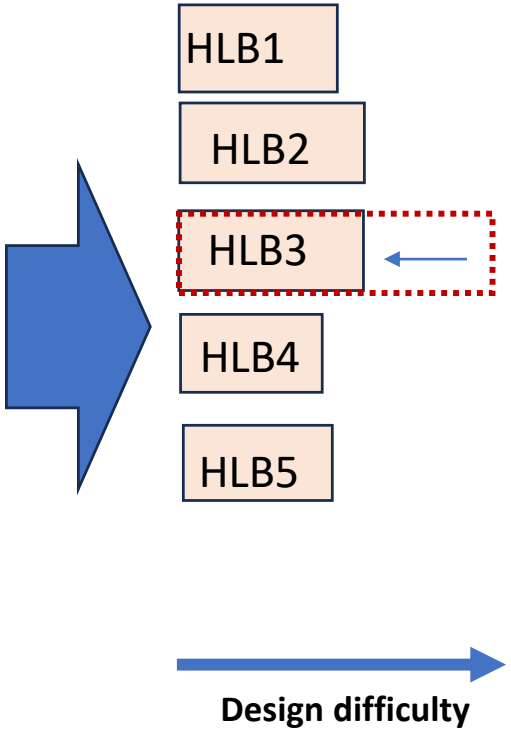
Raads.Manager concept

- Automatic block partition to achieve fast design convergence
- Evaluate “design convergence difficulty” when decide block partition

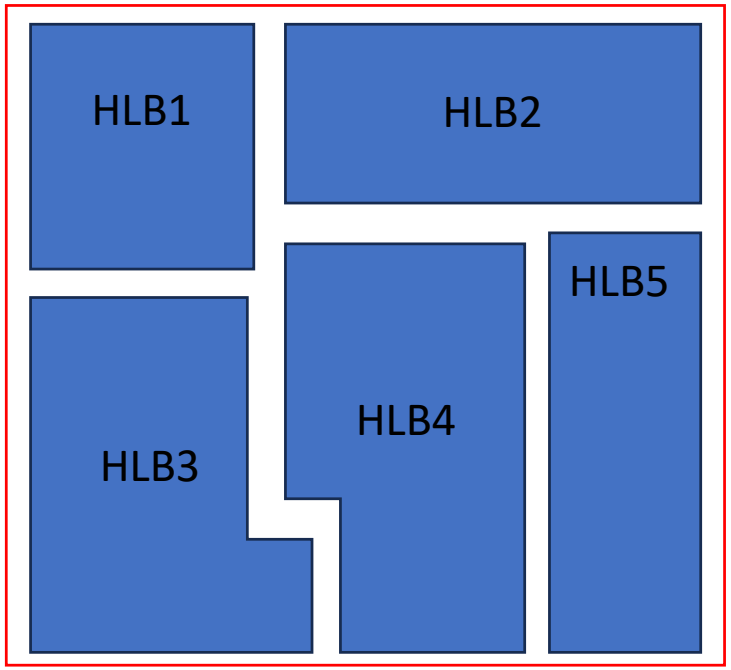
Example of worse physical partition







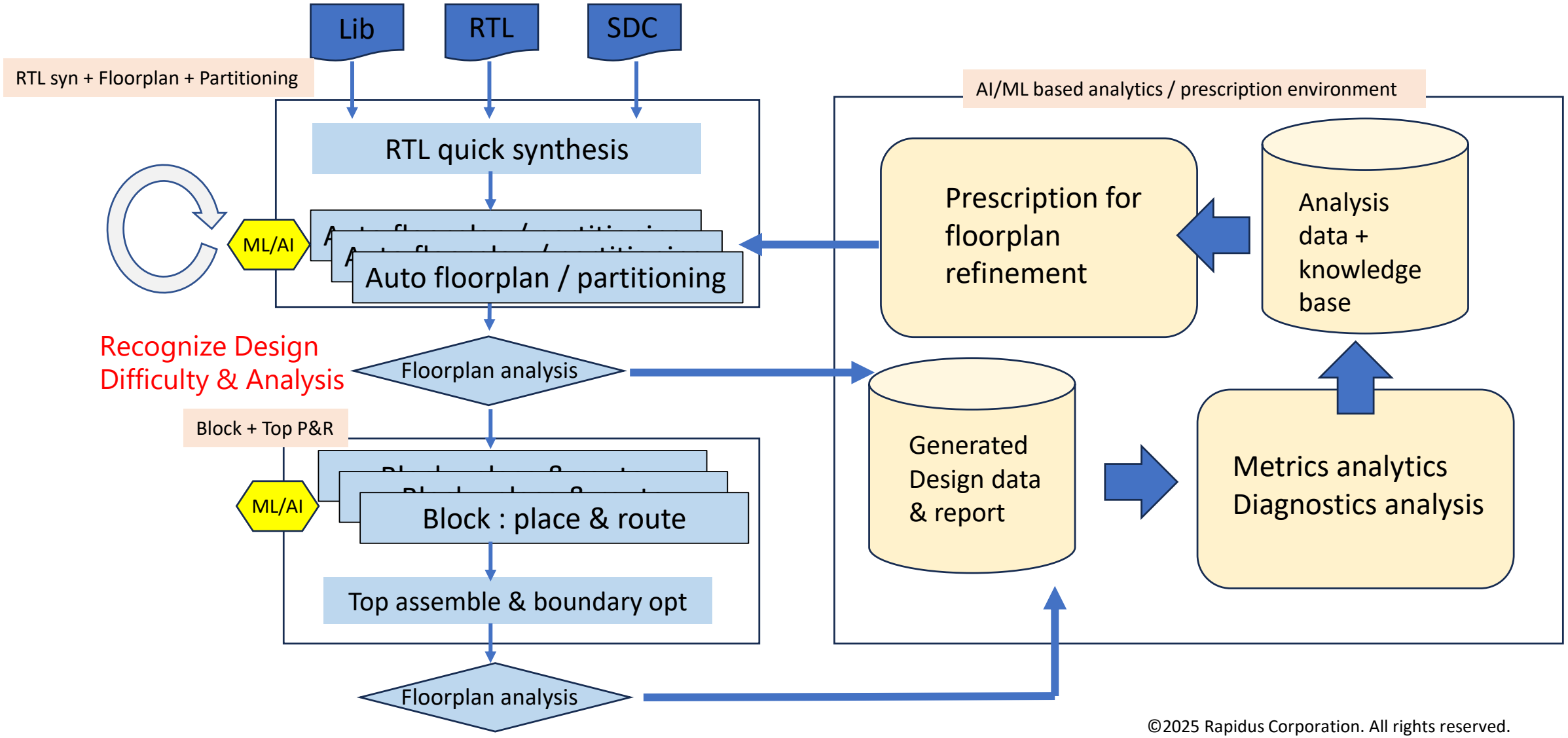
Better physical partition with repartitioning



Achieve equalization of “design convergence difficulty” -> Fast design convergence

Raads.Manager

- Achieve full auto hierarchical flow without designer experience
- Apply automatic iteration for partitioning and full block implementation flow with ML/AI



Raads development schedule and message

- Rapidus is developing each Raads item with major EDA venders, design partners and academic societies.
- The most of Raads items will be released by 2025 12/E, but we will improve continuously and add new features.
- Rapidus find beta customer to evaluate, some capabilities will be available earlier than the above.
  (The feedback from customers are very important)

Rapidus achieves halve design cycle time with

Raads
Rapidus AI-Assisted Design Solution

and
collaborate with you soon !!

Acknowledgement

This presentation is based on results obtained from “Research and Development Project of the Enhanced Infrastructures for Post-5G Information and Communication Systems” (JPNP20017), commissioned by the New Energy and Industrial Technology Development Organization (NEDO).