[ASP-DAC 2025]

Advanced Packaging Technology and Design Methodology for Next Generation Chiplets

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Outline

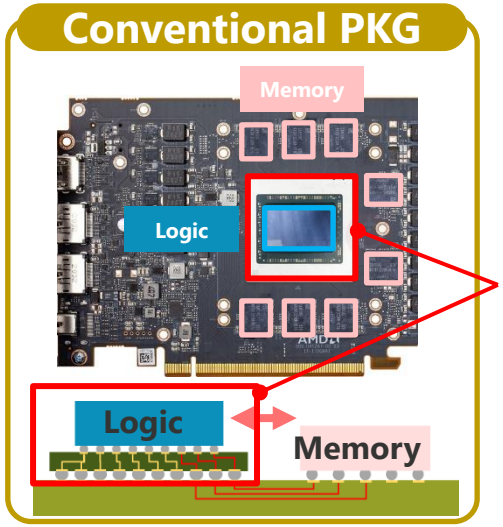
1. Chiplet Package Requirements Driven by Big Data
2. Roadmap of Chiplet Packages
3. Design Considerations for Chiplet Packages

1 Chiplet Package Requirements Driven by Big Data

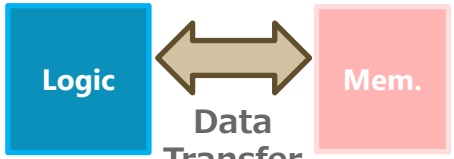
Big Data

New Natural Resource

HW Requirement: Higher Data Transfer Rate

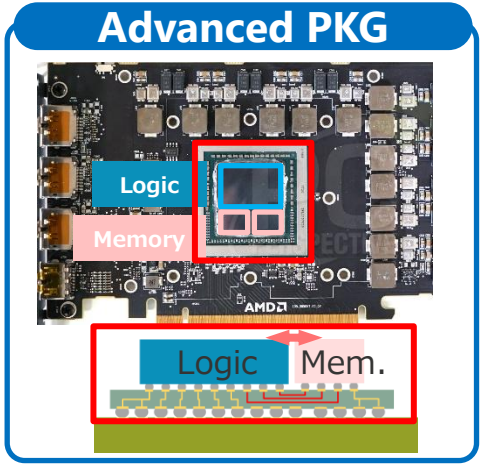


Source of Photos: AMD



HBM

50x



10x

PCIe
LPDDR

10x

DDR

20x

Multi-core CPU

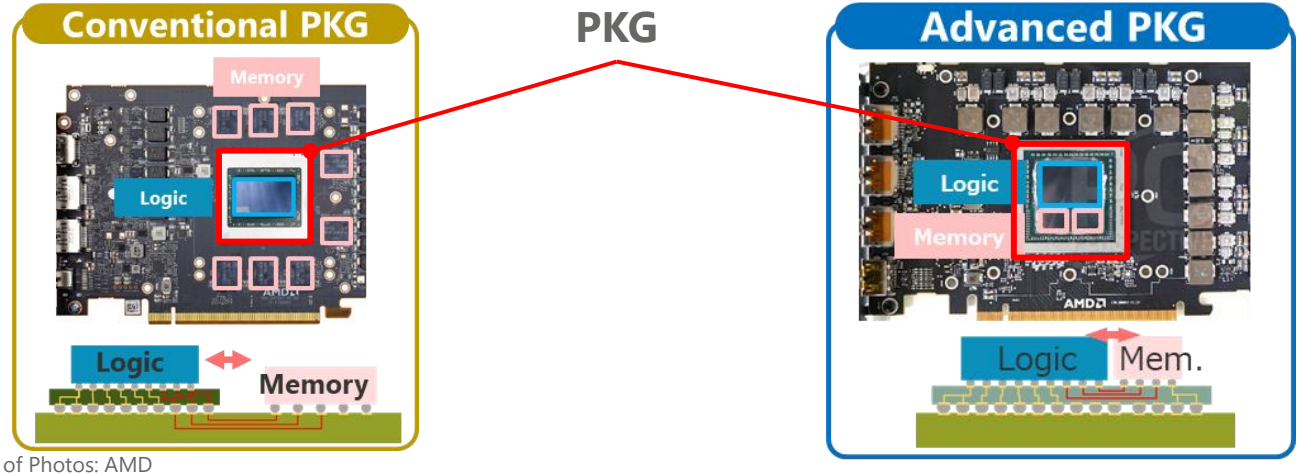
Multi tasks
Larger cash memory

1990 2000 2010 2020 2030

Allows higher data transfer rate by shortening the distance btw logic and memories.

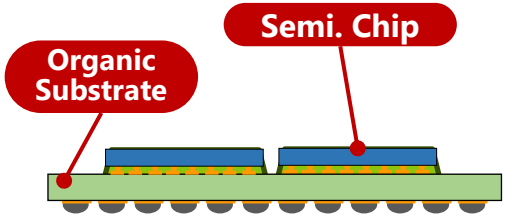
Source of Photos: AMD

Evolution of Semiconductor Packages

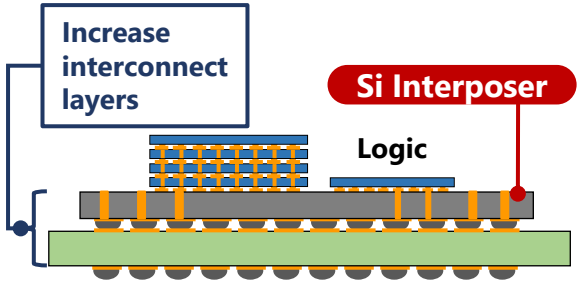


Source of Photos: AMD

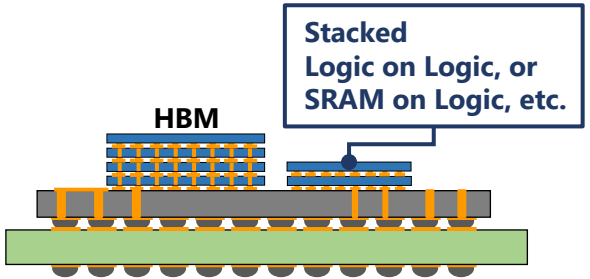
2D PKG



2.5D PKG

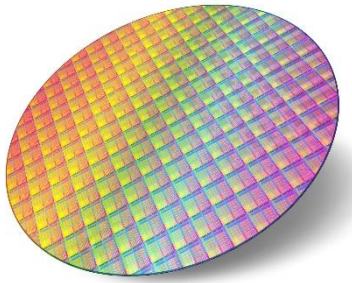


3D PKG



In an Era When PKG Determines Performance

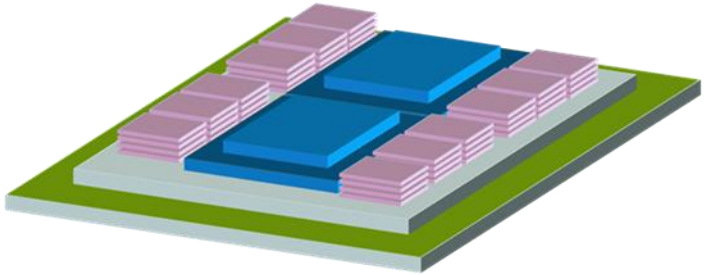
Front-end



Miniaturization of Tr.

Performance

Back-end (PKG)



To bring out performance of advanced node transistors, chips should be integrated into advanced package.

Integration with Chips

Performance

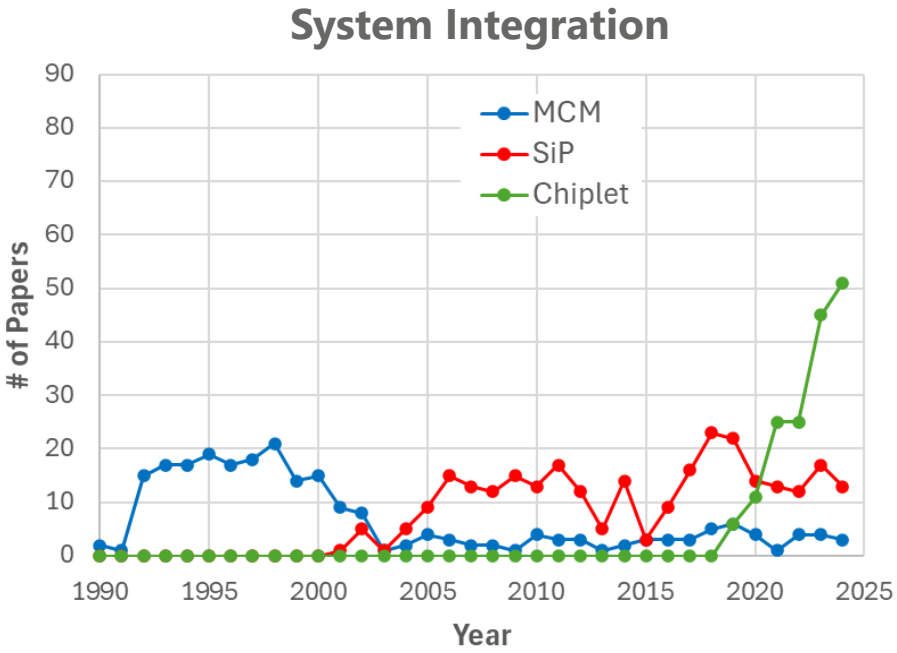
PKG determines performance

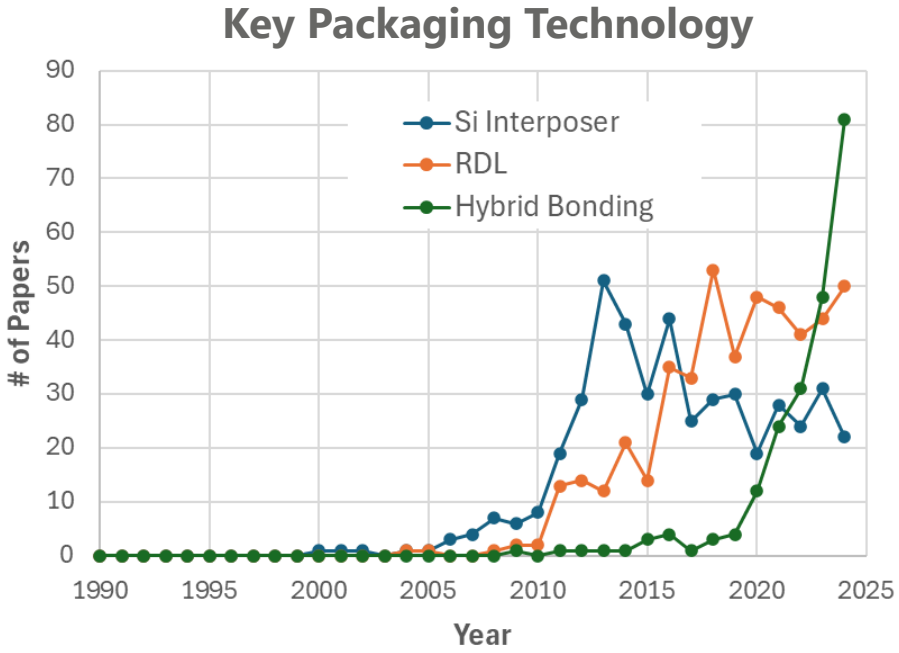
2

Roadmap of Chiplet Packages

Big Waves on Advanced Packaging Technology

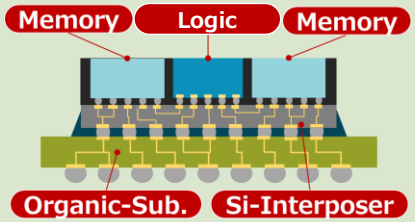
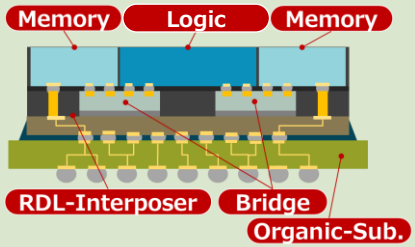
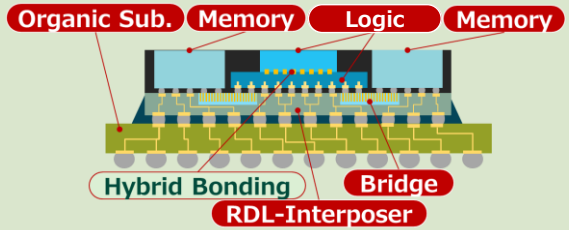
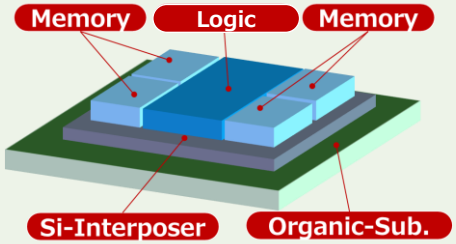
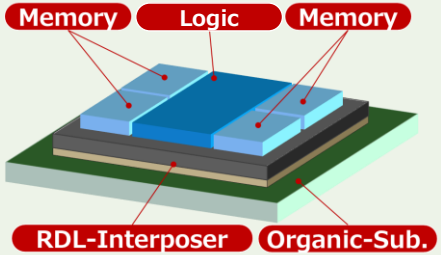
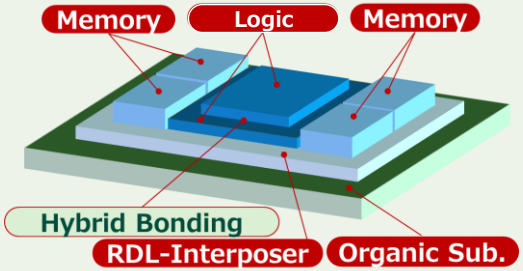
- MCM(1992-) -> SiP(2001-) -> **Chiplet (2019-)**
- Si Interposer(2006-) -> RDL(2011-) -> Hybrid Bonding(2020-)





Source: ECTC Data base by IEEE Xplore

Chiplet Packages

	Gen1 2.5D /Si Interposer	Gen2 2.xD/RDL Interposer	Gen3 3D/Hybrid Bonding
Cross Section			
Tile Image			

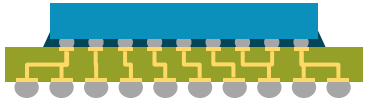
3

Design Considerations for Chiplet Packages

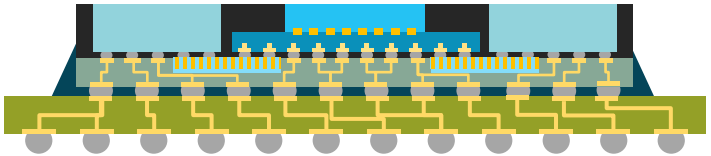
Package Design Requirements

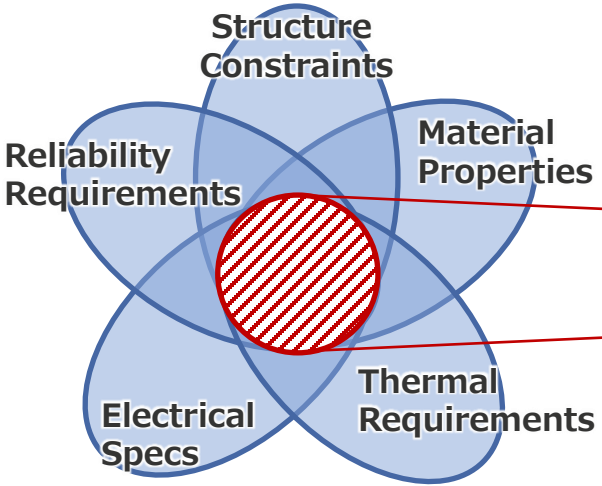
Design difficulty due to complex structure

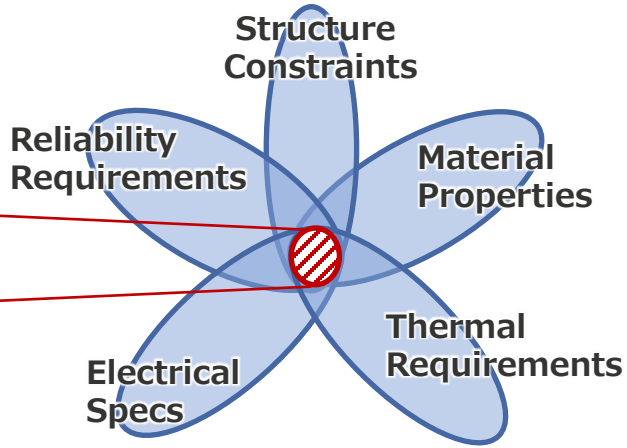
Single Chip Package



Chiplet Package

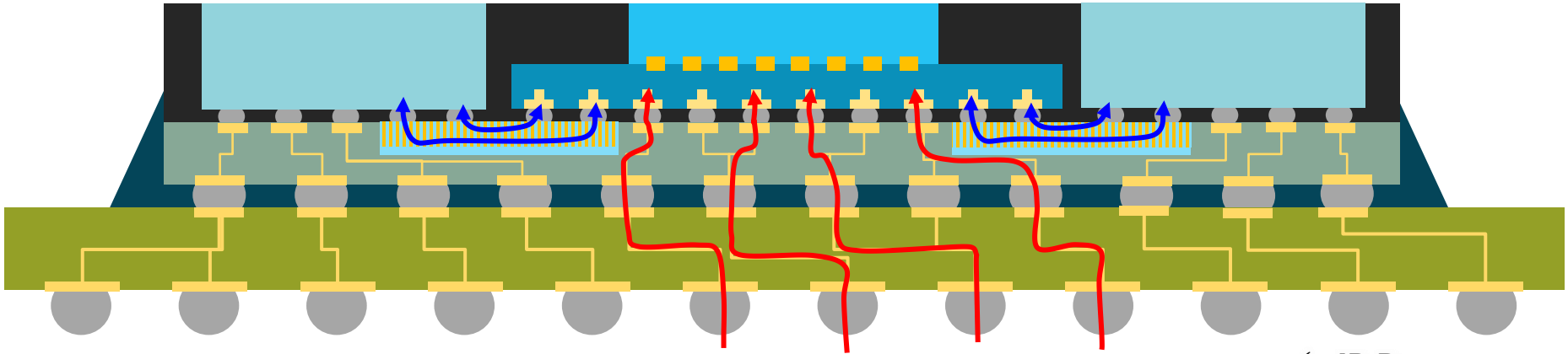




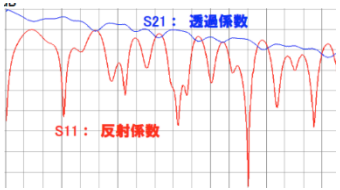


Design Consideration: Electrical Specs

Electrical Specs | **Structure Constraints** | **Reliability Requirements** | **Thermal Requirements** | **Material Properties**

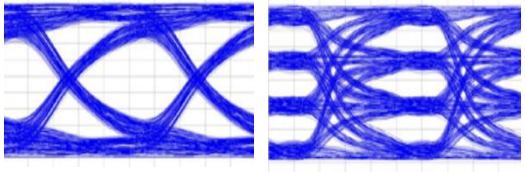


✓ **S-Parameter**



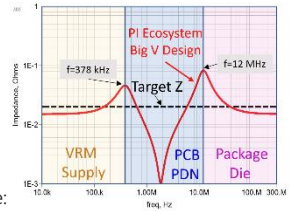
Source:
https://edn.itmedia.co.jp/edn/articles/1510/30/news007.html

✓ **Eye Pattern**



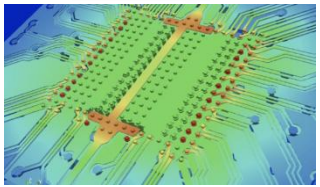
Source:
https://www.signalintegrityjournal.com/articles/432-s-parameters-signal-integrity-analysis-in-the-blink-of-an-eye

✓ **PDN Impedance**



Source:
https://www.signalintegrityjournal.com/blogs/12-fundamentals/post/2108-power-integrity-fundamentals-impedance-vs-frequency

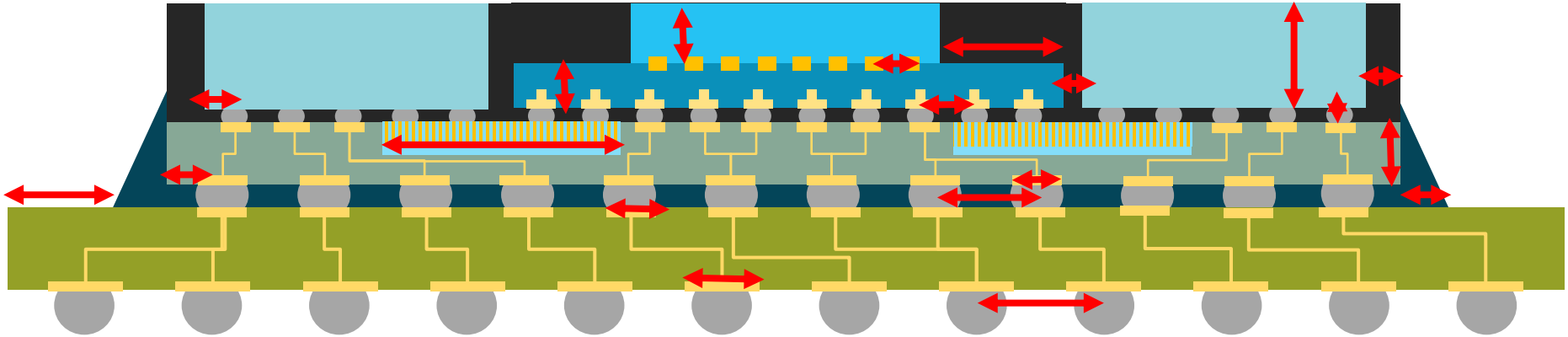
✓ **IR Drop**



Source:
https://community.cadence.com/cadence_blogs_8/b/pcb/posts/system-analysis-knowledge-bytes-celsius-powerdc-methodology-to-accurately-model-dc_2d00_dc-converters

Design Consideration: Structure Constraints

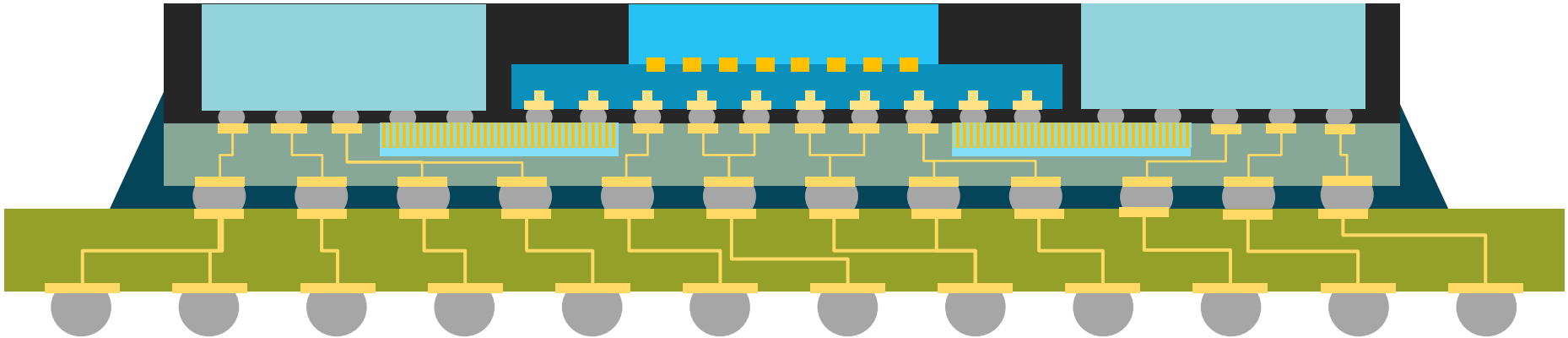
Electrical Specs | **Structure Constraints** | Reliability Requirements | Thermal Requirements | Material Properties



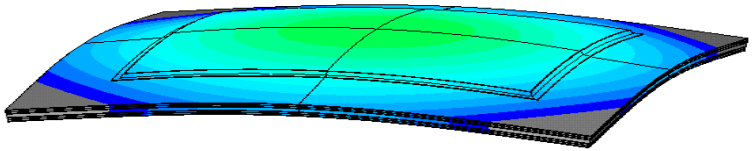
✓ **Assembly rules for high yield and low cost**

Design Consideration: Reliability Requirements

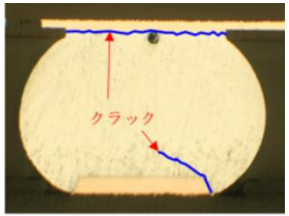
Electrical Specs | Structure Constraints | **Reliability Requirements** | Thermal Requirements | Material Properties

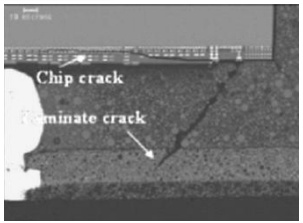


✓ **Control warpages caused by CTE mismatch**



✓ **Avoid cracks occurred by mechanical stress**





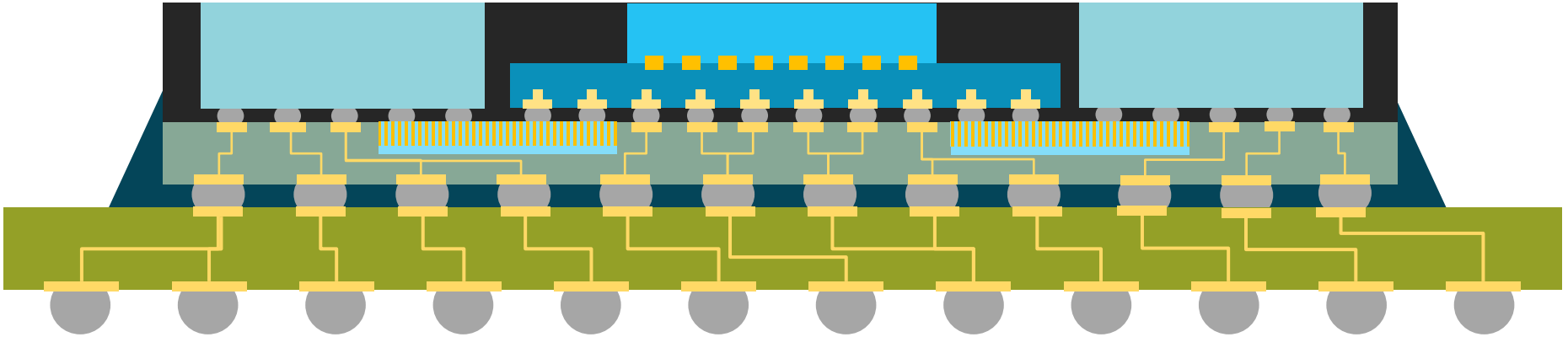
Source: https://www.wti.jp/contents/blog/blog201110.htmtate

✓ **Prevent ion migration**

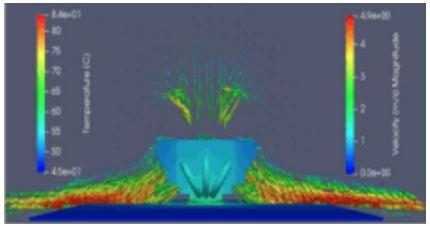
Source: https://j-ras.com/ecm.html

Design Consideration: Thermal Requirements

Electrical Specs | **Structure Constraints** | **Reliability Requirements** | **Thermal Requirements** | **Material Properties**

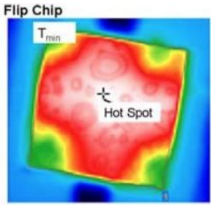


✓ **Design heat dissipation**



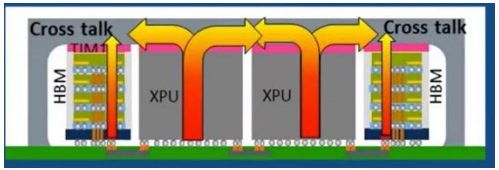
Source: https://www.cadence.com/en_US/home/resources/white-papers/thermal-and-stress-analysis-of-3d-ics-with-celsius-thermal-solver-wp.html

✓ **Avoid hot spots**



Source: https://www.researchgate.net/figure/Simulation-and-measurement-of-thermal-field-on-chip-surface-of-LED-packages_fig2_261420415

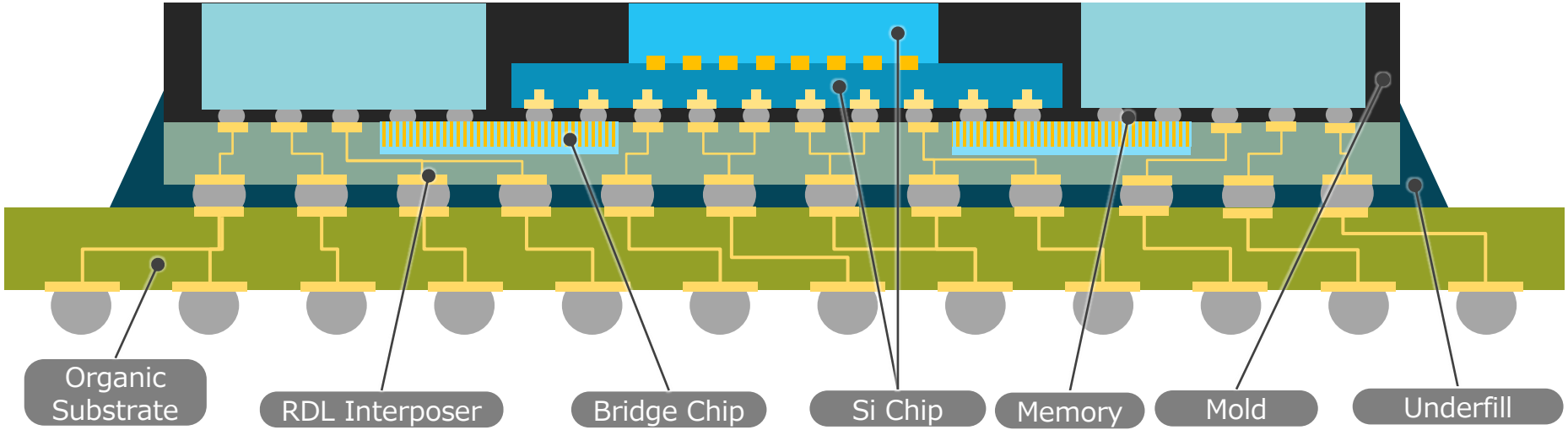
✓ **Reduce thermal crosstalk**



Source: https://www.youtube.com/watch?v=0gPSbZqbXUg

Design Consideration: Material Properties

Electrical Specs | Structure Constraints | Reliability Requirements | Thermal Requirements | **Material Properties**

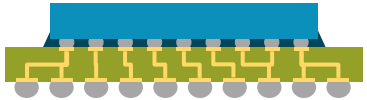


- ✓ **Select suitable materials for electrical properties.**
- ✓ **Select a material set that is optimized for warpage, heat dissipation, and reliability.**

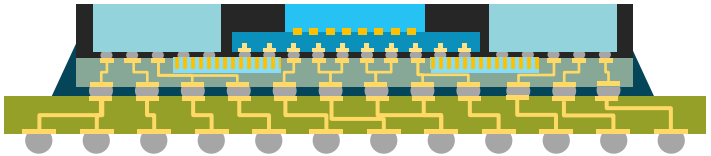
PKG Design with ADK (Assembly Design Kit)

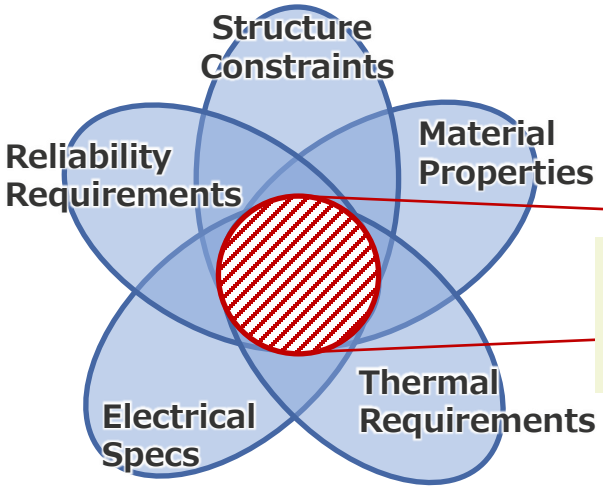
Design difficulty due to complex structure

Single Chip Package

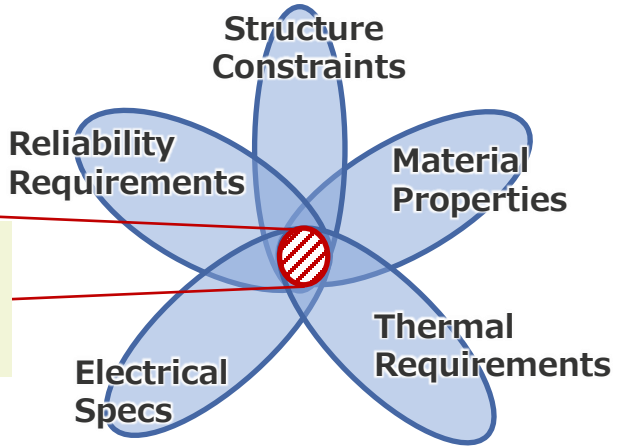


Chiplet Package





ADK reduces design difficulty and expects to shorten the design period.



Summary

- ✓ **Big Data is driving advanced packaging technologies. Advanced (Chiplet) packages improve computing performance.**
- ✓ **Chiplet packages evolute as 2.5D, 2.xD and 3D packages to improve data transfer rates between logic and memory.**
- ✓ **Chiplet package design is becoming increasingly difficult due to the complexity of the structure and material combinations.**
- ✓ **ADK (Assembly Design Kit) really reduces the design difficulty of complex chiplet packages and expects to shorten the design period.**


Rapidus