ASP-DAC 2025

Revisit MBFF: Efficient Early-Stage Multi-bit Flip-Flops Clustering with Physical and Timing Awareness

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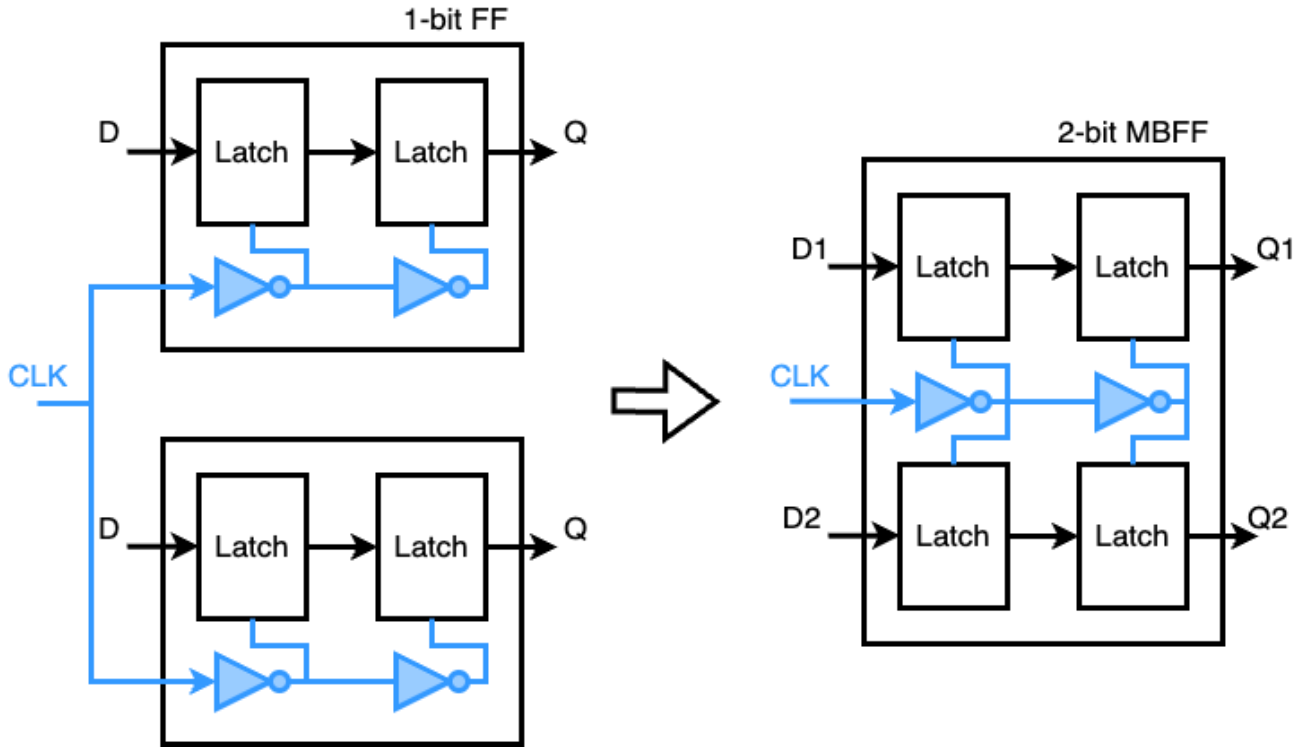
Outline

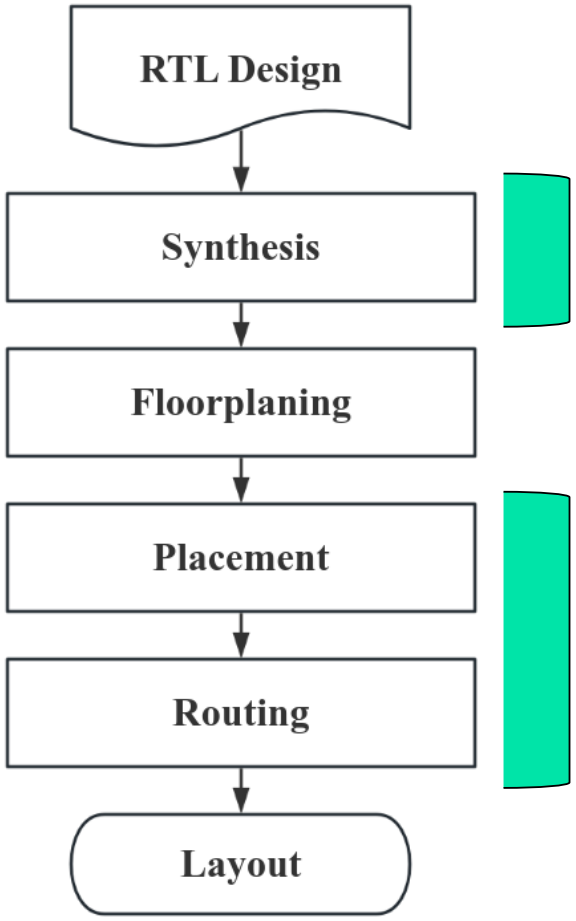
- Background
  - What is Multi-Bit Flip-Flop (MBFF)?
  - Stage-related Clustering Result
- Our Approach
  - Step 1. Flip-Flop Distance Estimation
  - Step 2. Signal Path Timing Estimation
  - Step 3. MBFF Clustering Algorithm
- Experiment Setup and Results
- Conclusions

What is Multi-Bit Flip-Flop (MBFF)?

- By clustering FFs together
  - Share a common clock pin
  - Save internal inverters
- Advances by clustering
  - Simplify clock tree structure
  - Reduce power

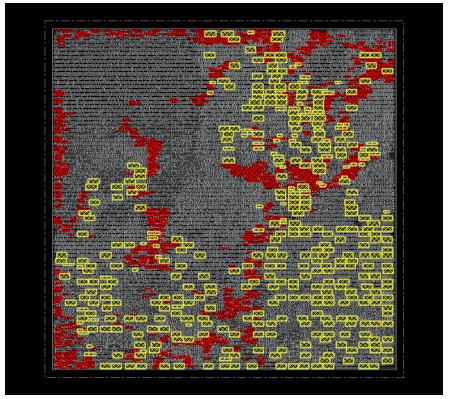


Stage-related Clustering Result

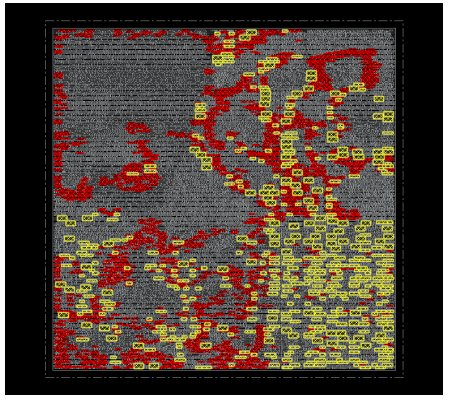


Logic-based clustering

Physics-based clustering



after synthesis



after placement

Design: or1200

Red: 1bit FF Yellow: MBFF

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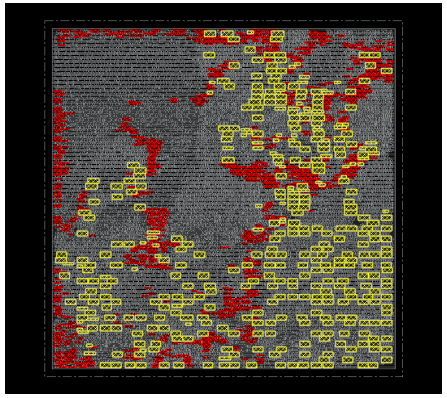

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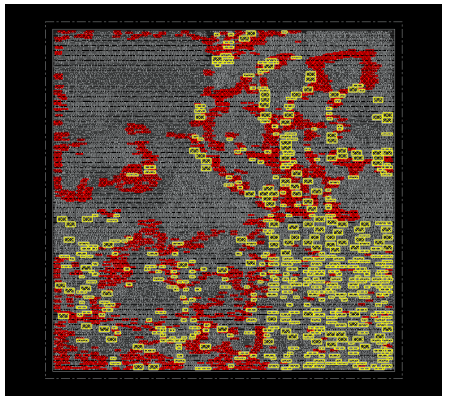

after placement

	Clustering after synthesis	Clustering after placement
P_{clk}	50.88	57.87
P_{total}	116.34	125.71
WNS	-0.172	-0.153
TNS	-289.664	-226.893
Bits/Flop	2.709	1.732

Design: or1200

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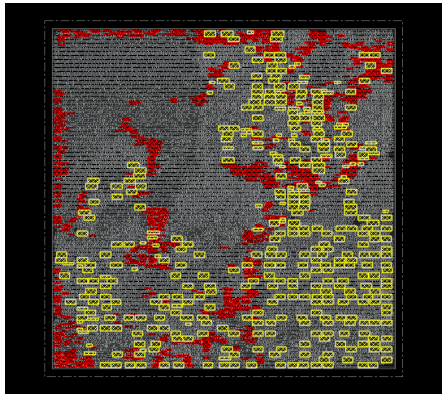
Stage-related Clustering Result



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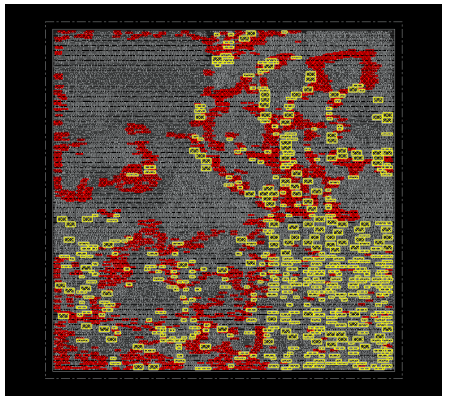

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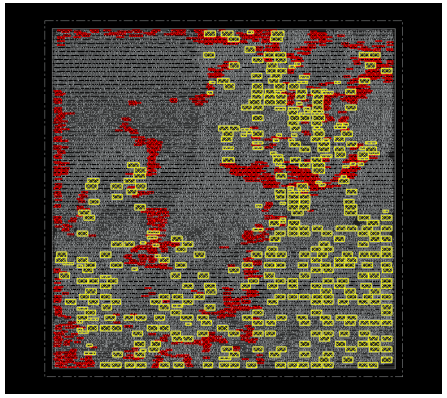

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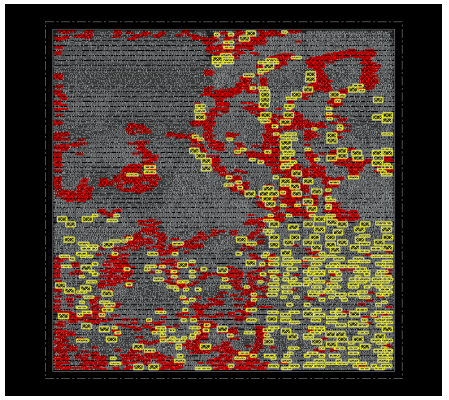

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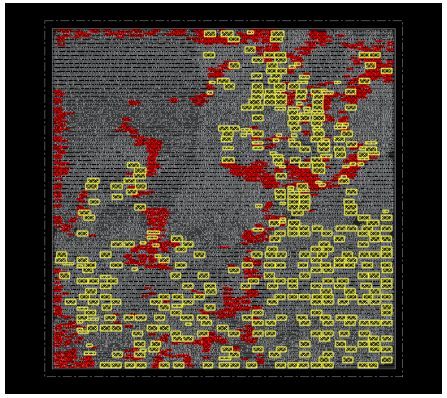

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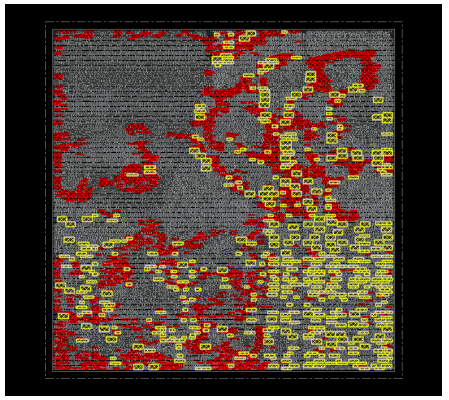

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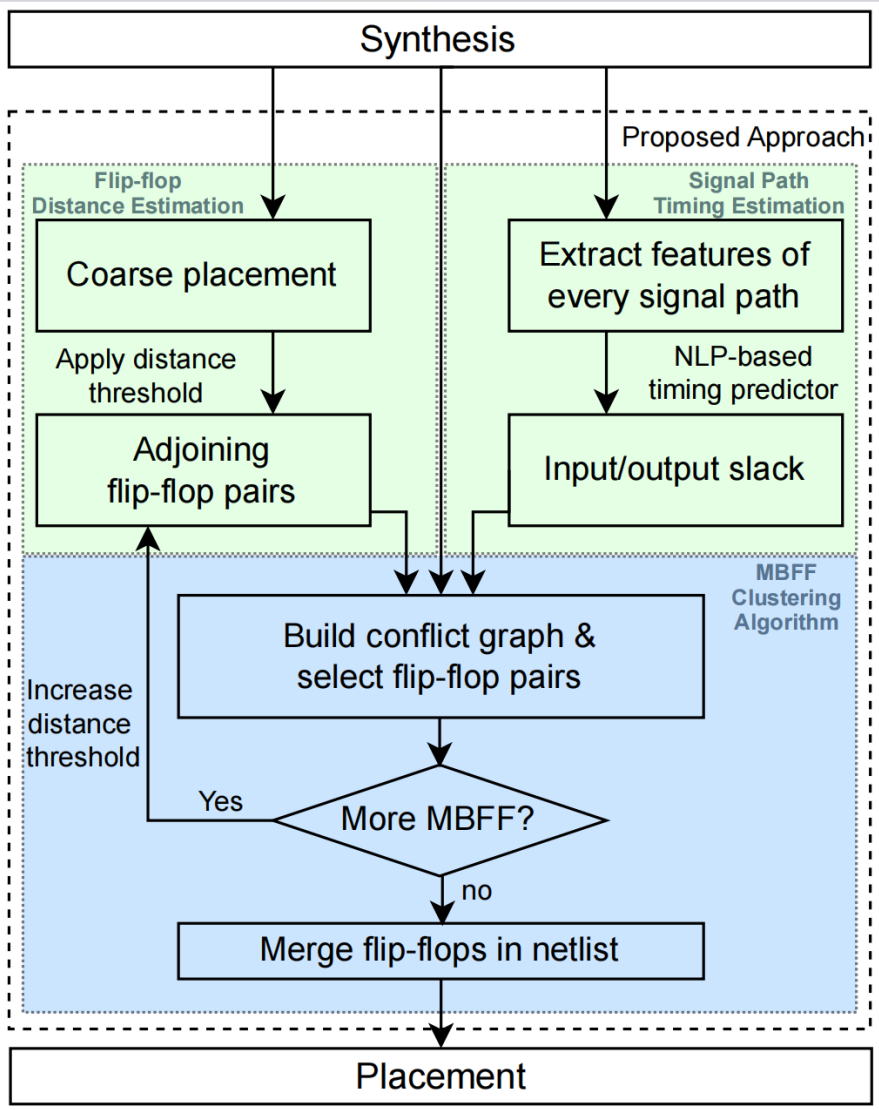
Our Approach



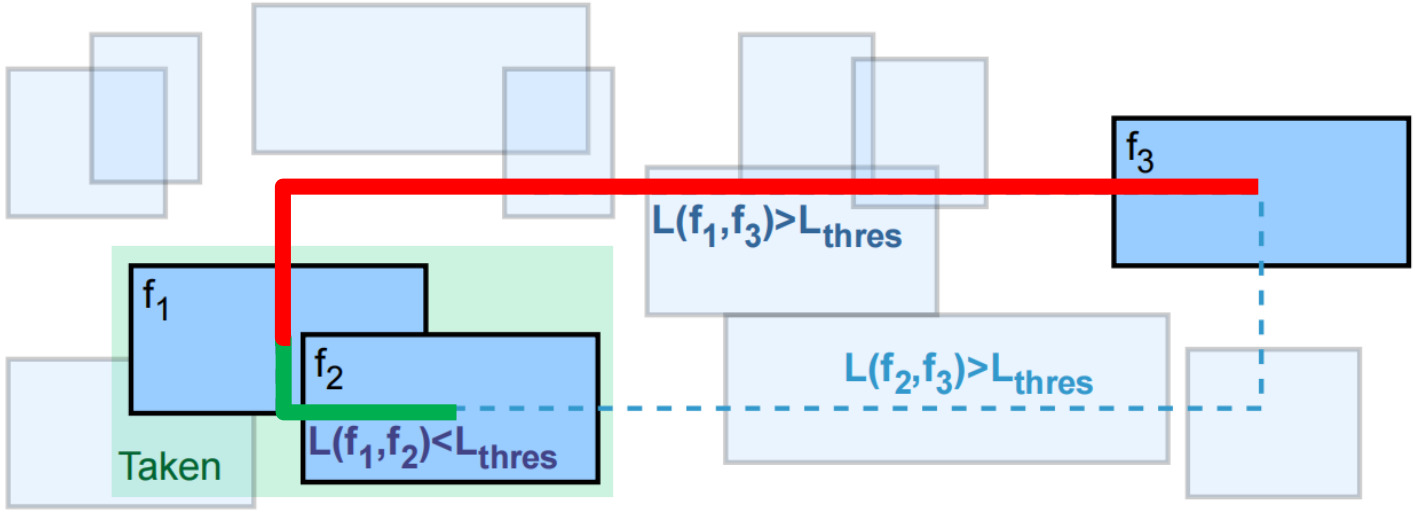
Early-stage timing awareness

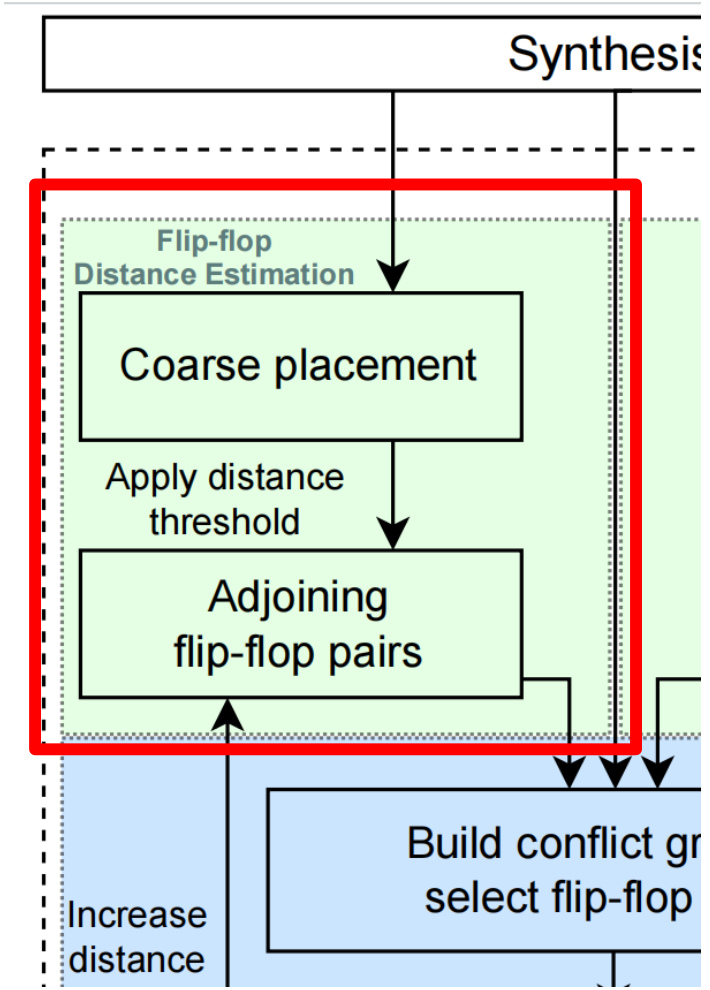
Early-stage physical awareness

MBFF clustering algorithm

Step 1. Flip-Flop Distance Estimation

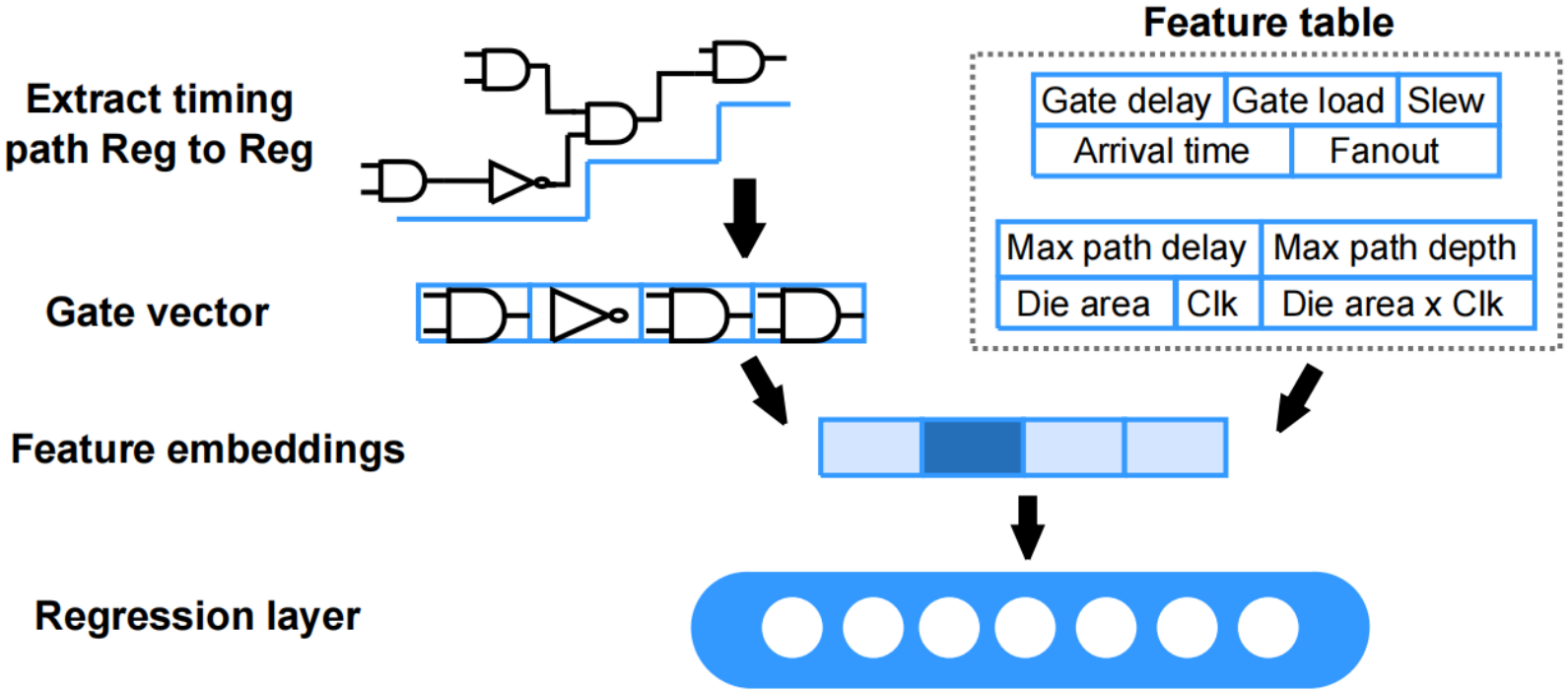
- Consider physical locality
  - FF with shorter distance will result in better timing
- Run placement in floorplan mode
  - ~87 times speedup compared to normal placement
- Calculate Manhattan distance
  - Apply threshold distance to filter FF combinations

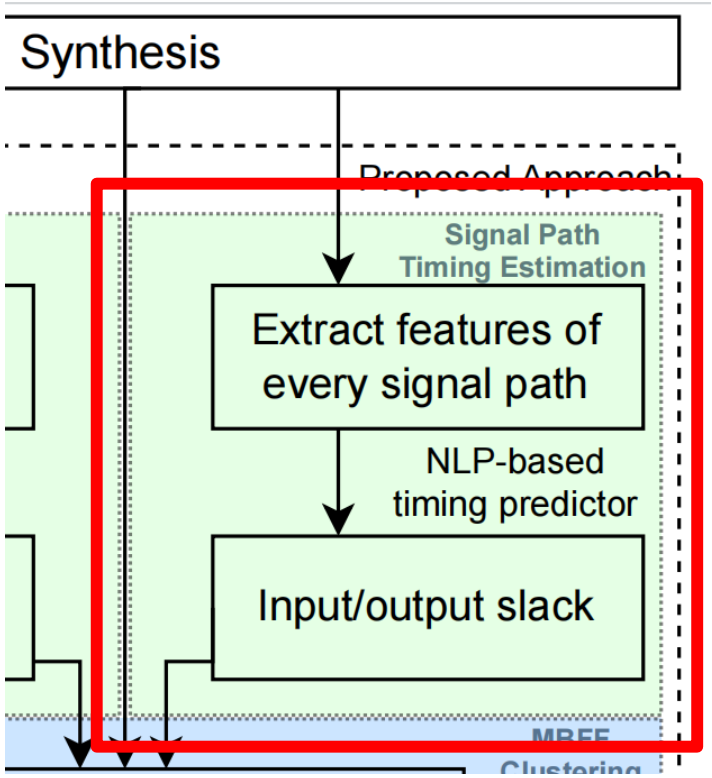




Step 2. Signal Path Timing Estimation

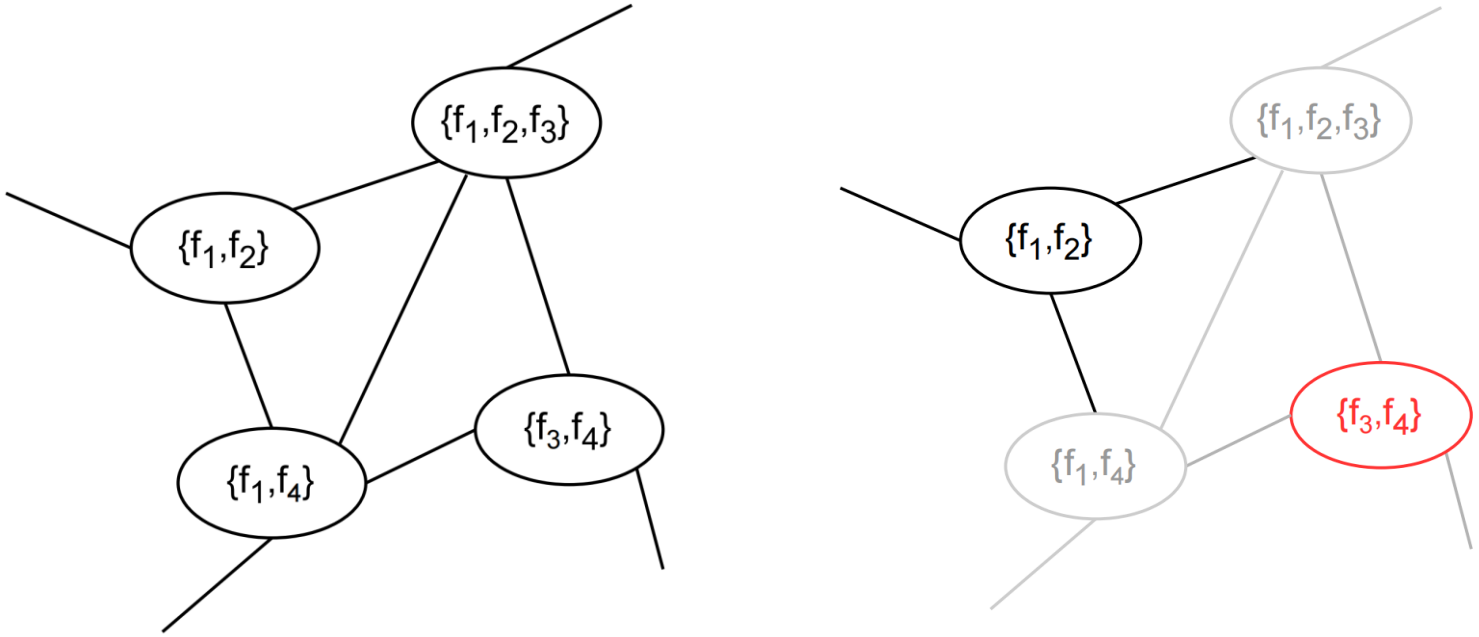
- Based on NLP-based timing prediction model
  - Embedded with basic gate features and global features
  - Trained as regression model using golden delays without MBFF clustering
  - Estimate both input and output delay





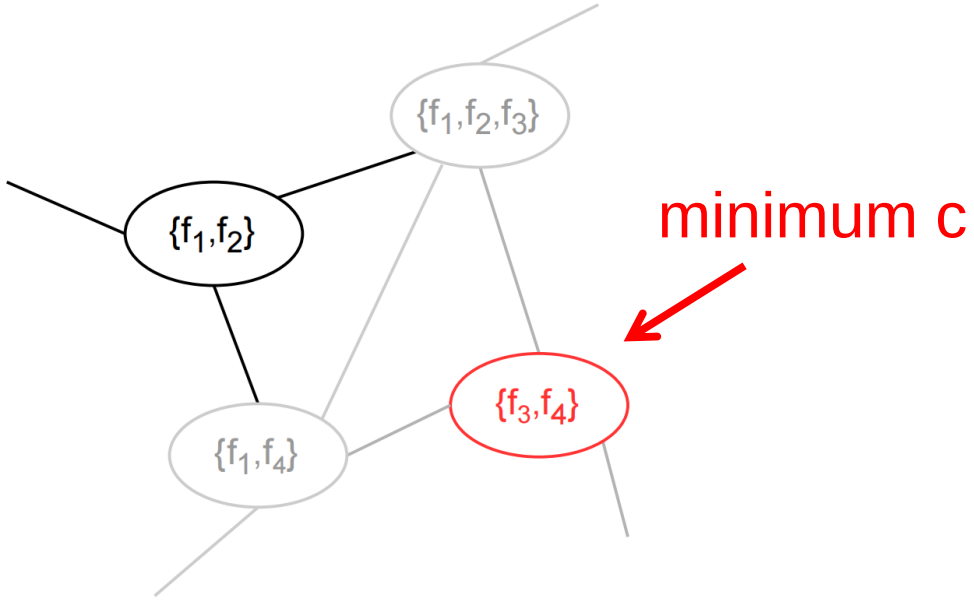
Step 3. MBFF Clustering Algorithm

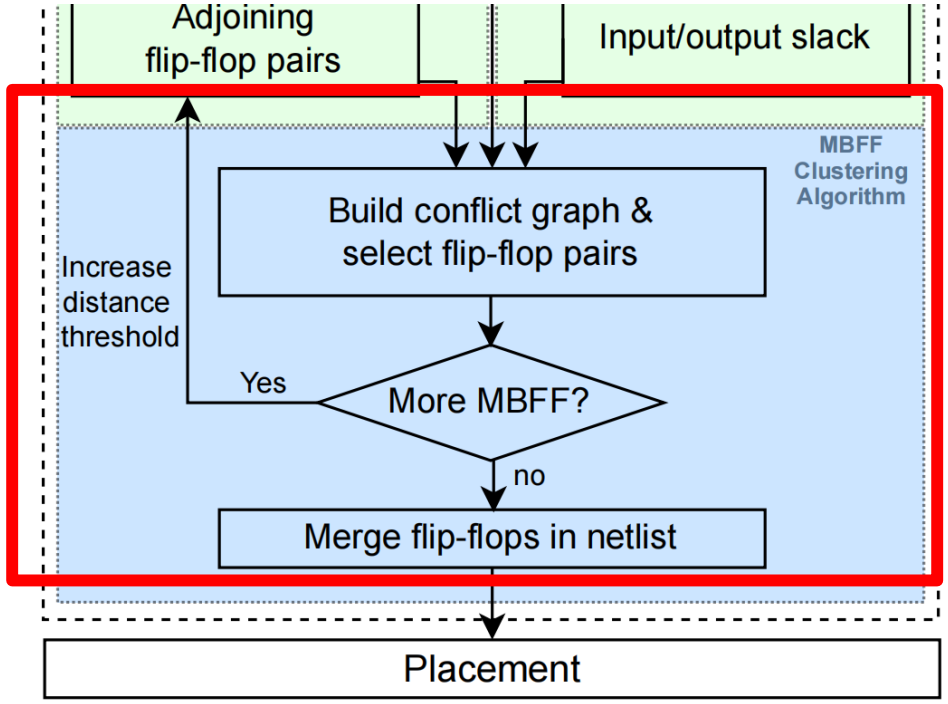
- Conflict graph
  - Each node -> one possible FF pair
  - Each edge -> share a same FF between two nodes
  - After select one node, should delete all adjoining nodes



Step 3. MBFF Clustering Algorithm

a) Build conflict graph based on all filtered FF pairs in Step 1
b) Assign weight of each node as potential power reduction amount
c) Calculate coefficient c (show in next few slides)
d) Find, select, and cluster the node with smallest coefficient c



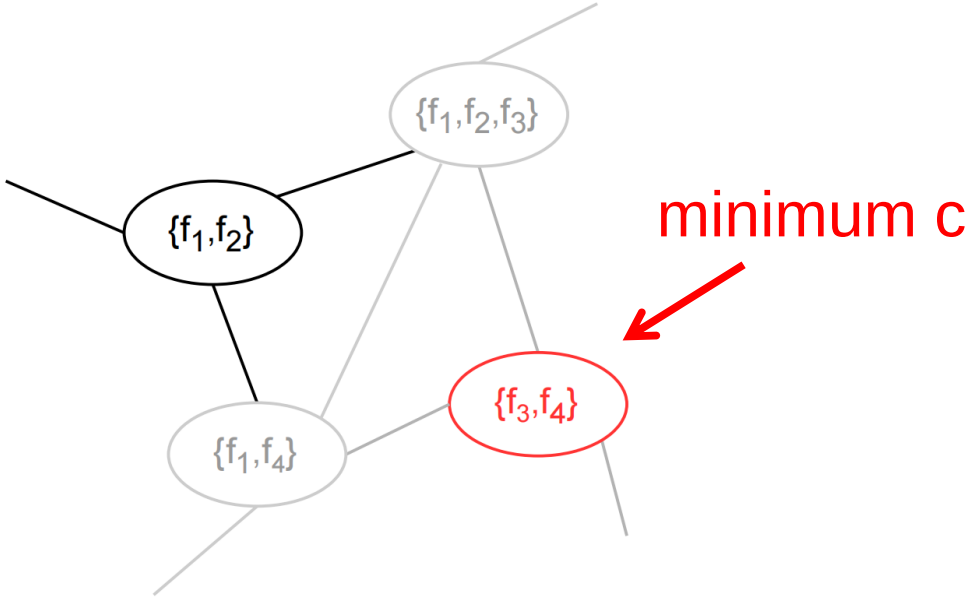


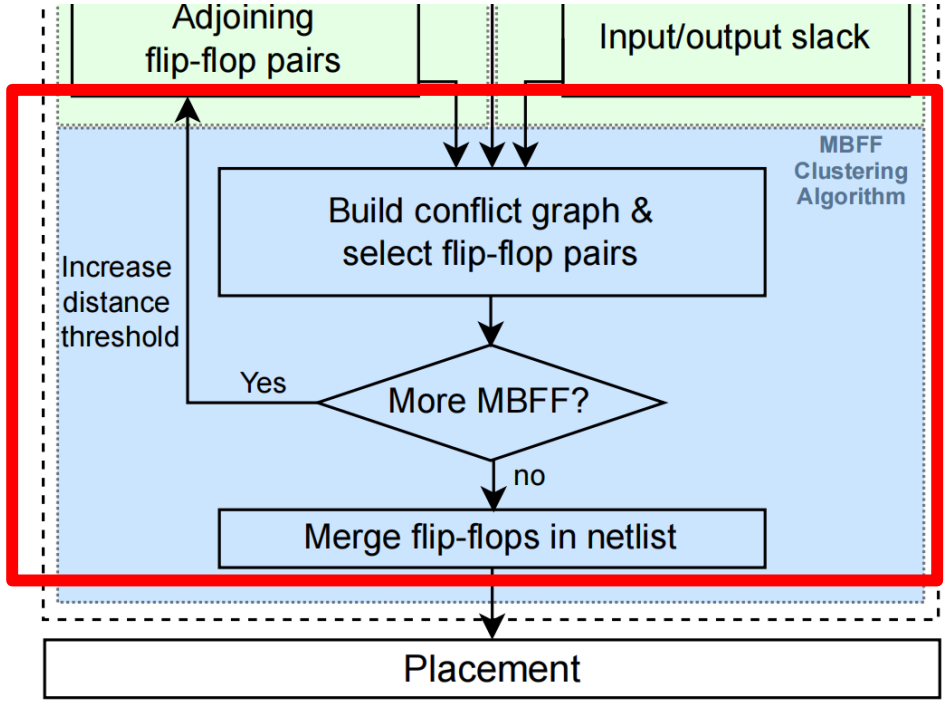
Step 3. MBFF Clustering Algorithm

e) Repeat above steps until all nodes are selected

f) Release the distance threshold to introduce more possible FF pairs into consideration

g) Iterate until no more MBFF can be further clustered





Step 3. MBFF Clustering Algorithm

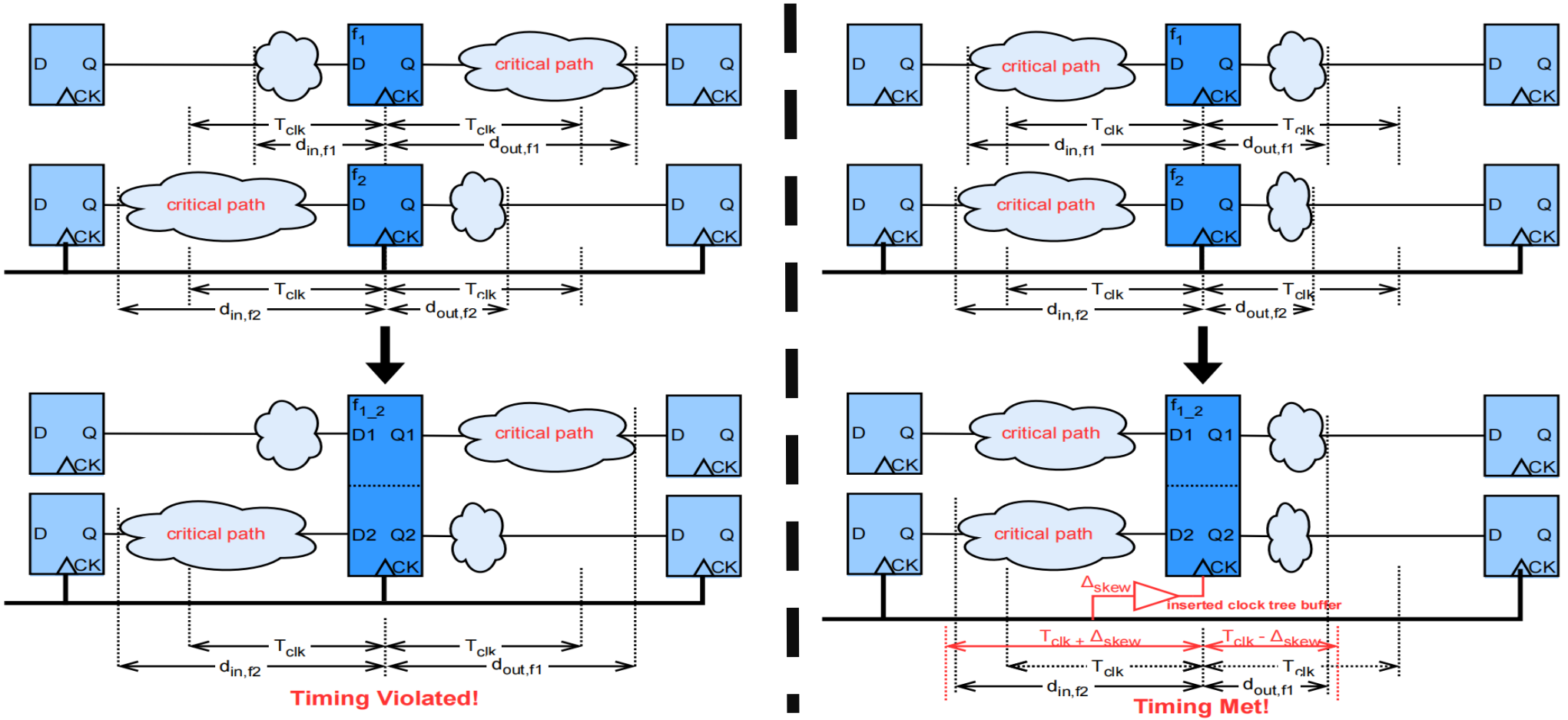
- The coefficient c is calculated by:

$$\Delta slk_{f_i} = d_{in,f_i} - d_{out,f_i}$$
$$\Delta slk_{f_j} = d_{in,f_j} - d_{out,f_j}$$
$$c_i = \frac{\sum_{adjacent} w_j}{w_i} * \left(1 + \frac{|\Delta slk_{f_i} - \Delta slk_{f_j}|}{|\Delta slk_{f_i} + \Delta slk_{f_j}|}\right)$$

Ratio of potentially wased power

timing coefficient based on useful skew optimization

Step 3. MBFF Clustering Algorithm



(a) Type I FF pair with large Δ_{slk} difference.

(b) Type II FF pair with small Δ_{slk} difference.

Smaller $1 + \frac{|\Delta slk_{f_i} - \Delta slk_{f_j}|}{|\Delta slk_{f_i} + \Delta slk_{f_j}|}$ results in better QoR

Experiment Setup

- Commercial EDA tools and flow
- 28nm technology node PDK
- Standard cell library and 2-bit MBFF library
- One OpenRISC core & six IWLS 2005 benchmark

Benchmarks	#FFs	#Cells	#Nets	Clock Period (ns)
or1200	3627	23417	23716	1
mem_ctrl	1002	5008	5124	0.15
ac97_ctrl	2161	6519	6604	0.5
wb_conmax	770	23531	24663	0.35
ethernet	10534	34025	34123	3
vga_lcd	17050	51885	51974	6
des_perf	8808	66951	67188	0.35

Experiment Results

Benchmarks		Commercial Tool without MBFF	Commercial Tool with MBFF		Pre-placement MBFF Clustering [19]		Proposed Approach	
or1200	P_{clk}	17.88	**13.74**	**23.15%**	14.10	21.14%	**13.74**	**23.15%**
	P_{total}	27.71	23.68	14.54%	23.60	14.83%	**23.26**	**16.06%**
	WNS	-0.206	-0.238	-15.53%	-0.250	-21.36%	**-0.217**	**-5.34%**
	TNS	-20.491	-17.517	14.51%	-17.723	13.51%	**-16.737**	**18.32%**
mem_ctrl	P_{clk}	32.49	28.91	11.02%	**26.03**	**19.88%**	26.60	18.13%
	P_{total}	39.44	36.17	8.29%	**33.44**	**15.21%**	33.83	14.22%
	WNS	-0.318	-0.337	-5.97%	-0.327	-2.83%	**-0.324**	**-1.89%**
	TNS	-156.437	-171.942	-9.91%	-179.379	-14.67%	**-164.090**	**-4.89%**
ac97_ctrl	P_{clk}	22.06	17.15	22.26%	17.23	21.89%	**16.56**	**24.93%**
	P_{total}	25.48	20.84	18.21%	20.93	17.86%	**20.10**	**21.11%**
	WNS	-0.281	-0.321	-14.23%	-0.333	-18.51%	**-0.275**	**2.14%**
	TNS	-16.554	-31.108	-87.92%	-23.016	-39.04%	**-9.017**	**45.53%**
wb_conmax	P_{clk}	15.30	11.38	25.62%	**9.76**	**36.21%**	11.13	27.25%
	P_{total}	37.61	33.50	10.93%	**31.15**	**17.18%**	33.65	10.53%
	WNS	-0.118	-0.112	5.08%	-0.209	-77.12%	**-0.084**	**28.81%**
	TNS	-13.802	-19.201	-39.12%	-41.450	-200.32%	**-14.097**	**-2.14%**
ethernet	P_{clk}	16.22	**11.47**	**29.28%**	12.94	20.22%	12.47	23.12%
	P_{total}	19.74	**15.03**	**23.86%**	16.56	16.11%	16.08	18.54%
	WNS	-2.608	-2.789	-6.94%	-2.943	-12.85%	**-2.380**	**8.74%**
	TNS	-273.830	-336.379	-22.84%	-352.083	-28.58%	**-260.849**	**4.74%**
vga_lcd	P_{clk}	12.52	**9.22**	**26.36%**	9.53	23.88%	9.29	25.80%
	P_{total}	15.70	13.80	12.10%	14.93	4.90%	**13.02**	**17.07%**
	WNS	-8.052	-16.796	-108.59%	-13.228	-64.28%	**-10.239**	**-27.16%**
	TNS	-367.614	-792.290	-115.52%	-610.260	-66.01%	**-456.827**	**-24.27%**
des_perf	P_{clk}	121.71	97.95	19.52%	100.73	17.24%	**89.22**	**26.69%**
	P_{total}	227.76	211.82	7.00%	208.64	8.39%	**192.33**	**15.56%**
	WNS	-0.271	-0.300	-10.70%	-0.259	4.43%	**-0.188**	**30.63%**
	TNS	-151.965	-171.134	-12.61%	-155.087	-2.05%	**-122.473**	**19.41%**
Average	P_{clk}	-	-	22.46%	-	22.92%	-	**24.15%**
	P_{total}	-	-	13.56%	-	13.50%	-	**16.16%**
	WNS	-	-	-22.41%	-	-27.50%	-	**5.13%**
	TNS	-	-	-39.06%	-	-48.16%	-	**8.10%**

Experiment Results

Benchmarks		Commercial Tool without MBFF	Commercial Tool with MBFF		Pre-placement MBFF Clustering [19]		Proposed Approach	
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	[illegible]	[illegible]	[illegible]	[illegible]	**33.44**	**15.21%**	33.83	14.22%
	[illegible]	[illegible]	[illegible]	[illegible]	-0.327	-2.83%	**-0.324**	**-1.89%**
	[illegible]	[illegible]	[illegible]	[illegible]	-179.379	-14.67%	**-164.090**	**-4.89%**
	[illegible]	[illegible]	[illegible]	[illegible]	17.23	21.89%	**16.56**	**24.93%**
	[illegible]	[illegible]	[illegible]	[illegible]	20.93	17.86%	**20.10**	**21.11%**
	[illegible]	[illegible]	[illegible]	[illegible]	-0.333	-18.51%	**-0.275**	**2.14%**
	[illegible]	[illegible]	[illegible]	[illegible]	-23.016	-39.04%	**-9.017**	**45.53%**
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	WNS	-	-	-22.41%	-	-27.50%	-	**5.13%**
	TNS	-	-	-39.06%	-	-48.16%	-	**8.10%**

One state-of-the-art pre-placement MBFF clustering algorithm based on pure logic locality.

Experiment Results

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wb_conmax	P_{clk}	15.30	11.38	25.62%	**9.76**	**36.21%**	11.13	27.25%
	P_{total}	37.61	33.50	10.93%	**31.15**	**17.18%**	33.65	10.53%
	WNS	-0.118	-0.112	5.08%	-0.209	-77.12%	**-0.084**	**28.81%**
	TNS	-13.802	-19.201	-39.12%	-41.450	-200.32%	**-14.097**	**-2.14%**
ethernet	P_{clk}	16.22	**11.47**	**29.28%**	12.94	20.22%	12.47	23.12%
	P_{total}	19.74	**15.03**	**23.86%**	16.56	16.11%	16.08	18.54%
	WNS	-2.608	-2.789	-6.94%	-2.943	-12.85%	**-2.380**	**8.74%**
	TNS	-273.830	-336.379	-22.84%	-352.083	-28.58%	**-260.849**	**4.74%**
vga_lcd	P_{clk}	12.52	**9.22**	**26.36%**	9.53	23.88%	9.29	25.80%
	P_{total}	15.70	13.80	12.10%	14.93	4.90%	**13.02**	**17.07%**
	WNS	-8.052	-16.796	-108.59%	-13.228	-64.28%	**-10.239**	**-27.16%**
	TNS	-367.614	-792.290	-115.52%	-610.260	-66.01%	**-456.827**	**-24.27%**
des_perf	P_{clk}	121.71	97.95	19.52%	100.73	17.24%	**89.22**	**26.69%**
	P_{total}	227.76	211.82	7.00%	208.64	8.39%	**192.33**	**15.56%**
	WNS	-0.271	-0.300	-10.70%	-0.259	4.43%	**-0.188**	**30.63%**
	TNS	-151.965	-171.134	-12.61%	-155.087	-2.05%	**-122.473**	**19.41%**
Average	P_{clk}	-	-	22.46%	-	22.92%	-	**24.15%**
	P_{total}	-	-	13.56%	-	13.50%	-	**16.16%**
	WNS	-	-	-22.41%	-	-27.50%	-	**5.13%**
	TNS	-	-	-39.06%	-	-48.16%	-	**8.10%**

Experiment Results

Benchmarks		Commercial Tool without MBFF	Commercial Tool with MBFF		Pre-placement MBFF Clustering [19]		Proposed Approach	
or1200	P_{clk}	17.88	**13.74**	**23.15%**	14.10	21.14%	**13.74**	**23.15%**
	P_{total}	27.71	23.68	14.54%	23.60	14.83%	**23.26**	**16.06%**
	WNS	-0.206	-0.238	-15.53%	-0.250	-21.36%	**-0.217**	**-5.34%**
	TNS	-20.491	-17.517	14.51%	-17.723	13.51%	**-16.737**	**18.32%**
mem_ctrl	P_{clk}	32.49	28.91	11.02%	**26.03**	**19.88%**	26.60	18.13%
	P_{total}	39.44	36.17	8.29%	**33.44**	**15.21%**	33.83	14.22%
	WNS	-0.318	-0.337	-5.97%	-0.327	-2.83%	**-0.324**	**-1.89%**
	TNS	-156.437	-171.942	-9.91%	-179.379	-14.67%	**-164.090**	**-4.89%**
ac97_ctrl	P_{clk}	22.06	17.15	22.26%	17.23	21.89%	**16.56**	**24.93%**
	P_{total}	25.48	20.84	18.21%	20.93	17.86%	**20.10**	**21.11%**
	WNS	-0.281	-0.321	-14.23%	-0.333	-18.51%	**-0.275**	**2.14%**
	TNS	-16.554	-31.108	-87.92%	-23.016	-39.04%	**-9.017**	**45.53%**
wb_conmax	P_{clk}	15.30	11.38	25.62%	**9.76**	**36.21%**	11.13	27.25%
	P_{total}	37.61	33.50	10.93%	**31.15**	**17.18%**	33.65	10.53%
	WNS	-0.118	-0.112	5.08%	-0.209	-77.12%	**-0.084**	**28.81%**
	TNS	-13.802	-19.201	-39.12%	-41.450	-200.32%	**-14.097**	**-2.14%**
ethernet	P_{clk}	16.22	**11.47**	**29.28%**	12.94	20.22%	12.47	23.12%
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	TNS	-273.830	-336.379	-22.84%	-352.083	-28.58%	**-260.849**	**4.74%**
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	WNS	-0.271	-0.300	-10.70%	-0.259	4.43%	**-0.188**	**30.63%**
	TNS	-151.965	-171.134	-12.61%	-155.087	-2.05%	**-122.473**	**19.41%**
Average	P_{clk}	-	-	22.46%	-	22.92%	-	**24.15%**
	P_{total}	-	-	13.56%	-	13.50%	-	**16.16%**
	WNS	-	-	-22.41%	-	-27.30%	-	**5.15%**
	TNS	-	-	-39.06%	-	-48.16%	-	**8.10%**

Experiment Results

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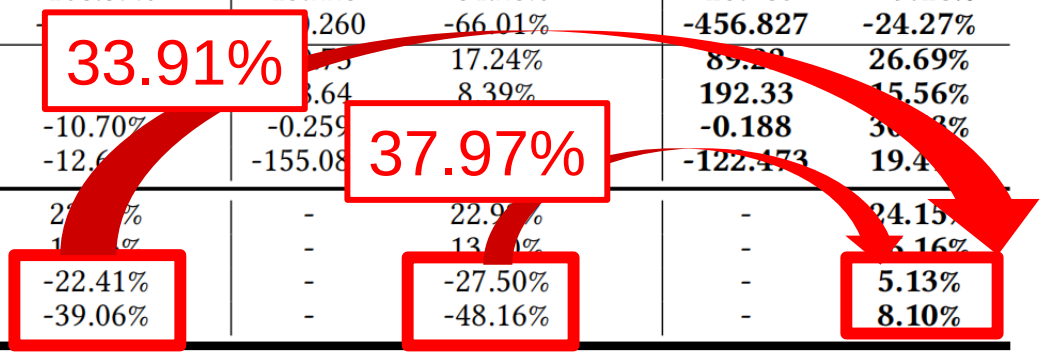
	WNS	-0.271	-0.300	-10.70%	-0.259		**-0.188**	**3**
	TNS	-151.965	-171.134	-12.	-155.08		**-122.**	**19.**
Average	P_{clk}	-	-	2 %	-	22.9 %	-	**24.15**
	P_{total}	-	-	1 %	-	13. %	-	**. 16%**
	WNS	-	-	-22.41%	-	-27.50%	-	**5.13%**
	TNS	-	-	-39.06%	-	-48.16%	-	**8.10%**



Conclusions

- An early stage MBFF clustering algorithm with both physical and timing awareness.
- Promise the final timing condition while reducing power through MBFF clustering and useful skew optimization.
- Without many iterations through placment and route, the proposed flow only needs to execute the flow for one time.
- The algorithm is implemented on commercial EDA tools and flow, and is capable to work with other power reduction techniques easily.

Thank you!

Time for Q&A