CACTI-CNFET: an Analytical Tool for Timing, Power, and Area of SRAMs with Carbon Nanotube Field Effect Transistors*

Shinobu Miwa† Eiichiro Sekikawa† Tongxin Yang†

Ryota Shioya‡ Hayato Yamaki† Hiroki Honda†

†The University of Electro-Communications

‡The University of Tokyo

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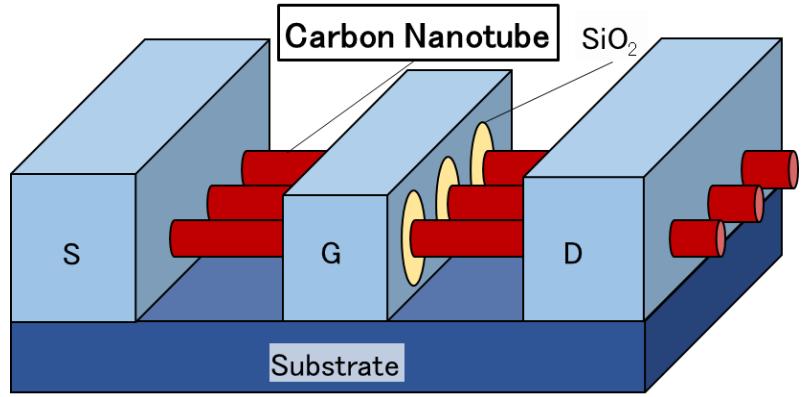
CNFET (Carbon Nanotube Field Effect Transistor)

Transistor composed of nano-meter order carbon nanotubes (CNTs)

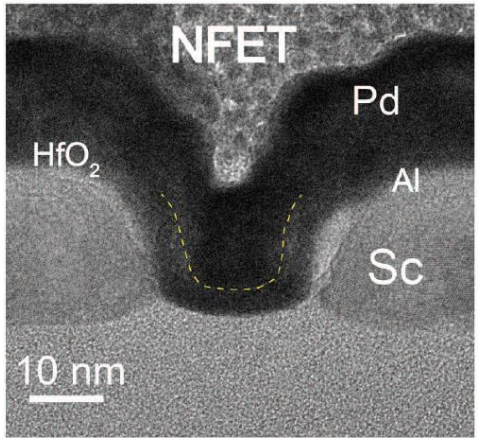
- Use CNTs, which have an electronic characteristic superior to silicon, as channel materials
- Operate at a high speed with a small supply voltage (e.g., 0.375V)

Greater performance than silicon transistors [1]

- Gate delay: 1/3.9
- Energy efficiency: 9.4x



CNFET

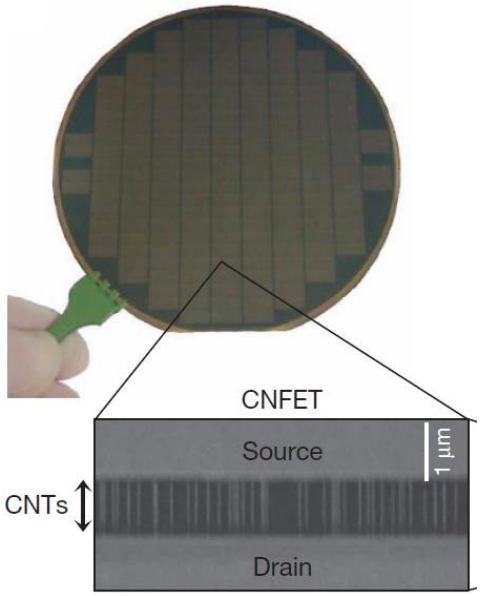


Cross section of CNFETs [1]

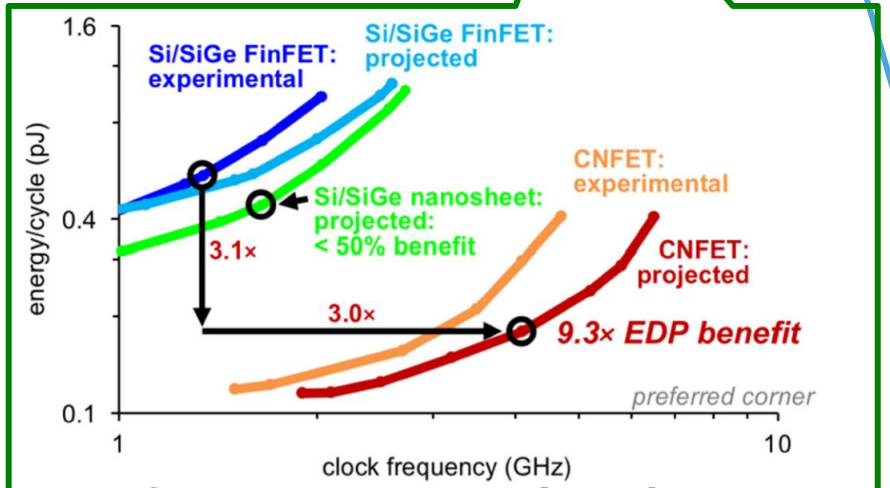
[1] C. Qiu et al., Scaling Carbon Nanotube Complementary Transistors to 5-nm Gate Lengths, Science (2017)

CNFET Processors

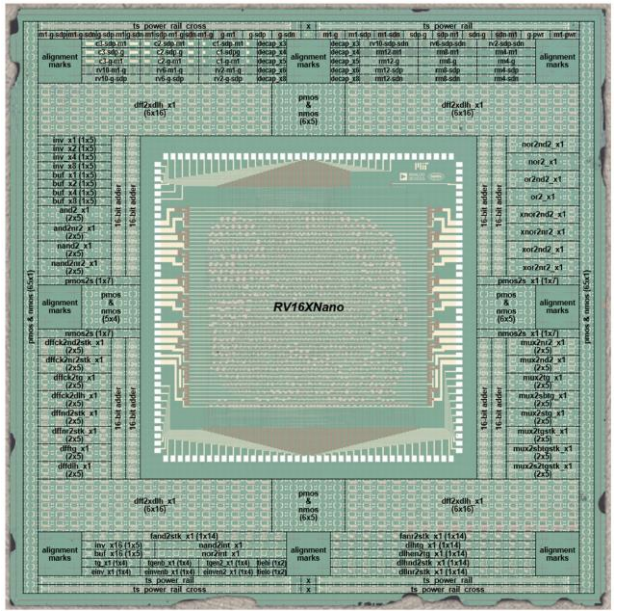
2010 — 2015 — 2020 — 2025



The first CNFET processor [2]
(data: 1b, frequency: 1KHz)



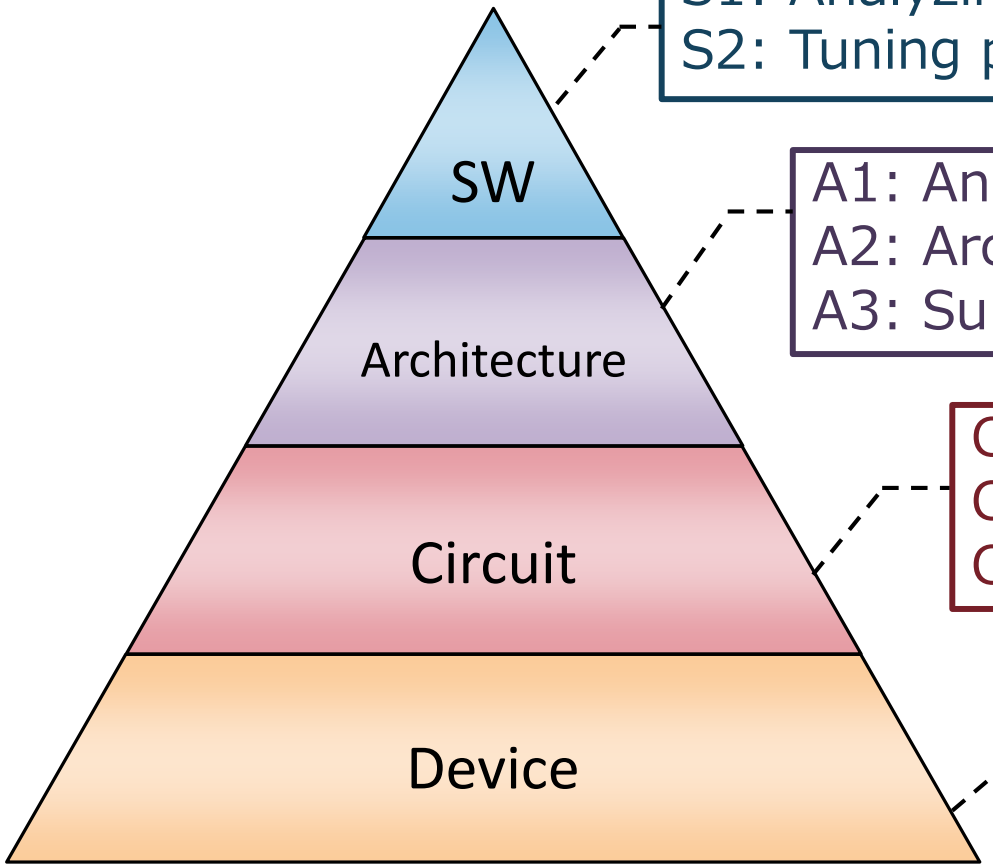
Performance comparison between 5nm FinFET and 5nm CNFET for an OpenSPARC T2 processor [3]



The first CNFET RISC-V processor [4]
(data: 16b, frequency: 10KHz)

[2] M. Shulaker et al., Carbon Nanotube Computer, Nature (2013)
[3] G. Hills et al., Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI, IEEE TNano (2018)
[4] G. Hills et al., Modern Microprocessor Built from Complementary Carbon Nanotube Transistors, Nature (2019)

Challenges towards Practical Use of CNFET Processors



S1: Analyzing the impact of CNFET on software performance
S2: Tuning performance of applications running on CNFET processors

A1: Analyzing the impact of CNFET on architecture performance
A2: Architectural optimization for CNFET
A3: Support of architectural design tools ⬅ **This work!**

C1: Analyzing the impact of CNFET on circuit performance
C2: Performance optimization for CNFET circuits
C3: Support of circuit design tools

D1: Establishment of manufacturing technologies
D2: Reduction of manufacturing cost

Lack of CNFET Processor Design Tools

Modern processors are designed with the help of various architecture-level design tools

- Performance simulator (e.g., Gem5, Sniper, GPGPU-Sim)
- Power and area simulator (e.g., McPAT, GPUWattch)

Current development of CNFET processors is executed fully at the circuit level (i.e., with some EDA tools and CNFET cell libraries)

This gap hinders us in exploring various processor architectures that utilize the great potential of CNFET!

Research Objectives and Contributions

Our goal is to fill the gap between processes to design traditional CMOS and CNFET processors

As a first step, we developed **CACTI-CNFET**

- First architecture-level analytical tool for SRAMs manufactured with the state-of-the-art (5nm) CNFET technology
- Help us make a quick decision on the architecture of CNFET SRAMs within a targeted processor
- Built at the top of CACTI so it can be used and extended easily

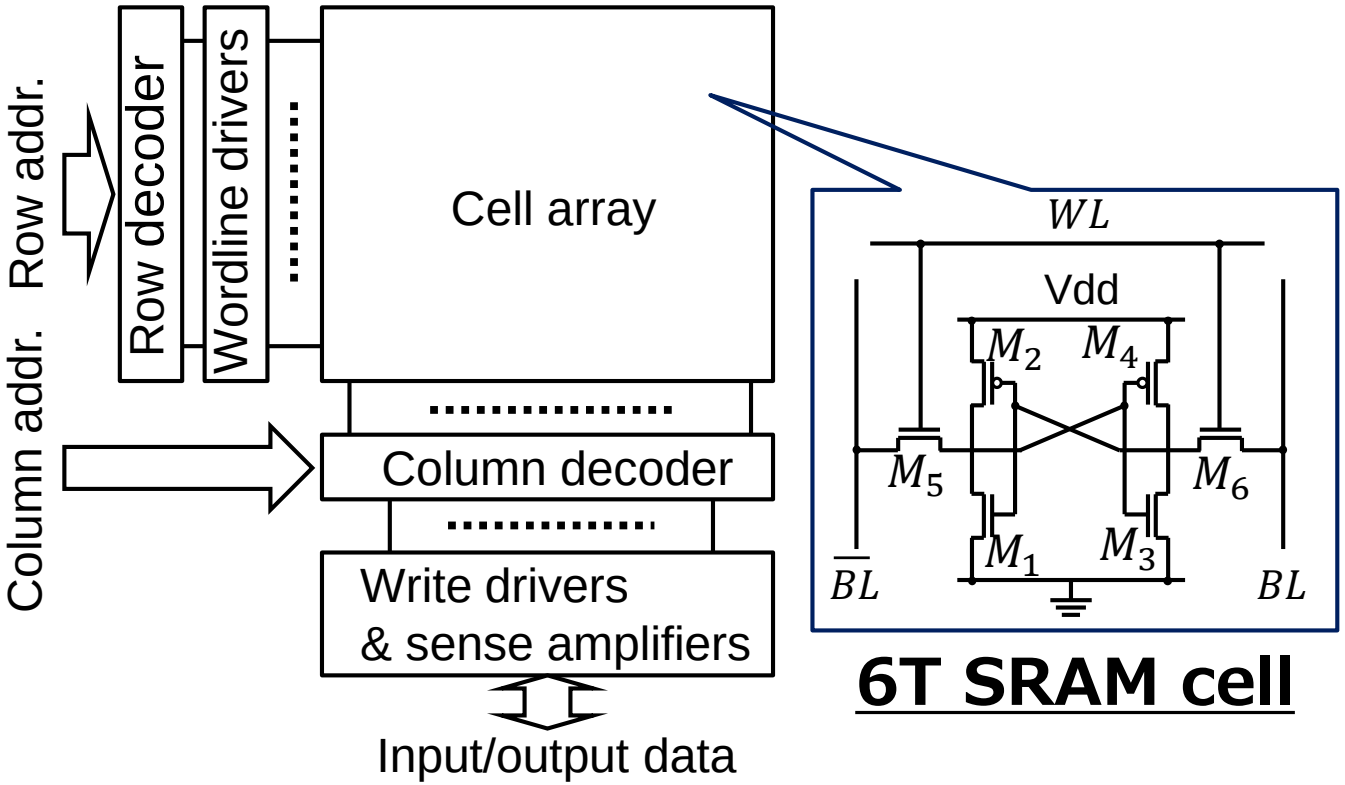
CACTI-CNFET is available on our GitHub repository

SRAM

Used as various on-chip memories in processors
(e.g., caches, register files, etc.)

Composed of several submodules

- Cell array
- Row/column decoders
- Wordline/write drivers
- Sense amplifiers



SRAM architecture

6T SRAM cell

CACTI

Analytical tool for various memories (e.g., SRAMs, CAMs, and DRAMs)

- Compute the performance, power, and area of a target memory from the given tech node and architectural description (e.g., capacity and port count), w/ some models
- Produce slightly incorrect outputs (within a 6% error [5]) but enable a quick analysis of the target memory

Used internally in some architecture-level processor design tools [6,7]

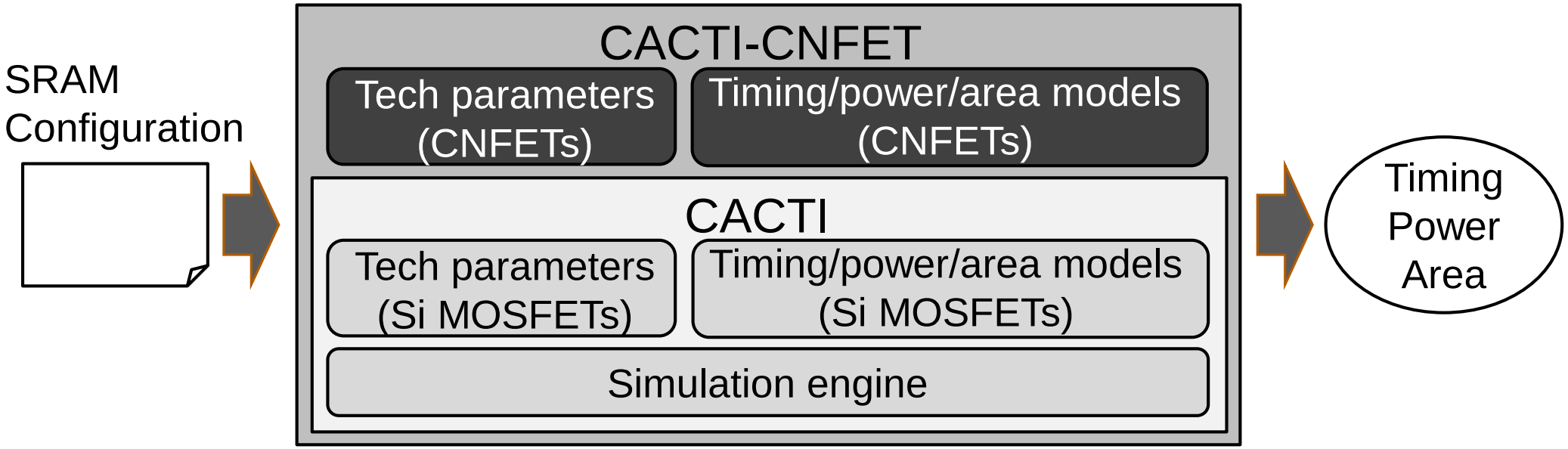
Support only conventional CMOS technology nodes

[5] S. J. E. Wilton and N. P. Jouppi, CACTI: an Enhanced Cache Access and Cycle Time Model, IEEE JSSCC, Vol. 31, No. 5 (1996)
[6] J. Leng et al., GPUWattch: Enabling Energy Optimizations in GPGPUs, ISCA (2013)
[7] S. Li et al., McPAT: An Integrated Power, Area, and Timing Modeling Framework for Multicore and Manycore Architectures, MICRO (2009)

Overview of CACTI-CNFET

Maintain CACTI's user interface and reuse the internal components as much as possible

The tech parameters and timing/power/area models related to CNFETs are newly added or modified



CACTI-CNFET

Supported CNFET Technology Node

5nm CNFET technology

- Used in the previous work [3]
- Projected from some device-level experimental data

Some of key parameters are used in CACTI-CNFET as is

Key parameters of 5nm CNFET

Parameters	Values
Width W (nm)	21
L_g, L_c, L_{ext} (nm)	10, 15, 8.5
Gate height H_g (nm)	20
Gate oxide T_{ox} (nm)	1.9
Gate oxide K_{ox}	10.6
Space oxide K_{spacer}	4.0
CNT diameter d (nm)	1.8
Inter-CNT pitch s (nm)	2
Apparent mobility (cm^2/Vs)	427.8
Supply voltage V_{dd} (V)	0.375

[3] G. Hills et al., Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI, IEEE TNano (2018)

Derivation of Undisclosed Parameters

Some parameters needed for CACTI-CNFET are not shown in the previous work

These parameters are derived from SPICE simulations and some theoretical formulas

Please read our paper if you would like to know the details of the derivation methods

Derived parameters of 5nm CNFET

Parameters	Values
On current I_{on} (A/μm)	1.72×10^{-3}
Off current I_{off} (A/μm)	1.04×10^{-7}
Gate leakage current $I_{gateleak}$ (A/μm)	9.09×10^{-11}
Threshold voltage V_{th} (V)	0.262
Drain saturation voltage V_{dsat} (V)	0.093
Voltage difference of sense amplifier V_{sense} (V)	0.154
Parallel plate capacitance C_{g_ideal} (aF/μm)	176.52
Fringe capacitance C_{fringe} (aF/μm)	148.26
Junction area capacitance C_{area} (aF/μm)	0.00
Junction sidewall capacitance $C_{sidewall}$ (aF/μm)	38.01

Model Correction

Some models used in the original CACTI do not match CNFET SRAMs

Make the following modifications to improve the estimation accuracy of CACTI-CNFET

- Change the channel width ratio of PMOS and NMOS from 2:1 to 1:1
- Remove the effect of shared contact from the formula that computes bitline capacitance
- Implement the leakage power and energy consumption models for write drivers

Experimental Setup

Compare CACTI-CNFET with SPICE simulation and OpenRAM [8]

Perform the evaluation for various SRAM subarrays with different numbers of rows and columns

Evaluation metrics

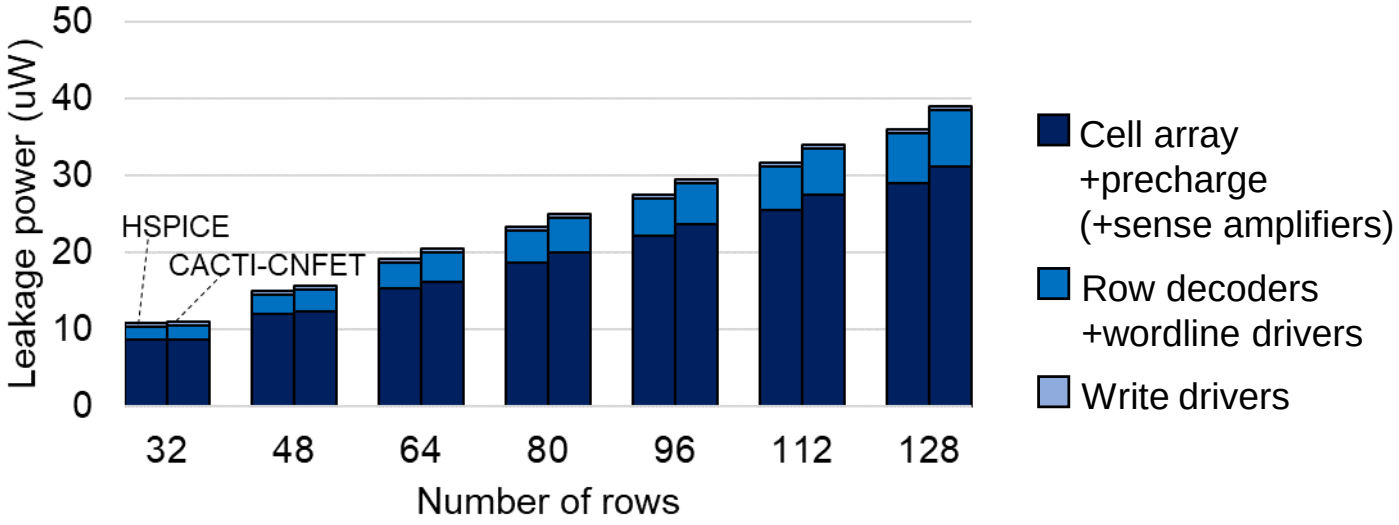
- Accuracy (delay, power, energy, and area)
- Speed

[8] M. R. Guthaus et al., OpenRAM: An Open-source Memory Compiler, ICCAD (2016)

Leakage Power Estimation Results

Show an error of 7.40% on average

Prediction for each submodule shows sufficient accuracy



Breakdown of leakage power (128 columns)

Columns

Rows	32	48	64	80	96	112	128
32	3.97	5.11	6.24	7.38	8.52	9.66	10.80
48	5.60	7.16	8.72	10.28	11.84	13.40	14.96
64	7.26	9.24	11.22	13.20	15.18	17.17	19.15
80	8.91	11.31	13.71	16.11	18.52	20.92	23.33
96	10.55	13.38	16.20	19.02	21.85	24.68	27.51
112	12.21	15.45	18.70	21.95	25.20	28.45	31.71
128	13.88	17.55	21.22	24.90	28.58	32.26	35.94

Rows	32	48	64	80	96	112	128
32	4.282	5.415	6.547	7.68	8.813	9.946	11.08
48	6.08	7.684	9.287	10.89	12.49	14.1	15.7
64	8.038	10.11	12.19	14.26	16.34	18.41	20.48
80	9.764	12.31	14.85	17.4	19.94	22.49	25.03
96	11.44	14.46	17.47	20.49	23.5	26.52	29.54
112	13.12	16.61	20.09	23.58	27.06	30.55	34.04
128	15.28	19.24	23.2	27.15	31.11	35.07	39.02

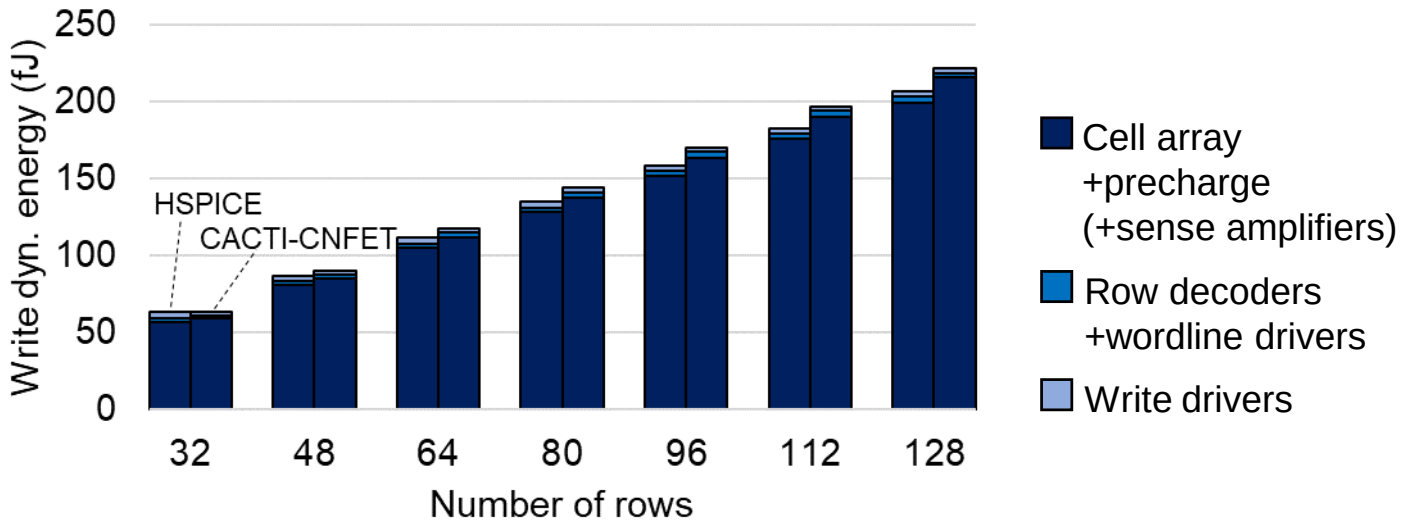
Rows	32	48	64	80	96	112	128
32	7.94	6.06	4.86	4.04	3.43	2.96	2.58
48	8.57	7.34	6.54	5.97	5.54	5.20	4.92
64	10.76	9.49	8.65	8.06	7.60	7.23	6.94
80	9.62	8.85	8.36	7.99	7.71	7.47	7.28
96	8.41	8.08	7.86	7.70	7.56	7.45	7.34
112	7.50	7.48	7.45	7.43	7.40	7.38	7.34
128	10.14	9.64	9.30	9.05	8.86	8.70	8.57

Validation results (top: HSPICE (μW), middle: CACTI-CNFET (μW), bottom: errors (%))

Write Dynamic Energy Estimation Results

Show an error of 7.08% on average

Prediction for each submodule shows sufficient accuracy



Breakdown of leakage power (128 columns)

Columns

Rows

	32	48	64	80	96	112	128
32	16.55	24.05	31.45	39.42	47.01	55.23	63.15
48	22.25	32.84	43.18	54.08	64.60	75.81	86.75
64	29.09	42.55	55.88	69.79	83.34	97.41	111.50
80	34.71	51.22	67.32	84.28	100.81	117.95	134.80
96	40.84	60.20	79.34	99.12	118.74	138.85	158.83
112	47.02	69.43	91.35	114.24	136.63	159.71	182.73
128	53.75	79.29	104.03	129.79	155.18	181.14	207.12

Rows

	32	48	64	80	96	112	128
32	17.13	24.88	32.62	40.37	48.11	55.86	63.6
48	23.9	34.9	45.91	56.91	67.92	78.92	89.93
64	31.89	46.15	60.42	74.68	88.95	103.2	117.5
80	38.74	56.26	73.79	91.31	108.8	126.4	143.9
96	45.55	66.34	87.12	107.9	128.7	149.5	170.3
112	52.37	76.42	100.5	124.5	148.6	172.6	196.6
128	57.5	84.8	112.1	139.4	166.7	194	221.3

Rows

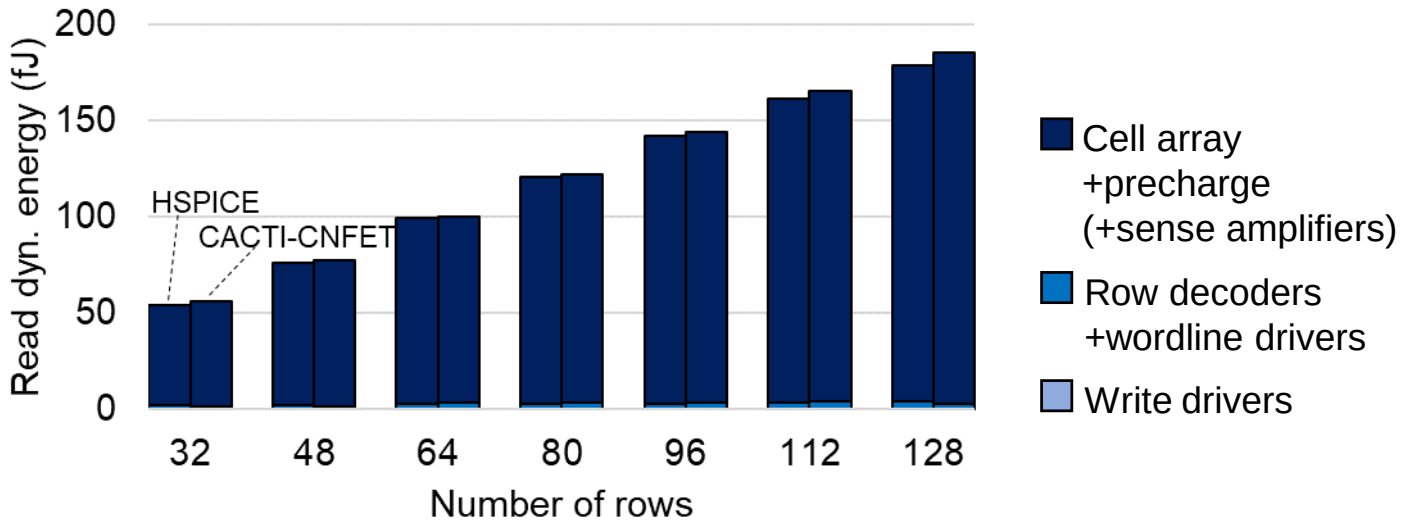
	32	48	64	80	96	112	128
32	3.54	3.43	3.73	2.41	2.34	1.14	0.71
48	7.40	6.26	6.31	5.24	5.13	4.11	3.66
64	9.63	8.48	8.13	7.02	6.73	5.96	5.36
80	11.61	9.85	9.61	8.34	7.96	7.13	6.74
96	11.55	10.19	9.82	8.87	8.39	7.65	7.20
112	11.38	10.06	9.97	8.99	8.73	8.07	7.61
128	6.97	6.95	7.77	7.42	7.43	7.11	6.86

Validation results (top: HSPICE (fJ), middle: CACTI-CNFET (fJ), bottom: errors (%))

Read Dynamic Energy Estimation Results

Show an error of 2.36% on average

Prediction for each submodule shows sufficient accuracy



Breakdown of leakage power (128 columns)

Columns

Rows

	32	48	64	80	96	112	128
32	14.95	21.33	28.10	34.54	41.18	47.78	54.24
48	20.39	29.47	39.14	48.41	57.83	67.02	76.41
64	26.91	38.70	51.22	63.34	75.19	87.36	99.88
80	32.14	46.57	61.89	76.69	91.52	106.14	121.06
96	37.70	54.69	72.19	90.20	107.69	124.70	142.14
112	42.93	62.23	82.19	102.63	121.93	142.33	161.50
128	48.17	69.51	92.40	114.23	136.17	157.34	179.10

Rows

	32	48	64	80	96	112	128
32	15.24	22.04	28.84	35.64	42.44	49.24	56.03
48	20.84	30.32	39.79	49.27	58.75	68.22	77.7
64	27.67	39.82	51.98	64.13	76.28	88.44	100.6
80	33.35	48.18	63.01	77.84	92.68	107.5	122.3
96	39	56.51	74.02	91.53	109	126.5	144.1
112	44.65	64.84	85.03	105.2	125.4	145.6	165.8
128	48.62	71.48	94.35	117.2	140.1	162.9	185.8

Rows

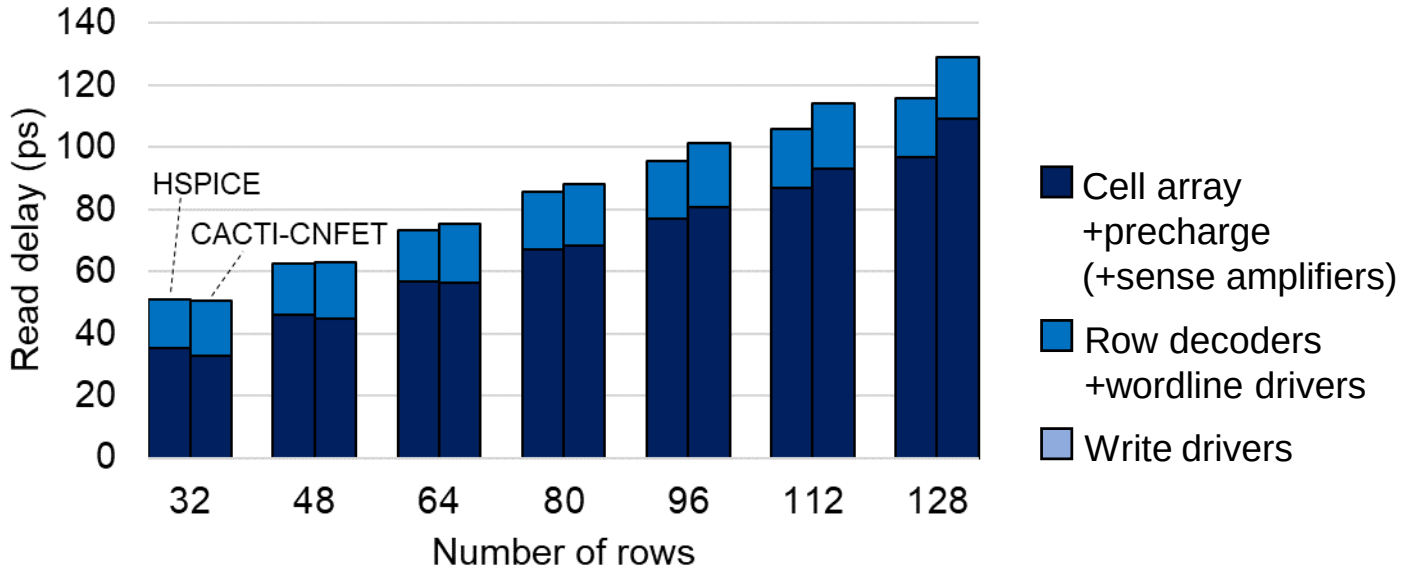
	32	48	64	80	96	112	128
32	1.92	3.32	2.64	3.18	3.05	3.05	3.32
48	2.18	2.87	1.67	1.78	1.58	1.80	1.69
64	2.81	2.90	1.48	1.25	1.45	1.23	0.71
80	3.78	3.45	1.81	1.50	1.27	1.29	1.06
96	3.45	3.33	2.54	1.47	1.25	1.49	1.35
112	4.01	4.20	3.46	2.52	2.85	2.29	2.65
128	0.92	2.84	2.11	2.61	2.87	3.56	3.75

Validation results (top: HSPICE (fJ), middle: CACTI-CNFET (fJ), bottom: errors (%))

Read Delay Estimation Results

Show an error of 8.33% on average

Prediction for each submodule shows sufficient accuracy



Breakdown of leakage power (128 columns)

Columns

Rows	32	48	64	80	96	112	128
32	41.02	41.99	43.21	44.73	46.53	48.63	51.04
48	52.28	53.26	54.53	56.06	57.84	59.96	62.34
64	63.27	64.25	65.58	67.06	68.85	70.97	73.40
80	75.34	76.35	77.63	79.16	80.95	83.04	85.45
96	85.56	86.52	87.77	89.33	91.16	93.27	95.69
112	95.54	96.53	97.79	99.35	101.19	103.33	105.73
128	105.45	106.48	107.70	109.25	111.18	113.33	115.70

Rows	32	48	64	80	96	112	128
32	44.59	45.24	46	46.89	47.93	49.1	50.42
48	57.12	57.77	58.53	59.42	60.46	61.63	62.96
64	69.66	70.31	71.07	71.96	73	74.18	75.5
80	82.33	82.97	83.74	84.63	85.67	86.85	88.17
96	95.26	95.9	96.67	97.57	98.6	99.78	101.1
112	108.4	109.1	109.8	110.7	111.8	113	114.3
128	123	123.7	124.4	125.3	126.4	127.5	128.9

Rows	32	48	64	80	96	112	128
32	8.72	7.74	6.45	4.84	2.99	0.96	1.20
48	9.27	8.46	7.33	6.00	4.52	2.79	0.99
64	10.10	9.43	8.37	7.31	6.02	4.51	2.87
80	9.27	8.67	7.87	6.92	5.83	4.58	3.18
96	11.33	10.85	10.14	9.21	8.16	6.98	5.66
112	13.49	12.99	12.32	11.46	10.46	9.31	8.08
128	16.66	16.14	15.54	14.72	13.66	12.55	11.38

Validation results (top: HSPICE (ps), middle: CACTI-CNFET (ps), bottom: errors (%))

Area Estimation Results

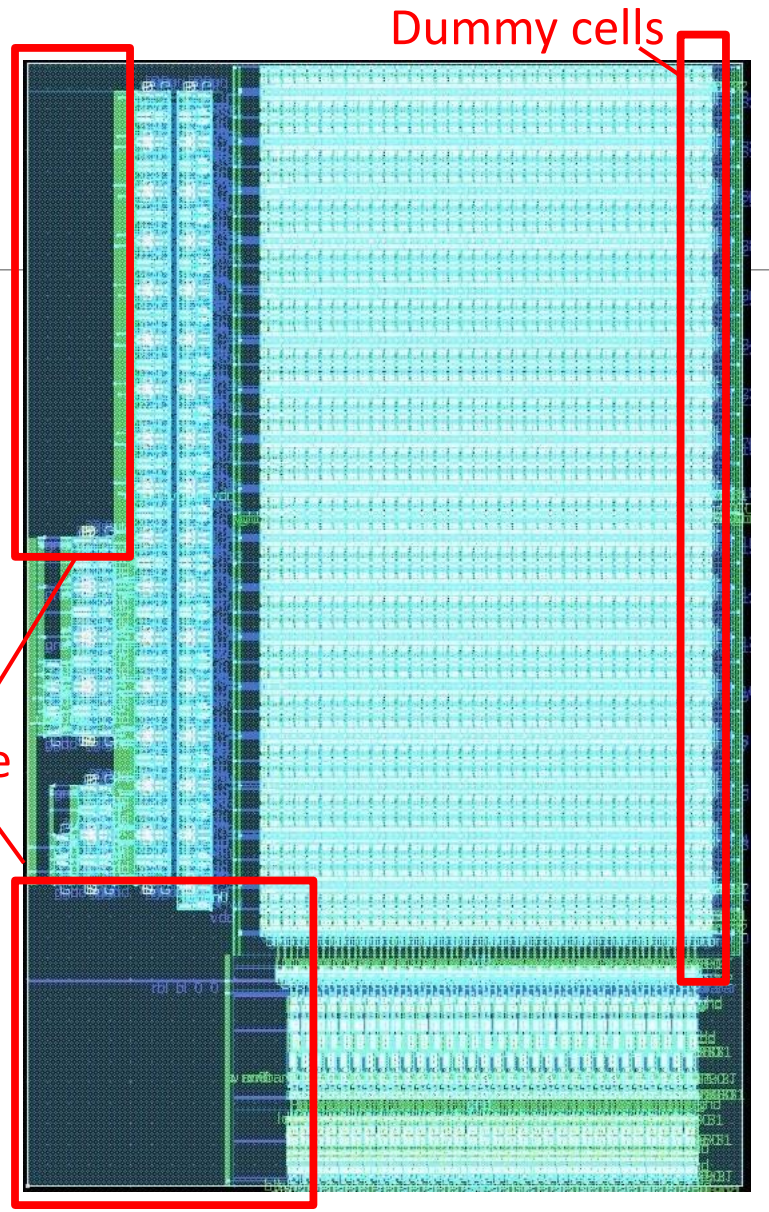
Underestimates the subarray area by 10.25-21.70% comparing OpenRAM's layouts

- The subarrays generated by OpenRAM have some extra circuits (e.g., dummy cells)
- The generated subarrays include a significant fraction of the dead space

The accuracy of CACTI-CNFET will be improved if these areas are modeled

Area of SRAMs

	OpenRAM (μm^2)	CACTI-CNFET (μm^2)	Error (%)
32x32	116.95	91.57	21.70
64x64	314.47	282.25	10.25



Layout of 32x32 CNFET SRAM (generated by OpenRAM)

Speed

Extremely ($3.2 \times 10^5 \sim 1.8 \times 10^7$ times) faster than SPICE simulation

More useful for analysis of larger memory

System configuration

Name	Remarks
CPU	AMD Ryzen 9 7950X3D (16C32T, 4.2GHz, 128MB LLC)
Memory	64GB DDR5-4800
HSPICE	U-2023.03-SP1
GCC	8.5.0

Columns

Rows	32	48	64	80	96	112	128
32	46.00	60.81	84.64	93.98	111.48	132.41	147.32
48	35.60	54.08	83.23	102.66	119.39	131.87	147.92
64	74.89	105.57	129.23	155.92	174.03	204.34	221.53
80	64.86	94.41	127.42	161.15	187.10	213.83	233.64
96	75.72	113.19	147.98	188.21	218.57	240.78	277.64
112	85.30	131.84	170.36	210.24	253.63	286.62	316.54
128	191.40	188.80	243.87	289.79	334.18	374.16	409.73

Rows	32	48	64	80	96	112	128
32	143.77	22.41	32.42	126.60	21.46	31.71	126.84
48	20.98	31.95	126.60	20.74	31.71	126.60	20.98
64	34.57	126.84	20.98	31.23	126.60	21.22	31.71
80	126.60	21.22	31.23	126.36	20.98	31.47	126.60
96	145.20	22.89	32.90	128.03	22.41	32.66	128.03
112	21.22	33.38	130.89	21.22	31.95	132.08	21.22
128	31.71	127.55	21.46	31.71	129.22	21.22	31.47

Rows	32	48	64	80	96	112	128
32	3.2E+05	2.7E+06	2.6E+06	7.4E+05	5.2E+06	4.2E+06	1.2E+06
48	1.7E+06	1.7E+06	6.6E+05	4.9E+06	3.8E+06	1.0E+06	7.1E+06
64	2.2E+06	8.3E+05	6.2E+06	5.0E+06	1.4E+06	9.6E+06	7.0E+06
80	5.1E+05	4.4E+06	4.1E+06	1.3E+06	8.9E+06	6.8E+06	1.8E+06
96	5.2E+05	4.9E+06	4.5E+06	1.5E+06	9.8E+06	7.4E+06	2.2E+06
112	4.0E+06	3.9E+06	1.3E+06	9.9E+06	7.9E+06	2.2E+06	1.5E+07
128	6.0E+06	1.5E+06	1.1E+07	9.1E+06	2.6E+06	1.8E+07	1.3E+07

Elapsed time for read delay analysis (top: HSPICE (s), middle: CACTI-CNFET (μs), bottom: speedup)

Related Work

CNFET circuit analysis

- Reveal the impact of 5nm and 7nm CNFETs on an OpenSPARC T2 processor [3]
- Evaluate the impact of 7nm CNFET for various benchmark circuits [9]
- Analyze the 6T SRAM cell optimized for 5nm CNFET [10]

No architecture-level analytical tool is used

CACTI extensions

- Support non-uniform cache architecture [11]
- Add the functionality to analyze I/O and PHY [12]
- Implement the 3D stacked DRAM model [13]

No study extends CACTI to support CNFET

[3] G. Hills et al., IEEE TNano (2018)
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Conclusions and Future Work

Conclusions

- Developed CACTI-CNFET, the first architecture-level analytical tool for CNFET SRAMs
- Showed that CACTI-CNFET can estimate the timing, power, and area of CNFET SRAMs with significant accuracy

Future work

- Validate CACTI-CNFET for the CNFET SRAM modules except for subarrays (e.g., H-tree, predecoder, etc.)
- Extend to the other SRAMs (e.g., single-ended SRAMs, 4T, 8T, and 10T SRAMs, etc.)
- Develop a complete set of architecture-level design tools for CNFET processors

Thank you!