Via Fabrication with Multi-Row Guiding Templates Using Lamellar DSA

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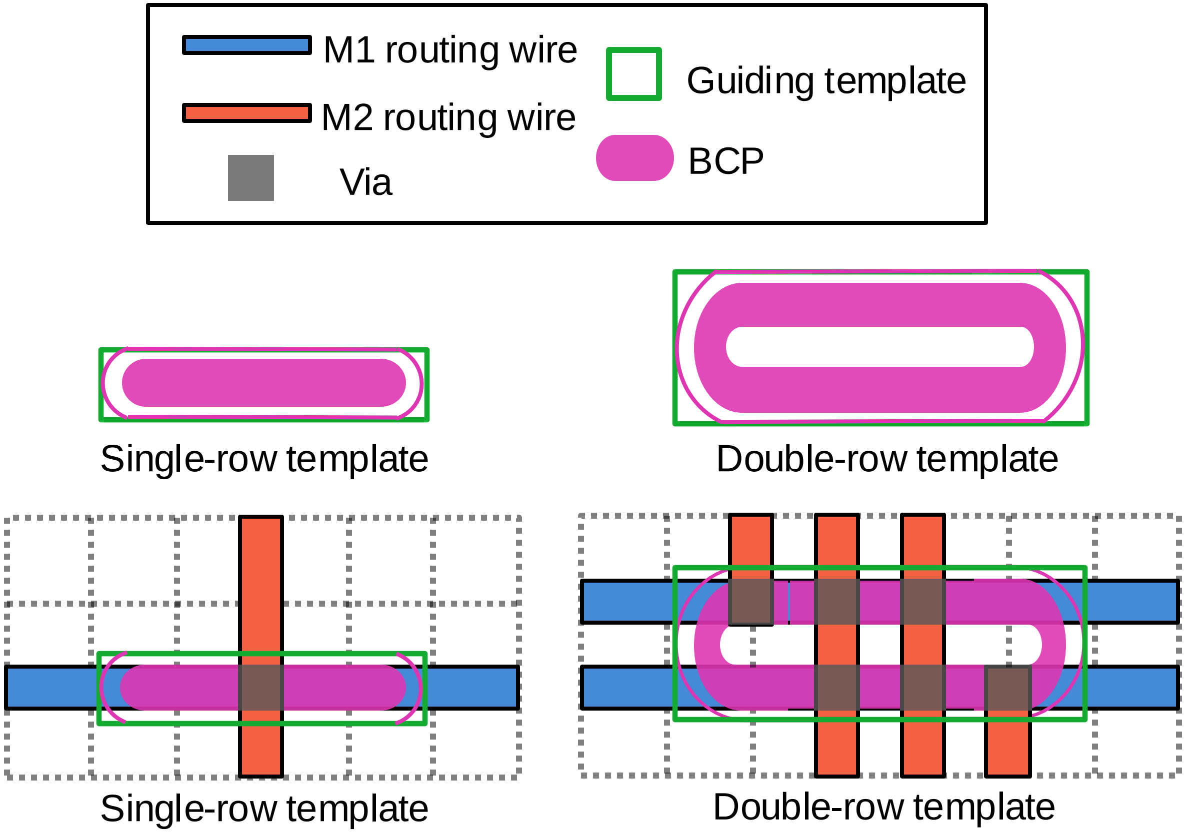
Outline

- Introduction
- Our Approaches
- Experimental Results
- Conclusion

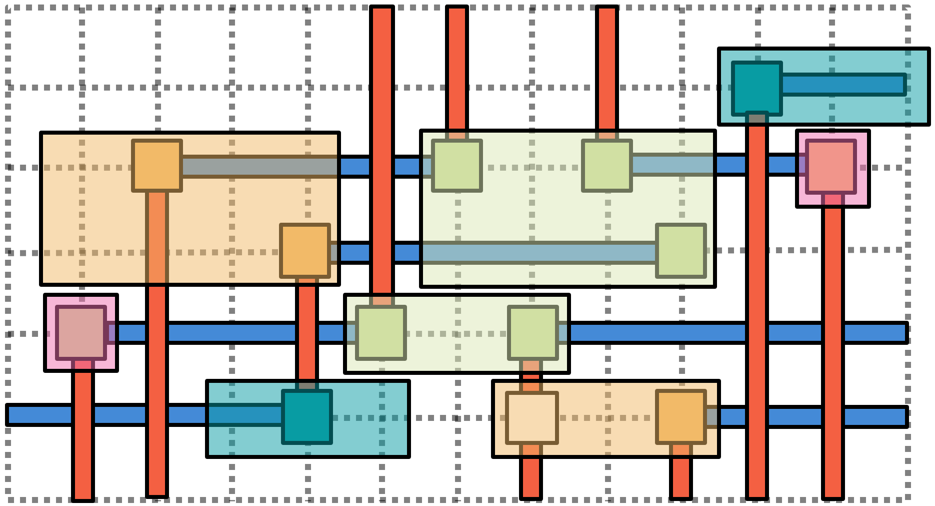
Lamellar DSA

- **Lamellar Directed Self-Assembly (Lamellar DSA)**
  - An advanced process for via layer fabrication



Introduction

- **Design Constraints**
  - Limited template shapes
    - Single-row templates: 1 x n
    - Double-row templates: 2 x n
    - Short template
      - 1 x 1 single-row template
      - 2 x 3 double-row template
  - Mask conflict
    - Layout decomposability
  - BCP violation
    - Circuit functionality



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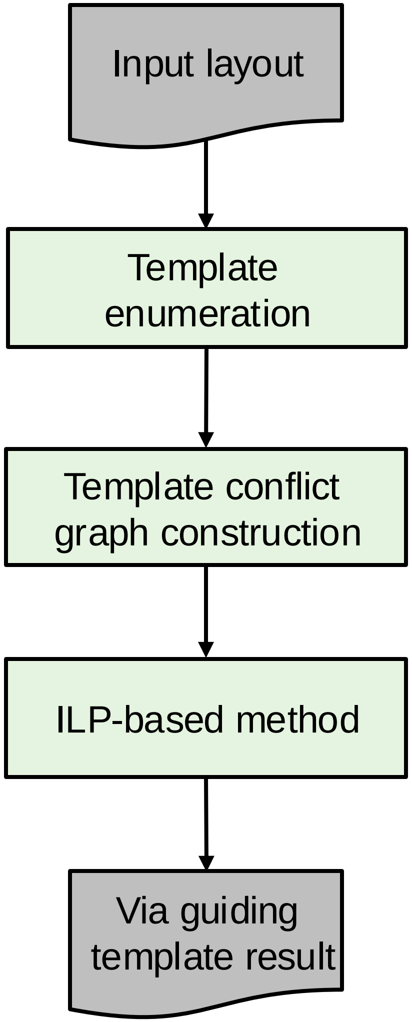
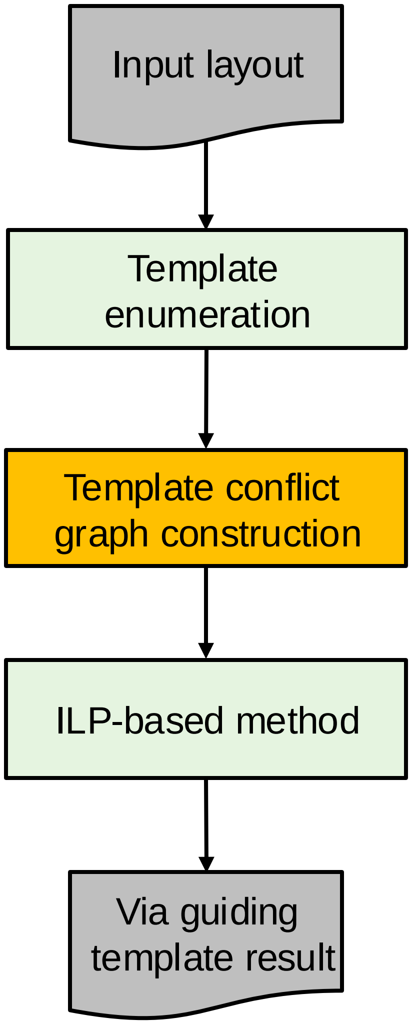
The proposed ILP flow



Template Enumeration

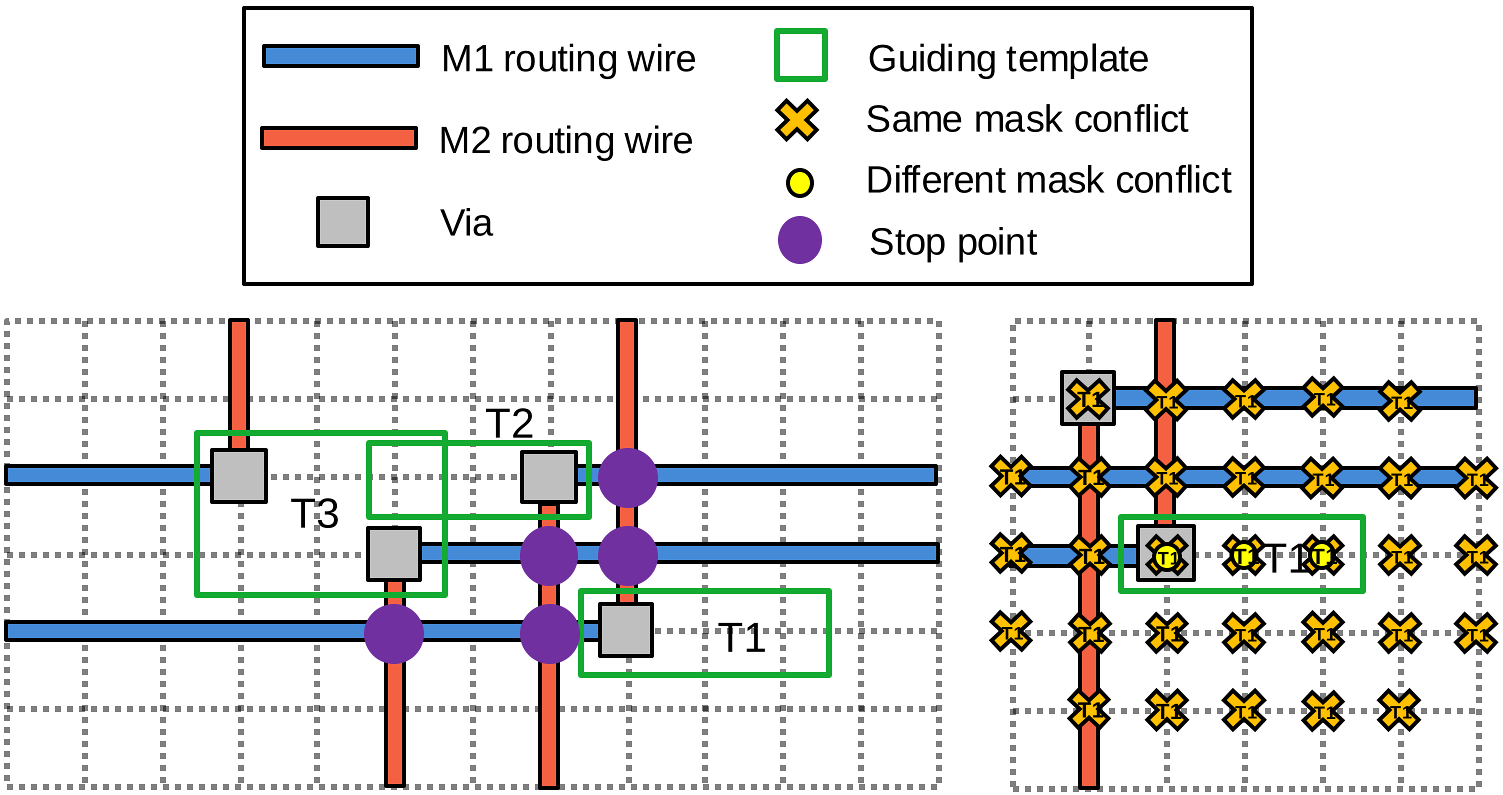
- **Given a via layout, construct a grid-based data structure (map)**
  - Vias location
  - Wire distribution (lower metal layer & upper metal layer)
  - Stop point: a grid point generating a BCP violation if it overlaps with a template
- **Single-row template**
  - 1 × 1 (short template)
  - 1 × 3
  - 1 × n
- **Double-row template**
  - 2 × 3 (short template)
  - 2 × 4
  - 2 × n

The Proposed ILP Flow

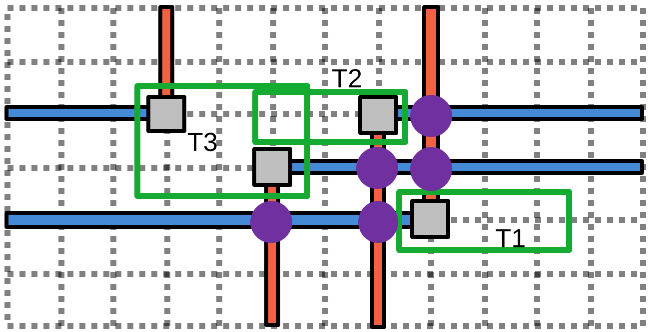


Template Conflict Graph Construction

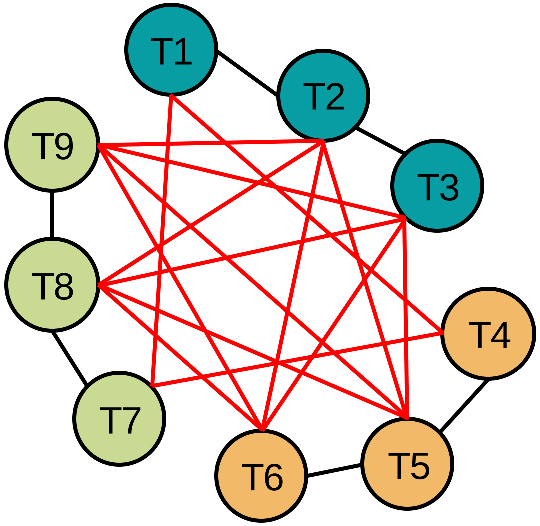
- **Mask conflict area of each template**
  - Same-mask conflict area
  - Different-mask conflict area



Template Conflict Graph Construction



	T1	T2	T3
Same mask	T2	T1、T3	T2
Different mask	Null	T3	T2

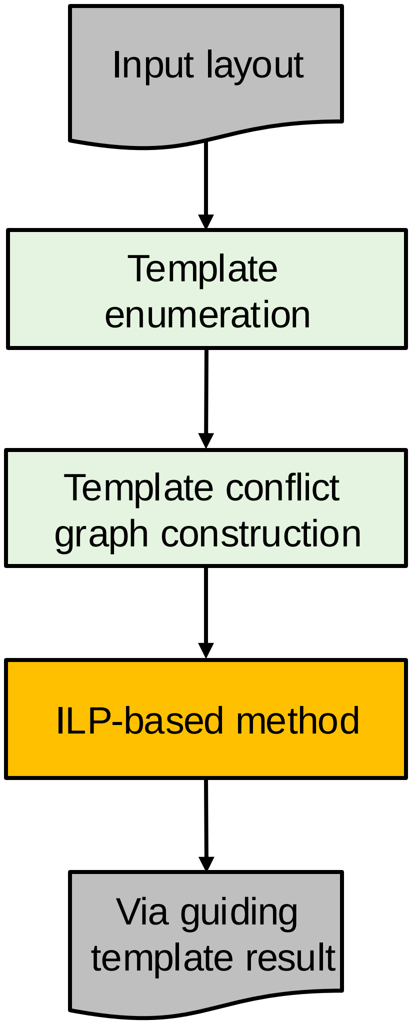


Conflict graph

	T1 (mask1)	T2 (mask1)	T3 (mask1)	T4 / T1 (mask2)	T5 / T2 (mask2)	T6 / T3 (mask2)	T7 / T1 (mask3)	T8 / T2 (mask3)	T9 / T3 (mask3)
Conflict edge	T2、T4、T7	T1、T3、T5、T6、T8、T9	T2、T5、T6、T8、T9	T5、T1、T7	T4、T6、T2、T3、T8、T9	T5、T2、T3、T8、T9	T8、T1、T4	T7、T9、T2、T3、T5、T6	T8、T2、T3、T5、T6

Conflict edge table

The Proposed ILP Flow



ILP-Based Method

- **Conflict graph**
  - Maximum weight independent set problem
    - Breadth-first search algorithm (BFS)
      - component
  - $\alpha = 1; \beta = 0.01$

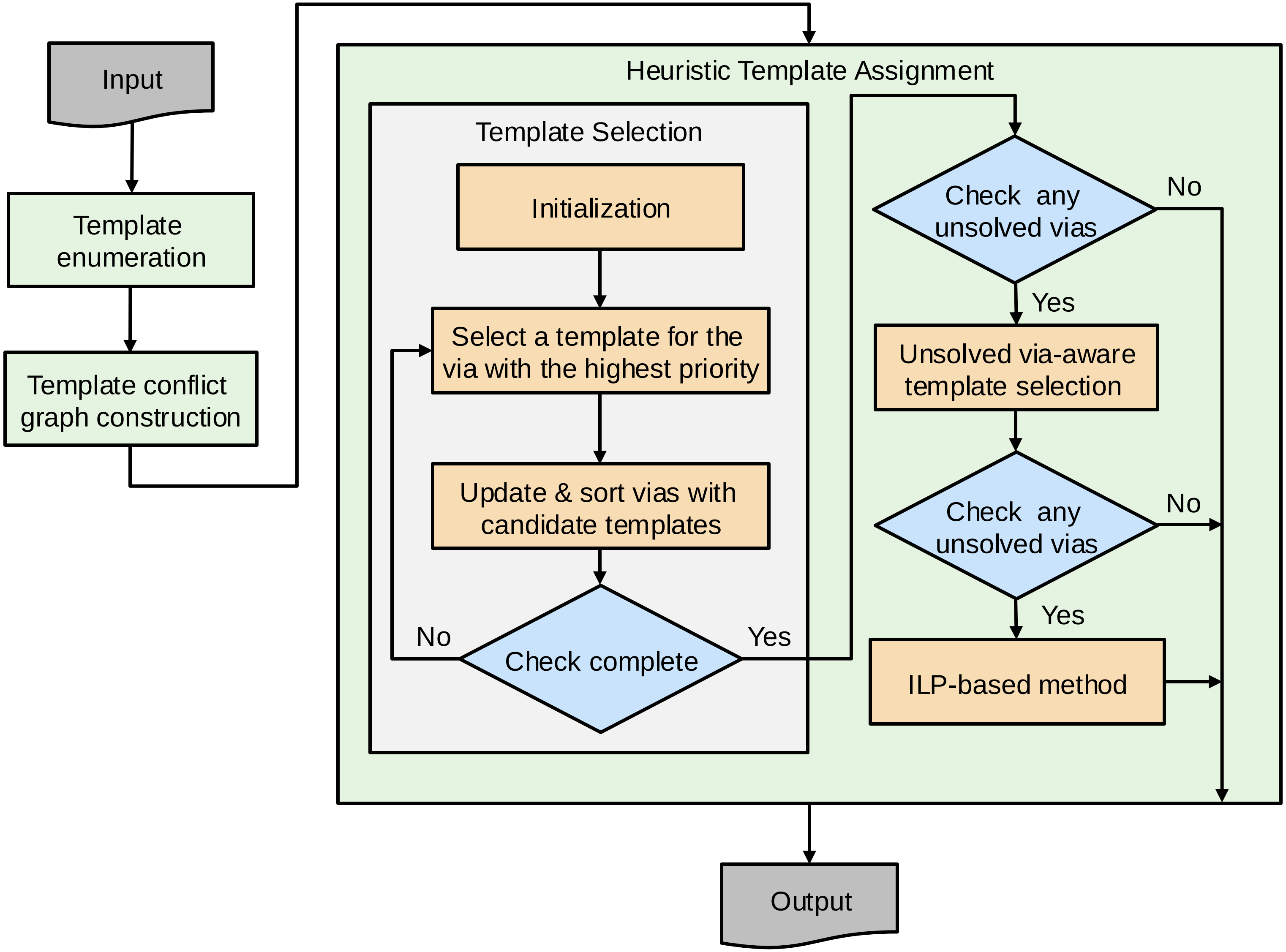
v_i	**The i-th node.**
n_{v_i}	The number of vias in the i-th node.
s_{v_i}	Boolean variable, $s_{v_i} = 1$ if v_i is a short template; $s_{v_i} = 0$, otherwise.
x_{v_i}	Boolean variable, $x_{v_i} = 1$ if v_i be chosen; $x_{v_i} = 0$, otherwise.
N	The set of nodes in a component.
E	The set of conflict edges in a component.

$$\max \quad \sum_{i=1}^{N} \left(\alpha \times n_{v_i} - \beta \times s_{v_i}\right) \times x_{v_i} \tag{1}$$

$$\text{s.t.} \quad x_{v_i} \in \{0, 1\}, \qquad i = 1, 2, \ldots, N \tag{2}$$

$$x_{v_i} + x_{v_j} \leq 1, \qquad \forall \{v_i, v_j\} \in E \tag{3}$$

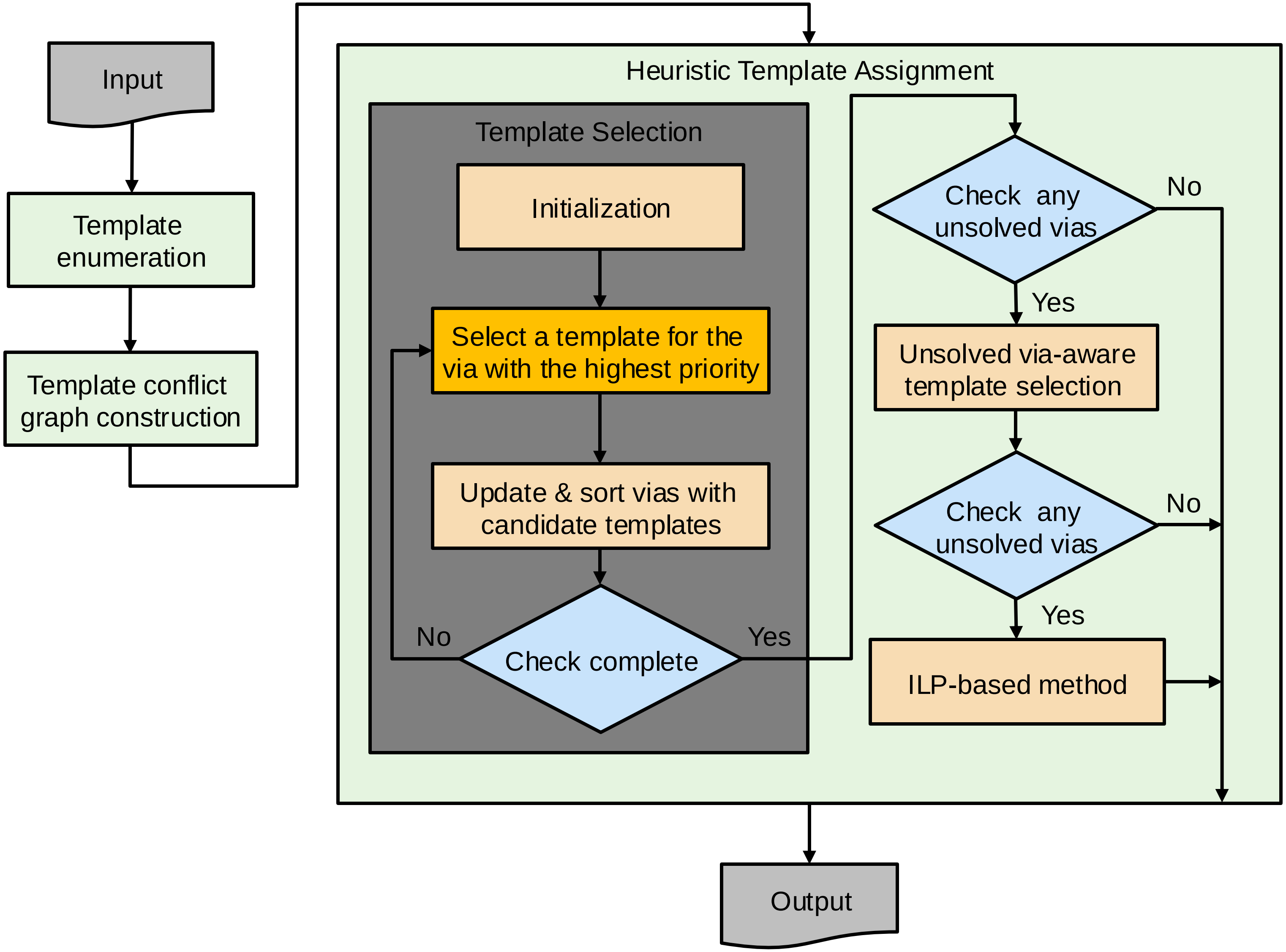
The Proposed Heuristic Flow



Initialization

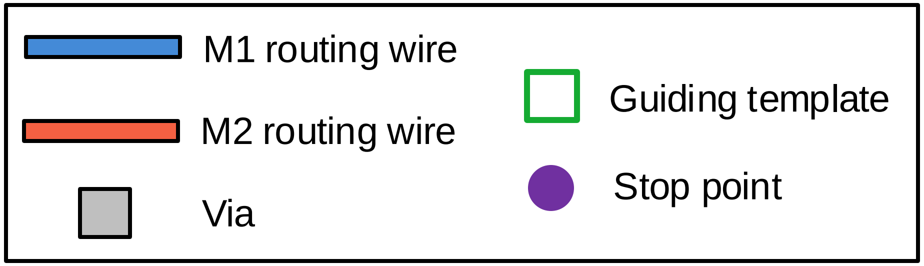
- **Give a weight to each node**
  - 1 × 1 (short template) 👉 1
  - 2 × 3 (short template) 👉 2
  - 1 × 3 (only one via) 👉 3
  - 1 × n 👉 the density of vias in a template × 15 (coefficient)
    - Ex. 1 × 6 template with 2 vias, weight = [2 / (1 × 6)] × 15 = 5
  - 2 × n 👉 the density of vias in a template × 25 (coefficient)
    - Ex. 2 × 4 template with 2 vias, weight = [2 / (2 × 4)] × 25 = 6.25 (rounded to 6)
- **Record # candidate templates for each via**
  - Each candidate template is assigned a specific mask color

The Proposed Heuristic Flow

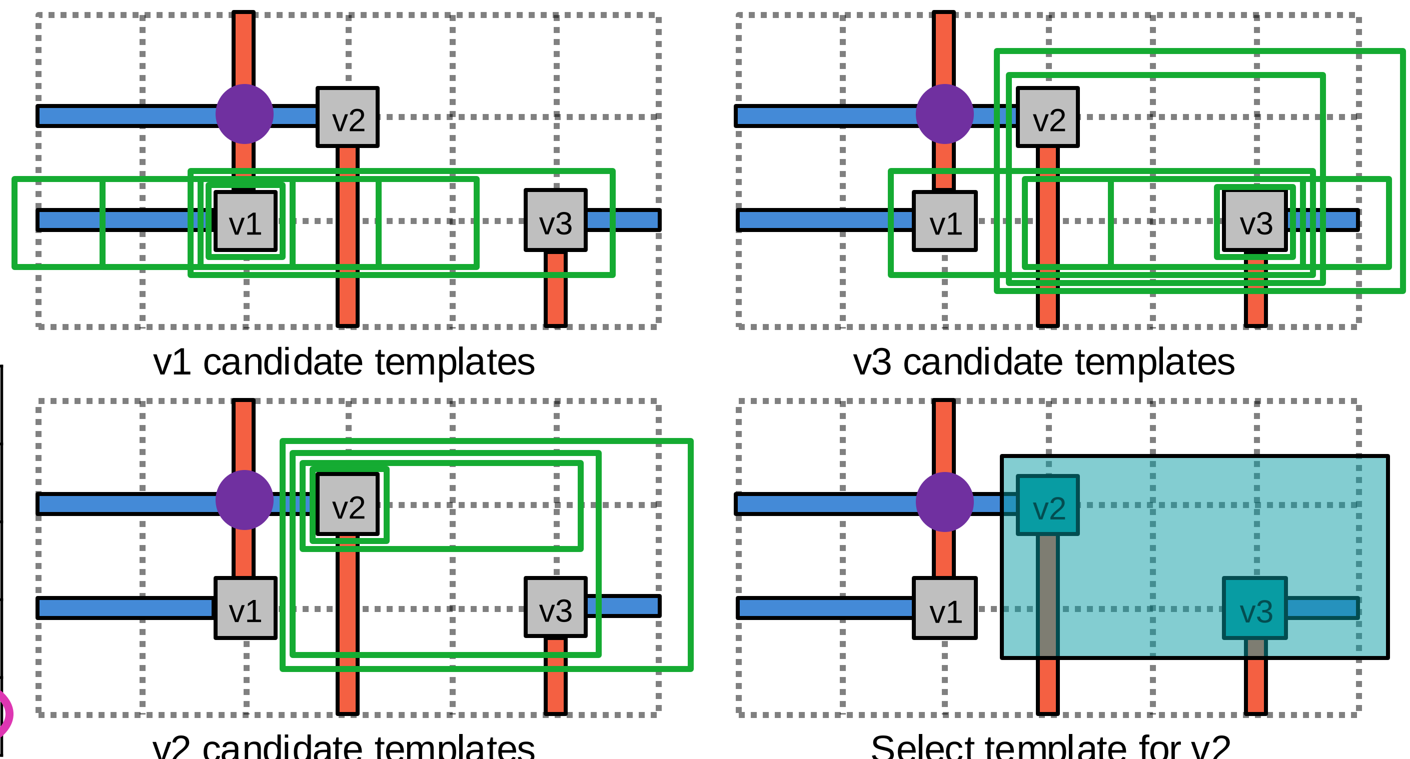


Select Template

- **Select a template for the via with the highest priority**

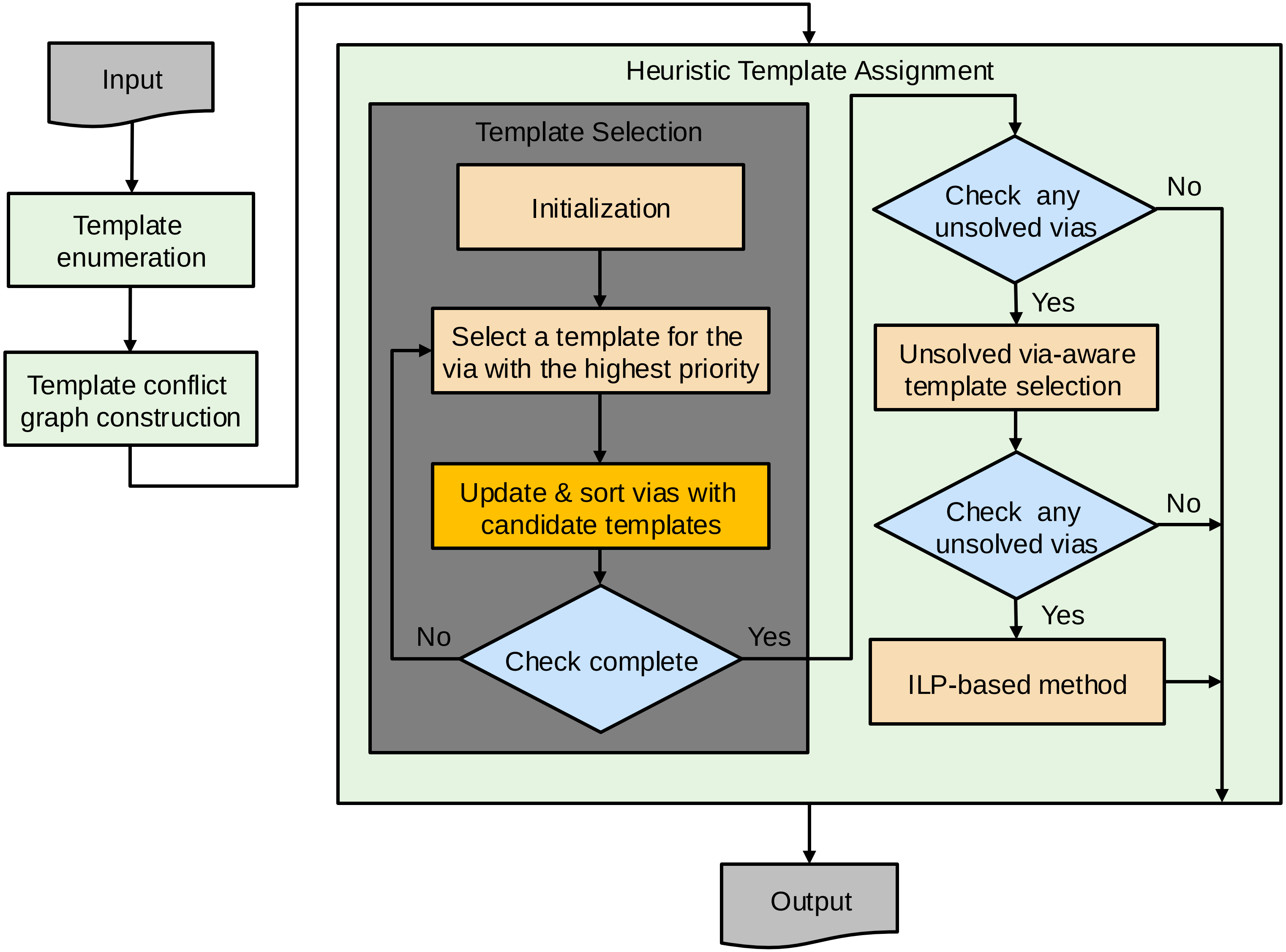


#Candidates	Via ID
12	v2
15	v1
18	v3



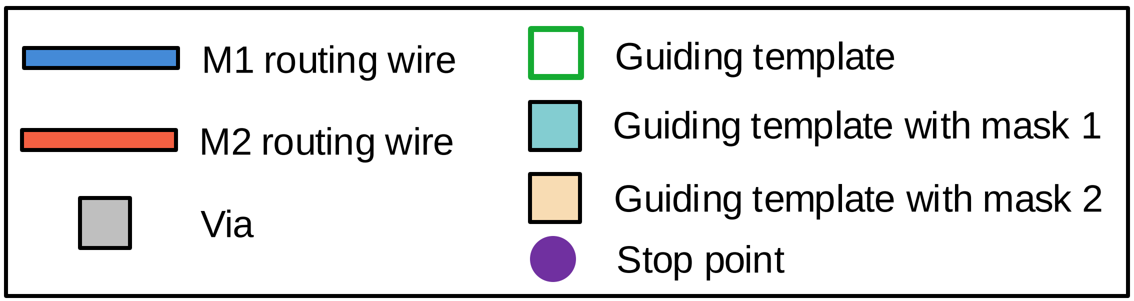
T	W
1 × 1	1
1 × 3	3
2 × 3	2
2 × 4	6

The Proposed Heuristic Flow

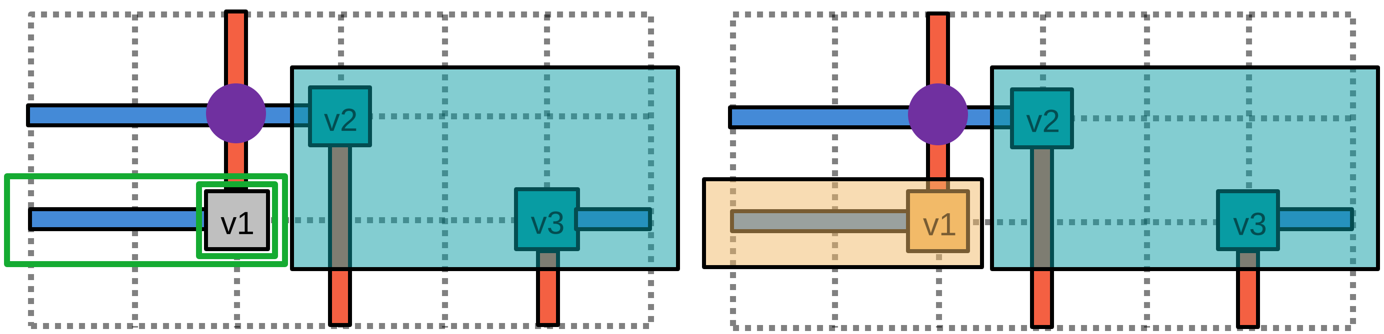


Update & Sort

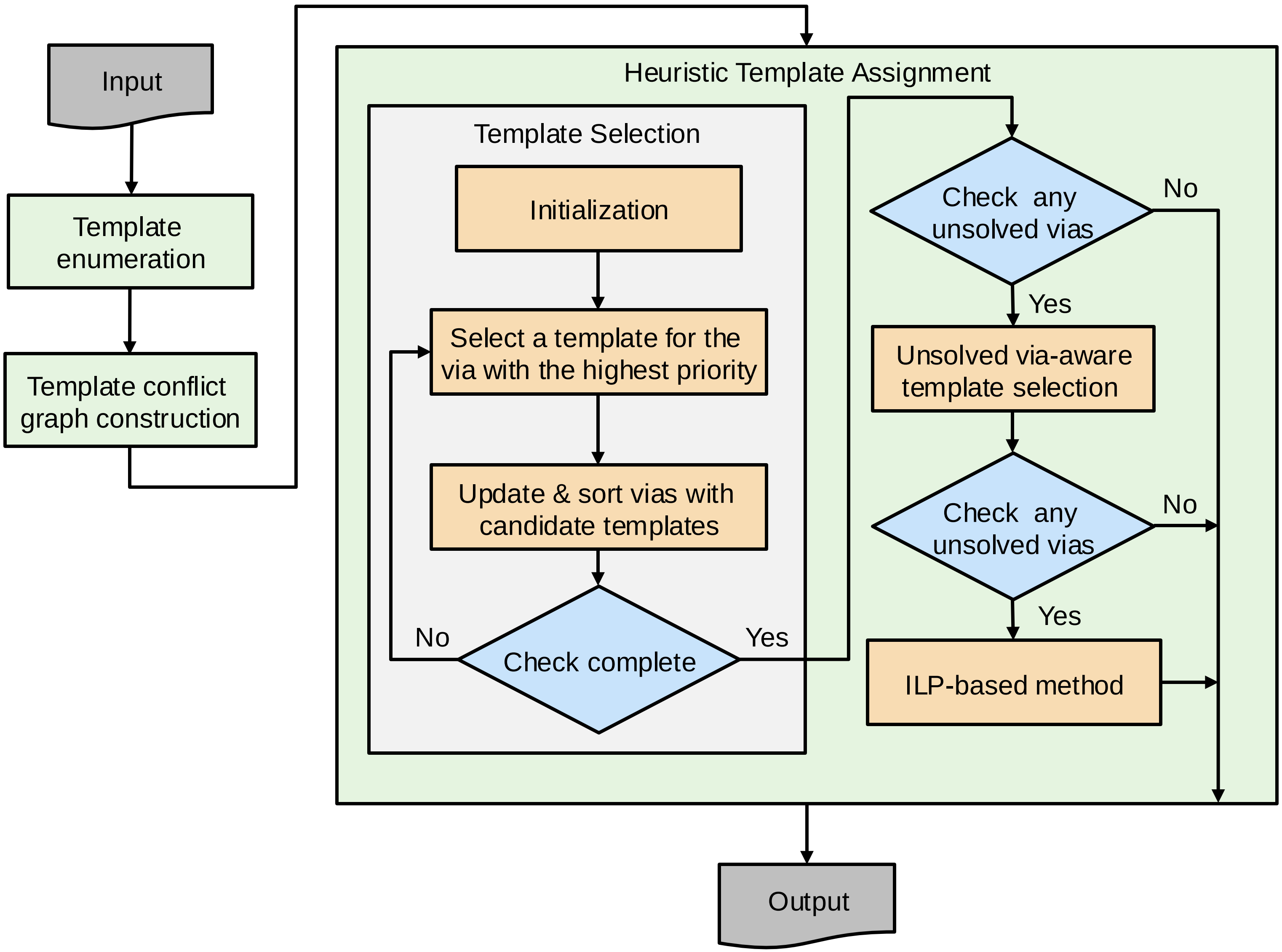
- **Check completeness (for each component)**
  - No more template candidate
  - No more unsolved via



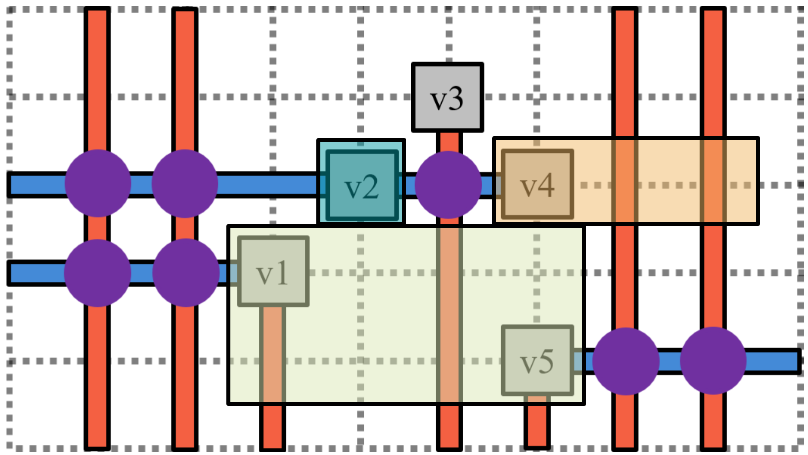
#Candidates	Via ID
4	v1
~~0~~	~~v2~~
~~0~~	~~v3~~



The Proposed Heuristic Flow



Template Selection



#Can	ID
3	v2
6	v4
9	v1
9	v5
12	v3

#Can	ID
4	v4
6	v1
7	v5
8	v3

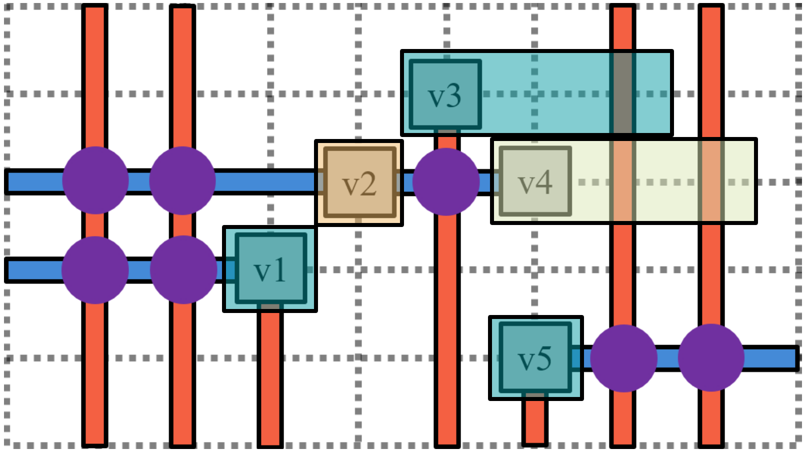
#Can	ID
4	v1
4	v3
4	v5

#Can	ID
~~0~~	~~v3~~
~~0~~	~~v5~~

Unsolved via ID
v3

Unsolved Via-Aware Template Selection

Unsolved via ID
v3



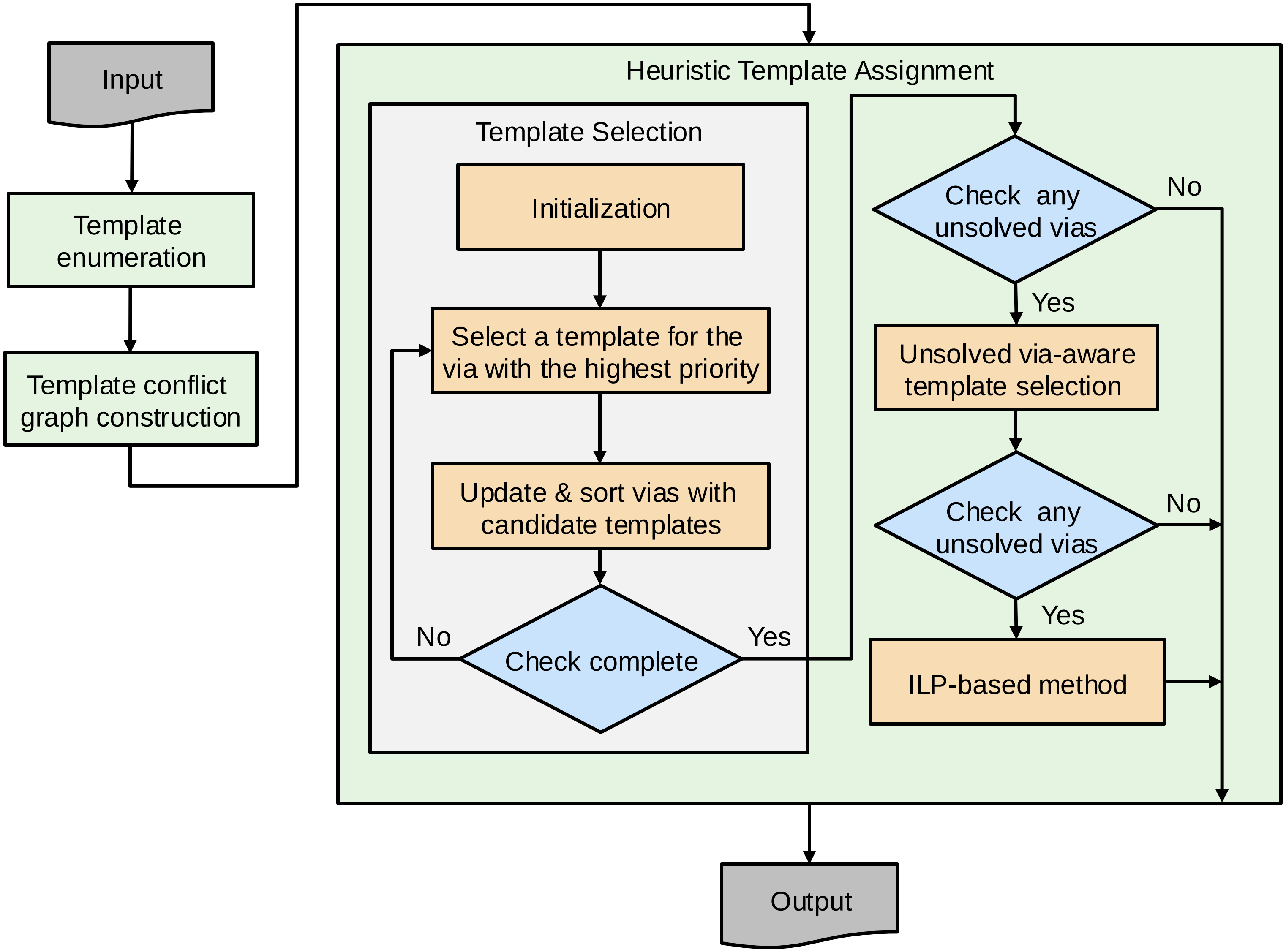
#Can	ID
2	v2
4	v4
7	v1
8	v5

#Can	ID
2	v4
4	v1
6	v5

#Can	ID
2	v1
3	v5

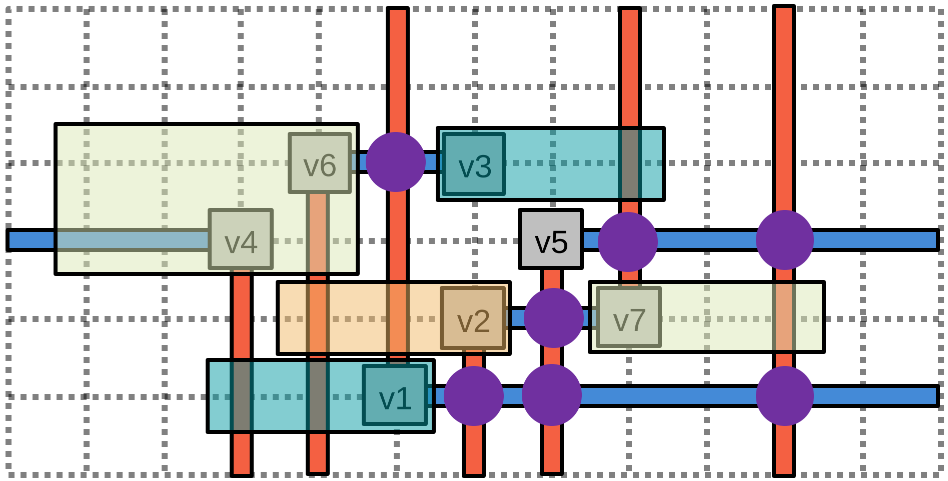
#Can	ID
1	v5

The Proposed Heuristic Flow



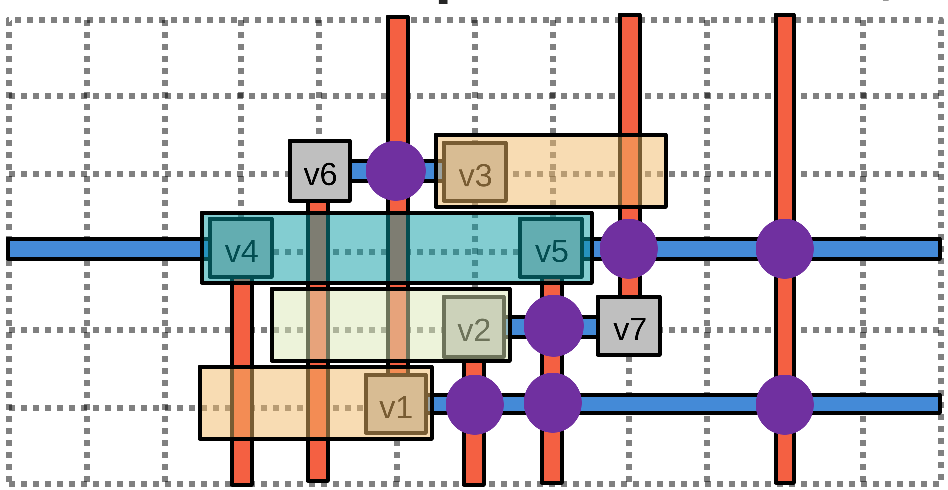
Unsolved Via (1/2)

- **Template selection**



Unsolved via ID
v5

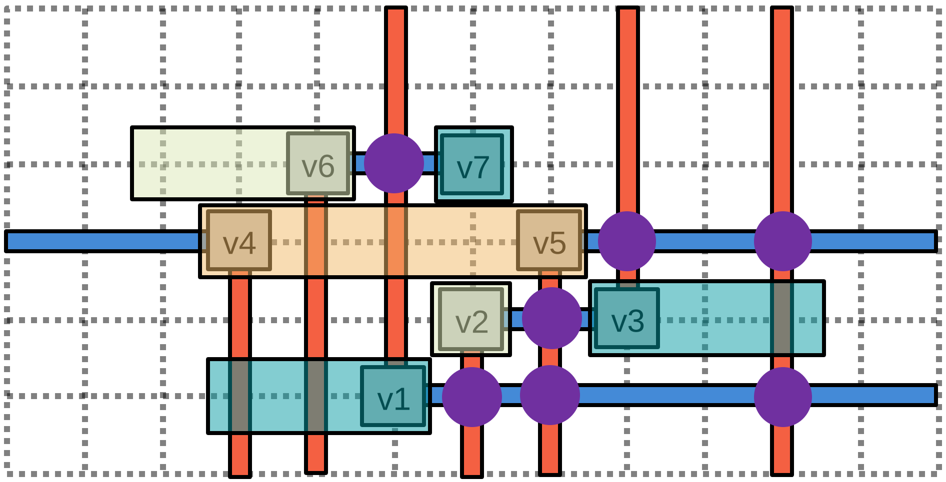
- **Unsolved via-aware template selection, v5**



Unsolved via ID
v6, v7

Unsolved Via (2/2)

- **ILP-based method**



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Experimental Setup (1/2)

- **Platform**
  - C++ programming language
  - 3.5 GHz CPU
  - 72 GB RAM
- **ILP solver**
  - CPLEX
- **Benchmarks**
  - ISPD 2015 placement contest

Experimental Setup (2/2)

- **For a fair comparison with [Shih et al., ICCAD'20], we applied the same experimental setups**
  - Width and spacing of metal wires are both 20 nm
  - The width of guiding template is set as 30 nm
  - The minimum mask spacing, L_{litho}, is set as 70 nm
- **ILP formulation**
  - α and β are set as 1 and 0.01

Experimental Results (1/2)

- **The comparison results of [Shih] and ours**
  - #V – the number of vias
  - #UV – the number of unsolved vias
  - #ST – the number of short templates

Case name	Original Layout		[14] ILP			Our ILP		
	Layer	#V	#UV	#ST	CPU	#UV	#ST	CPU
mgc_des_perf_1_routed	Via23	274,272	113	163,331	291	5	12,809	532
mgc_des_perf_a_routed	Via23	319,905	101	219,974	415	14	20,164	431
mgc_des_perf_b_routed	Via23	302,528	50	169,186	397	5	9,497	423
mgc_edit_dist_a_routed	Via23	583,804	452	499,716	744	186	198,790	554
mgc_fft_1_routed	Via23	91,244	53	52,815	96	4	3,739	202
mgc_fft_2_routed	Via23	99,027	25	61,041	117	1	4,950	138
mgc_fft_a_routed	Via23	87,673	31	45,202	111	1	3,230	171
mgc_fft_b_routed	Via23	91,683	37	54,854	113	4	4,791	178
mgc_pci_bridge32_a_routed	Via23	87,756	30	44,510	110	5	4,852	115
mgc_pci_bridge32_b_routed	Via23	73,027	7	32,829	93	0	1,512	143
Comp	-	-	1.000	1.000	1.000	0.111	0.108	1.366

Experimental Results (2/2)

- **The comparison results of our approaches**
  - #Component – the number of components
  - #MaxCOT – the maximum number of templates in a component
  - CPU –not include the time to build the data structure

Case name	Problem Size-related Information			Our ILP			Our Heuristic		
	Utilization (%)	#Component	#MaxCOT	#UV	#ST	CPU	#UV	#ST	CPU
mgc_des_perf_1_routed	70.01	15,364	24,810	5	12,809	389	5	13,583	408
mgc_des_perf_a_routed	42.90	73,832	15,414	14	20,164	314	14	20,991	37
mgc_des_perf_b_routed	49.71	70,627	4,836	5	9,497	312	5	10,134	14
mgc_edit_dist_a_routed	45.54	164,193	10,839	186	198,790	445	186	201,785	47
mgc_fft_1_routed	83.55	5,695	26,844	4	3,739	149	4	3,979	114
mgc_fft_2_routed	49.97	19,305	2,112	1	4,950	101	1	5,285	3
mgc_fft_a_routed	25.09	19,931	2,262	1	3,230	125	1	3,422	4
mgc_fft_b_routed	28.19	15,754	8,283	4	4,791	126	4	5,108	16
mgc_pci_bridge32_a_routed	38.39	27,301	2,274	5	4,852	87	5	5,020	2
mgc_pci_bridge32_b_routed	14.30	25,303	3,294	0	1,512	109	0	1,599	2
Comp	-	-	-	1.000	1.000	1.000	1.000	1.053	$\boxed{0.231}$

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Conclusion

- **We investigate the design methods of multi-row guiding templates for lamellar DSA with SAV process**
  - Consider the design constraints
- **Propose an ILP-based optimal method**
  - Maximize the number of vias that can be fabricated
  - Minimize short templates for yield optimization
- **Propose a heuristic method**
  - Speed up the running time
  - Find near-optimal solutions

Thank you