Call for Papers
ASP-DAC 2025

http://www.aspdac.com/
January 20-23, 2025
Miraikan (The National Museum of Emerging Science and Innovation), Tokyo, Japan

Aims of the Conference:

ASP-DAC 2025 is the 30th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design, CAD and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to design and Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC. ASP-DAC recognizes excellent contributions with the Best Paper Award and 10-Year Retrospective Most Influential Paper Award. Selected papers will be invited to submit the extended version of their work to a Special Issue of Integration, the VLSI Journal.

Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:
- 1.1. HW/SW co-design, co-simulation and co-verification
- 1.2. System-level design exploration, synthesis, and optimization
- 1.3. System-level formal verification
- 1.4. System-level modeling, simulation and validation
- 1.5. Networks-on-chip and NoC-based system design

[2] Embedded, Cyberphysical (CPS), IoT Systems, and Software:
- 2.1. Many- and multi-core SoC architecture
- 2.2. IP/platform-based SoC design
- 2.3. Dependable architecture
- 2.4. Cyber physical system and Internet of Things
- 2.5. Kernel, middleware, and virtual machine
- 2.6. Compiler and toolchain
- 2.7. Real-time system
- 2.8. Resource allocation for heterogeneous computing platform
- 2.9. Storage software and application
- 2.10. Human-computer interface

[3] Memory Architecture and Near/In Memory Computing:
- 3.1. Storage system and memory architecture
- 3.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
- 3.3. Memory/storage hierarchies and management for emerging memory technologies
- 3.4. Near-memory and in-memory computing

[4] Tools and Design Methods with and for Artificial Intelligence (AI)
- 4.1. Design method for learning on a chip
- 4.2. Deep neural network for EDA
- 4.3. Large language model (LLM) for circuit design and EDA
- 4.4. Tools and design methodologies for edge AI and TinyML
- 4.5. Efficient ML training and inference

[5] Hardware Systems and Architectures for AI:
- 5.1. Hardware, device, architecture, and system-level design for deep neural networks
- 5.2. Hardware acceleration for large language model
- 5.3. Neural network acceleration co-design techniques
- 5.4. Novel reconfigurable architectures, including FPGAs for AI/MLs

[6] Photonic/RF/Analog-Mixed Signal Design:
- 6.1. Analog/mixed-signal/RF synthesis
- 6.2. Analog layout, verification, and simulation techniques
- 6.3. High-frequency electromagnetic simulation of circuit
- 6.4. Mixed-signal design consideration
- 6.5. Communication and computing using photonics

[7] Approximate, Bio-Inspired and Neuromorphic Computing:
- 7.1. Circuit and system techniques for approximate, hyper-dimensional, and stochastic computing
- 7.2. Neuromorphic computing
- 7.3. CAD for approximate and stochastic systems
- 7.4. CAD for bio-inspired and neuromorphic systems

[8] High-Level, Behavioral, and Logic Synthesis and Optimization:
- 8.1. High-level/Behavioral synthesis tool and methodology
- 8.2. Combinational, sequential, and asynchronous logic synthesis
- 8.3. Synthesis for deep neural networks
- 8.4. Technology mapping, resource scheduling, allocation and synthesis
- 8.5. Functional, logic, and timing ECO (engineering change order)
- 8.6. Interaction between logic synthesis and physical design

[9] Physical Design and Timing Analysis:
- 9.1. Floorplanning, partitioning, placement and routing optimization
- 9.2. Interconnect planning and synthesis
- 9.3. Clock network synthesis
- 9.4. Post layout and post-silicon optimization
- 9.5. Package/PCB/3D-IC placement and routing
- 9.6. Extraction, TSV, and package modeling
- 9.7. Deterministic/statistical timing analysis and optimization

[10] Design for Manufacturability/Reliability and Low Power:
- 10.1. Reticle enhancement, lithography-related design and optimization
- 10.2. Resilience under manufacturing variation
- 10.3. Design for manufacturability, yield, and defect tolerance
- 10.4. Reliability, robustness, aging, and soft error analysis
- 10.5. Power modeling, analysis and simulation
- 10.6. Low-power design and optimization at circuit and system levels
- 10.7. Thermal aware design and dynamic thermal management
- 10.8. Energy harvesting and battery management
- 10.9. Signal/Power integrity, EM modeling and analysis

[11] Testing, Validation, Simulation, and Verification:
- 11.1. ATPG, BIST and DFT
- 11.2. System test and 3D IC test, online test and fault tolerance
- 11.3. Memory test and repair
- 11.4. RTL and gate-leveling modeling, simulation, and verification
- 11.5. Circuit-level formal verification
- 11.6. Device/circuit-level simulation tool and methodology

[12] Hardware and Embedded Security:
- 12.1. Hardware-based security
- 12.2. Detection and prevention of hardware trojans
- 12.3. Side-channel attacks, fault attacks and countermeasures
- 12.4. Design and CAD for security
- 12.5. Cyberphysical system security
- 12.6. Nanoelectronic security
- 12.7. Supply chain security and anti-counterfeiting
- 12.8. Security/privacy for LLM/AI/ML

[13] Emerging Devices, Technologies and Applications:
- 13.1. EDA and circuits design for quantum and Ising computing
- 13.2. Nanotechnology, MEMS
- 13.3. Biomedical, biochip, and biodata processing
- 13.4. Edge, fog and cloud computing
- 13.5. Energy-storage/smart-grid/smart-building design and optimization
- 13.6. Automotive system design and optimization
- 13.7. New transistor/device and process technology: spintronic, phase-change, single-electron, 2D materials, etc.

Authors must submit full-length, double-columned, original papers, with a maximum of 6 pages in PDF format (including the abstract, figures and tables) and are recommended to format their papers based on the ACM template. One page of references is allowed, which does not count towards the 6-page limitation. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals. The submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, references and bibliographic citations. While research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar), the authors' identities need to be anonymized in the submitted paper for the double-blind review process. Issuing the paper as a technical report, posting the paper on a website, or presenting the paper at a workshop that does not publish formally reviewed proceedings, does not disqualify it from appearing in the proceedings. Note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by any author.

Submission of Papers:

Deadline for abstract submission:	**5 PM AOE (Anywhere on earth)**	**July 5 (Fri), 2024**
Deadline for PDF uploading:	**5 PM AOE (Anywhere on earth)**	**July 12 (Fri), 2024**
Announcement of accepted manuscript IDs:		**Sept. 2 (Mon), 2024**
Notification of acceptance:		**Sept. 4 (Wed), 2024**
Deadline for final version:	**5 PM AOE (Anywhere on earth)**	**Nov. 1 (Fri), 2024**

For detailed instructions for submission, please refer to the "Authors' Guide" at:
http://www.aspdac.com/
Paper submission site:
https://tsys.jp/aspdac/cgi/submit_top.cgi

ASP-DAC 2025 Chairs

General Chair: **Yuichi Nakamura (NEC)**
Technical Program Chair: **Yu Wang (Tsinghua University)**
Technical Program Vice Chairs: **Takashi Sato (Kyoto University), Tsung-Yi Ho (CUHK)**

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to aspdac2025-ss@aspdac.com for special sessions & panels, aspdac2025-tutorial@aspdac.com for tutorials, no later than Aug 30 (Fri), 2024.

Contact: Conference Secretariat: aspdac2025@aspdac.com TPC Secretariat: aspdac2025-tpc@aspdac.com

Call for Designs

University LSI Design Contest
ASP-DAC 2025

http://www.aspdac.com/
January 20-23, 2025
Tokyo, Japan

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Aims of the Contest:

As a unique feature of ASP-DAC 2025, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

(1) Implemented on FPGAs/chips in universities or other educational organizations during the last two years.
(2) Designs that report actual measurements from implementations.
(3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.
Methods or technology used for implementation include:
(a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2-4 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at **http://www.aspdac.com/**

Deadline for summary:	5 PM AOE (Anywhere on Earth)	August 2 (Fri), 2024
Notification of acceptance:		Sep. 16 (Mon), 2024
Deadline for camera-ready:	5 PM AOE (Anywhere on Earth)	Nov. 8 (Fri), 2024

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:

(1) Novelty of application, algorithm, architecture, design, measurement, etc.
(2) Quality of design and implementation.
(3) Performance of the design.

Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2025. A separate poster session will be arranged to enable interactive discussion with the audience. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2025-udc@aspdac.com

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General Chair:	**Yuichi Nakamura (NEC)**
Technical Program Chair:	**Yu Wang (Tsinghua University)**
Technical Program Vice Chair:	**Takashi Sato (Kyoto University)**
Design Contest Co-Chairs:	**Shinya Takamaeda-Yamazaki (The University of Tokyo, Japan)**
	Mahfuzul Islam (Kyoto University, Japan)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM