Call for Participation

ASP-DAC

30th Asia and South Pacific Design Automation Conference

Date: January 20 – 23, 2025

Place: 7th Floor, Miraikan, The National Museum of Emerging Science and Innovation, Tokyo, Japan

Early Registration Due: Friday, December 13, 2024

Aims of the Conference

ASP-DAC is the largest conference in Asia and South-Pacific regions on Electronic Design Automation (EDA) area for VLSI and systems. ASP-DAC has been started at 1995 and this ASP-DAC 2025 is the **30th-anniversary** conference. ASP-DAC 2025 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas by technical papers and tutorials. ASP-DAC also holds Designers' Forum to make presentations about the latest designs for designers. Please do not miss ASP-DAC 2025.

Features of ASP-DAC 2025

■ **Keynote Speeches**

1. **January 21:** Kazunari Ishimaru (Rapidus, Japan), "Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry"
2. **January 22:** Jason Cong, (UCLA, USA), "Compilation and Architecture Optimization for Quantum Computing"
3. **January 23:** Abu Sebastian (IBM Research Europe - Zurich, Switzerland), "In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects"

■ **Tutorials**

Half-day tutorial sessions will take place on **January 20**. Conference participants can attend any of the following 4 topics taught by world-class experts.

Tutorial-1: Automation of Standard Cell Layout Generation and Design-Technology Co-optimization
Tutorial-2: AHS: An EDA toolbox for Agile Chip Front-end Design
Tutorial-3: Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification
Tutorial-4: Efficient Deployment of Large Language Models on Resource-Constrained Edge Computing Platforms

■ **Designers' Forum**

Designers' Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA academia/developers. This forum will take place on **January 22 and 23**. This year has 4 oral sessions: "Quantum Computing", "Advanced Sensor Technologies and Sensor Fusion", "Extending the Limits of Classical Computers using Emerging Device and Circuit Technology", and "Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence".

■ **University LSI Design Contest**

In University LSI Design Contest, state-of-the-art LSI and/or system designs compete on their design excellence and implementation quality. 17 high-quality designs all including actual measurement proof will be introduced at the design contest session on **January 21**.

■ **Technical Sessions**

There are 168 high quality papers selected from 578 submissions. We also plan 9 special sessions: "Machine Learning Based Physical Simulation and Physics-Aware Optimization", "Advances in 3D-IC and Ultra-Large-Scale Integration", "LLM Acceleration and Specialization for Circuit Design and Edge Applications", "ML for IC Design and Manufacturing: When Is It Real?", "Beyond Digital: Advancing Design Automation for Physical Computing Systems", "Rapidus' Initiatives to Half Semiconductor Development Time", "Hardware Authenticity towards a Trustworthy Society", "Innovations and Challenges on Cryo-CMOS Devices, Circuits and Design Platforms", "CEDA/CASS/SSCS Joint session on Silicon Photonics".

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