ASP-DAC 2025

30th Asia and South Pacific Design Automation Conference

FINAL PROGRAM

Date: January 20-23, 2025

Place: Miraikan 7F
The National Museum of Emerging Science and Innovation

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ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

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ASP-DAC 2025

Contents

Welcome to ASP-DAC 2025

On behalf of the Organizing Committee, I would like to invite all the engineers on the LSI design and design automation fields to the 30th Asia and South Pacific Design Automation Conference (ASP-DAC 2025). We are very happy to celebrate the 30th anniversary of ASP-DAC. I want to thank all who have helped to make ASP-DAC possible for 30 years, and many thanks to all successive SC and OC members, TPC members, contributors and participants.

ASP-DAC is a high-quality and premium conference on Electronic Design Automation (EDA) like other sister conferences such as Design Automation Conference (DAC), Design, Automation & Test in Europe (DATE), International Conference on Computer Aided Design (ICCAD), and Embedded Systems Week (ESWEEK). ASP-DAC started in 1995 and has continuously offered opportunities to learn about the advancements on LSI design and design automation fields, as well as to communicate with each other for researchers and designers around Asia and South Pacific regions.

We have 3 keynotes to share the latest trends in this area, message to design engineers from foundry, CAD for quantum circuits and in-memory computing for AI:

1. “Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry”, by Dr. Kazunari Ishimaru, Rapidus.
2. “Compilation and Architecture Optimization for Quantum Computing”, by Prof. Jason Cong, UCLA.
3. “In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects”, by Dr. Abu Sebastian, IBM Research Europe – Zurich

We believe everyone will be very satisfied with these valuable keynote talks.

ASP-DAC 2025 includes Technical Sessions, Special Sessions, Keynotes, Designers’ Forum, University Design Contest, Tutorial, and social events. ASP-DAC 2025 received 537 submissions from all over the world. Based on rigorous and thorough reviews and a face-to-face meeting by the Technical Program Committee, 168 papers have been accepted and 39 technical sessions have been organized. Nine Special Sessions have also been organized based on invited talks by the Technical Program Committee.

The Designers’ Forum is a unique program that will share design experiences and solutions of actual product designs of the industry. The topics discussed in this forum include Quantum Computing, Advanced Sensor Technologies and Sensor Fusion, Extending the Limits of Classical Computers Using Emerging Device and Circuit Technology, and Integrated Circuit Design Methodologies Using Open Source and Artificial Intelligence. The University Design Contest is also an important annual event of ASP-DAC where 17 high-quality designs, all including actual silicon proof, were selected for presentation with Q&A at poster. Furthermore, at WIP (Work In Progress) poster session, you can present and discuss ongoing research with experts from the design automation community around the world.

Four tutorials have been arranged on January 20th. Each tutorial has a 3 hour presentation. The topics given in Tutorial includes Agile design methodologies and LLM on the edge. In this year you can attend the tutorial without additional tutorial fee. These tutorials will help you gain the latest knowledge about design area.

ASP-DAC 2025 offers you an ideal opportunity to touch the recent technologies and the future directions of the LSI design and design automation fields. So please do not miss ASP-DAC 2025 conference and enjoy Japan as well. Finally, we would like to express our sincere appreciation to those who have contributed to ASP-DAC 2025, including authors, speakers, reviewers, session organizers, session chairs, sponsors, supporters, and committee members.

Yuichi Nakamura
General Chair, ASP-DAC 2025

Message from the Technical Program Committee

Yu Wang

Takashi Sato

Tsung-Yi Ho

On behalf of the Technical Program Committee (TPC), it is our tremendous pleasure to welcome you to the 30th Asia and South Pacific Design Automation Conference (ASP-DAC) 2025, scheduled from January 20 to 23, 2025, at Tokyo Odaiba Miraikan, Japan.

This year, the call for papers of ASP-DAC 2025 employed a two-step procedure, where each submission first registered its abstract and subsequently submitted the full manuscript. We received total 587 abstracts, and of those registered abstracts, we received 537 full manuscripts from 29 counties/regions. The number of submissions reaches a record high, reflecting the thriving development of our field. The highest submissions came from the Asia region, followed by North America and Europe. In addition, China and USA contributed nearly 51% of the total submission. To better reflect the submission trend in recent years, we split the design methods with & for Artificial Intelligence (AI) track into two dedicated tracks, "Tools and Design Methods with AI" and "Tools and Design Methods for AI." In addition to continued strong submissions in fundamental EDA topics such as physical design and timing analysis, system-level modeling and design methodology, design for manufacturability/reliability, etc., we received substantial submissions and support in the area of AI hardware systems and architectures. We have also seen a significant increase in new computing paradigms such as near/in memory computing, approximate and bio-inspired computing, and quantum computing. Meanwhile, hardware and embedded security continued to be a strong track as well. These submission trends are strong evidence that ASP-DAC is actively reflecting and correlating with the state-of-the-art research in both academia and industry. We organized the Technical Program Committee (TPC) with 144 professionals who are leading experts in EDA, IC design, embedded system design, memory architectures, hardware security, emerging technologies & applications, AI/ML systems, and formed 14 subcommittees. The paper selection process ensured fairness through a rigorous double-blind review process with tight control of conflicts of interest. We held a face-to-face and partially hybrid TPC meeting at Marco Polo Hong Kong Hotel, Hong Kong SAR, China on August 30, 2024. Out of the 537 submissions, 168 high-quality regular papers were selected, representing a very competitive acceptance rate of 31%, further demonstrating that ASP-DAC strives to be a premier conference with technical strengths.

The complete conference program consists of the regular papers, keynote speeches, as well as strong set of special sessions, designers' forums, and design contest sessions. We have tutorials on the first day of the conference, with regular programs compiled into three-day, six parallel sessions. The keynotes are held every morning to kick off the technical sessions. Among the accepted regular papers, 13 were nominated from sub-committees for the Best Paper Award. These best paper candidates went through a thorough evaluation process by the Best Paper Award Committee which is chaired by Vice Technical Program Chair Prof. Takashi Sato, and finally two Best Papers were selected. In addition, Prof. Takashi Sato also chaired the 10-year Retrospective Most Influential Paper selection committee and selected one from papers published in the proceedings of the 20th ASP-DAC conference in 2015.

The exciting and stimulating technical program of ASP-DAC 2025 is the outcome of the hard work and efforts from the authors, reviewers, invited speakers, and TPC members. We would like to sincerely thank all of them. Special thanks go to the TPC Secretaries, Zhenhua Zhu and Jun Shiomi, the conference secretaries, Yuki Kobayashi, Jun Shiomi, and Yukihide Kohira, the publication chairs, Kohei Miyase, Shinobu Nagayama, and Tetsuya Iizuka, and web publicity chairs, Junichiro Kadomoto and Yutaka Masuda, for their extraordinary support. Additionally, we thank Satoshi Taoka for his support in the TPC and review management system. Last but not least, the deepest thanks go to the entire Organizing Committee for their excellent efforts in organizing and hosting a great conference.

We hope you all enjoy the ASP-DAC 2025 technical program and we'll meet you all in Tokyo Japan.

Yu Wang
TPC Chair, ASP-DAC 2025

Takashi Sato
TPC Vice Chair

Tsung-Yi Ho
TPC Vice Chair

Session Schedule

Monday, January 20, 2025

Room Saturn	Innovation Hall
T1 Tutorial-1: Automation of Standard Cell Layout Generation and Design-Technology Co-optimization 9:30 - 12:30	T2 Tutorial-2: AHS: An EDA toolbox for Agile Chip Front-end Design 9:30 - 12:30
T3 Tutorial-3: Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification 14:30 - 16:30	T4 Tutorial-4: Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms 14:30 - 17:30

Tuesday, January 21, 2025

Room Saturn	Room Uranus	Room Venus	Room Mars/Mercury	Innovation Hall	Miraikan Hall
1K (Miraikan Hall) Opening and Keynote Session I 8:30 - 9:45					
Coffee Break 9:45 - 10:05					
1A (T1-1) System-Level Modeling and Design Methodologies 10:05 - 11:45	1B (T4.2-1) Tools and Techniques for On-Device AI Deployment 10:05 - 11:45	1C (T8-1) AI and Logic Synthesis - A perfect match? 10:05 - 11:20	1D (T3-1) Application-Specific Computing-In-Memory 10:05 - 11:45	1E (SS-1) Machine Learning Based Physical Simulation and Physics-Aware Optimization 10:05 - 11:45	1F (SS-CEDA) CEDA/CASS/SSCS Joint session on Silicon Photonics 10:05 - 11:45
Lunch Break 11:45 - 13:15					
2A (T5-1) Accelerating Vision and Transformer Models 13:15 - 15:20	2B (T6-1) Shaping the Future of Analog EDA 13:15 - 14:55	2C (T7-1) Approximate and Stochastic Computing 13:15 - 15:20	2D (T2-1) Next-Generation Embedded Architectures and Tools 13:15 - 15:20	2E (SS-2) Advances in 3D-IC and Ultra-Large-Scale Integration 13:15 - 15:20	2F University Design Contest 13:15 - 15:20
Coffee Break 15:20 - 15:40					
3A (SS-3) LLM Acceleration and Specialization for Circuit Design and Edge Applications 15:40 - 17:20	3B (T9-1) Timing Analysis and Optimization 15:40 - 17:45	3C (T12-1) Side Channel Attacks and Trusted Execution Environment 15:40 - 17:45	3D (T3-2) Frameworks and Modeling for Computing-In-Memory 15:40 - 17:20	3E (T4.1-1) AI/ML for Circuit Design and Prediction 15:40 - 17:45	
1S (Room Jupiter) ACM SIGDA Student Research Forum / WIP Poster Session 18:00 - 20:00					

Wednesday, January 22, 2025

Room Saturn	Room Uranus	Room Venus	Room Mars/Mercury	Innovation Hall	Miraikan Hall
2K (Miraikan Hall) 30th Anniversary and Keynote Session II 8:30 - 9:45					
Coffee Break 9:45 - 10:05					
4A (T4.2-2) Advanced Methods in AI Hardware Co-Design 10:05 - 11:45	4B (T1-2) Communication Networks 10:05 - 11:45	4C (T2-2) Design and Optimization of Emerging Embedded Applications 10:05 - 11:45	4D (T11-1) Verification and Testing in Machine Lerning Era 10:05 - 11:45	4E (T3-3) Hybrid/Co-Designed Near/In Memory Computing 10:05 - 11:45	4F (SS-4) ML for IC Design and Manufacturing: When Is It Real? 10:05 - 11:45
1W (Innovation Hall and more) CEDA 20th Anniversary Panel 12:00 - 13:00					
5A (T5-2) Innovations in Deep Learning and Neural Network Acceleration 13:15 - 15:20	5B (T7-2) Neuromorphic and Emerging Computing Techniques 13:15 - 15:20	5C (T9-2) Package and PCB 13:15 - 14:55	5D (T12-2) Logic Locking and Hardware Watermarking 13:15 - 14:55	5E (T4.1-2) AI-Driven Innovative Design Methods 13:15 - 15:20	5F (DF-1) Quantum Computing 13:15 - 14:30
Coffee Break 15:20 - 15:40					
6A (SS-5) Beyond Digital: Advancing Design Automation for Physical Computing Systems 15:40 - 17:20	6B (T9-3) Floorplan and Placement 15:40 - 17:45	6C (T13-1) Let's Quantumize: Welcome to the World of Quantum 15:40 - 16:55	6D (T10-1) Innovative Techniques for Energy-Efficient and Reliable Hardware Systems 15:40 - 17:45	6E (T4.1-3) Leveraging Large Language Models in Hardware Design 15:40 - 17:45	6F (DF-2) Advanced Sensor Technologies and Sensor Fusion 15:40 - 16:55
Banquet 18:30 - 20:30					

Thursday, January 23, 2025

Room Saturn	Room Uranus	Room Venus	Room Mars/Mercury	Innovation Hall	Miraikan Hall
3K (Miraikan Hall) Keynote Session III 9:00 - 9:45					
Coffee Break 9:45 - 10:05					
7A (T1-3) Accelerator Design Methodologies 10:05 - 11:45	7B (T5-3) Advanced Architectures for Scientific and Edge Computing 10:05 - 11:45	7C (T6-2) The Science of Light: the New Advancement of Photonic Computing 10:05 - 11:45	7D (T8-2) From Math to Circuits 10:05 - 11:20	7E (T4.2-3) Innovative Techniques in AI Model Optimization and Training 10:05 - 11:20	7F (SS-6) Rapidus' Initiatives to Half Semiconductor Development Time 10:05 - 11:20
Lunch Break 11:45 - 13:15					
8A (T1-4) System Level Modelling & Optimization 13:15 - 14:55	8B (T5-4) Emerging Trends in Reconfigurable and Compute-in-Memory 13:15 - 14:55	8C (T3-4) Adaptive and Flexible Memory Architecture 13:15 - 14:55	8D (T9-4) Reliability in Physical Design 13:15 - 14:55	8E (SS-7) Hardware Authenticity towards a Trustworthy Society 13:15 - 14:55	8F (DF-3) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology 13:15 - 14:30
Coffee Break 14:45 - 15:20					
9A (T12-3) Homomorphic Encryption and Cloud Security 15:20 - 17:30	9B (T11-2) Advanced Modeling, Simulation, and Verification 15:20 - 17:30	9C (T13-2) Carbon, Light, Fluids: Emerging Technologies 15:20 - 17:30	9D (T10-2) Advanced Techniques for Power Optimization and IR Prediction 15:20 - 17:30	9E (SS-8) Innovations and Challenges on Cryo-CMOS Devices, Circuits and Design Platforms 15:20 - 17:30	9F (DF-4) Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence 15:20 - 16:35

DF: Designers' Forum, SS: Special Session

Highlights

Opening and Keynote I

Tuesday, January 21, 2025, 9:00-9:45

Kazunari Ishimaru **(Rapidus Corporation)**
"Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry"

Keynote II

Wednesday, January 22, 2025, 9:00-9:45

Jason Cong **(UCLA)**
"Compilation and Architecture Optimization for Quantum Computing"

Keynote III

Thursday, January 23, 2025, 9:00-9:45

Abu Sebastian **(IBM Research Europe – Zurich)**
"In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects"

Special Sessions

1E (SS-1): (Invited Talks) Machine Learning Based Physical Simulation and Physics-Aware Optimization
Tuesday, January 21, 2025, 10:05-11:45

1F (SS-CEDA): (Invited Talks) CEDA/CASS/SSCS Joint session on Silicon Photonics
Tuesday, January 21, 2025, 10:05-11:45

2E (SS-2): (Invited Talks) Advances in 3D-IC and Ultra-Large-Scale Integration
Tuesday, January 21, 2025, 13:15-15:20

2F: (Presentation + Poster Discussion) University Design Contest
Tuesday, January 21, 2025, 13:15-15:20

3A (SS-3): (Invited Talks) LLM Acceleration and Specialization for Circuit Design and Edge Applications
Tuesday, January 21, 2025, 15:40-17:20

4F (SS-4): (Invited Talks) ML for IC Design and Manufacturing: When Is It Real?
Wednesday, January 22, 2025, 10:05-11:45

1W: (Panel Discussion) CEDA 20th Anniversary Panel
Wednesday, January 22, 2025, 12:00-13:00

6A (SS-5): (Invited Talks) Beyond Digital: Advancing Design Automation for Physical Computing Systems
Wednesday, January 22, 2025, 15:40-17:20

7A (SS-6): (Invited Talk) Rapidus' Initiatives to Half Semiconductor Development Time
Thursday, January 23, 2025, 10:05-11:20

8E (SS-7): (Invited Talks) Hardware Authenticity towards a Trustworthy Society
Thursday, January 23, 2025, 13:15-14:55

9E (SS-8): (Invited Talks) Innovations and Challenges on Cryo-CMOS Devices, Circuits and Design Platforms
Thursday, January 23, 2025, 15:20-17:30

Designers' Forum

5F (DF-1): (Oral Session) Quantum Computing

Wednesday, January 22, 2025, 13:15-14:30

6F (DF-2): (Oral Session) Advanced Sensor Technologies and Sensor Fusion

Wednesday, January 22, 2025, 15:40-16:55

8F (DF-3): (Oral Session) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology

Thursday, January 23, 2025, 13:15-14:30

9E (DF-4): (Panel Discussion) Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence

Thursday, January 23, 2025, 15:20-16:35

Tutorials

ASP-DAC 2025 offers attendees a set of three-hour intense introductions to specific topics. If you register for the conference, you have the option to select two out of the four topics. T2 is a session with hands-on training.

Tutorial-1: Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

Monday, January 20, 2025, 9:30-12:30 @ Room Saturn

Speaker:

Taewhan Kim (Seoul National University)

Tutorial-2: AHS: An EDA toolbox for Agile Chip Front-end Design

Monday, January 20, 2025, 9:30-12:30 @ Innovation Hall

Speakers:

Yun (Eric) Liang (Peking University)

Youwei Xiao (Peking University)

Ruifan Xu (Peking University)

Tutorial-3: Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

Monday, January 20, 2025, 14:30-16:30 @ Room Saturn

Speaker:

Prashant Seetharaman (Siemens Digital Industries Software)

Tutorial-4: Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Monday, January 20, 2025, 14:30-17:30 @ Innovation Hall

Speaker:

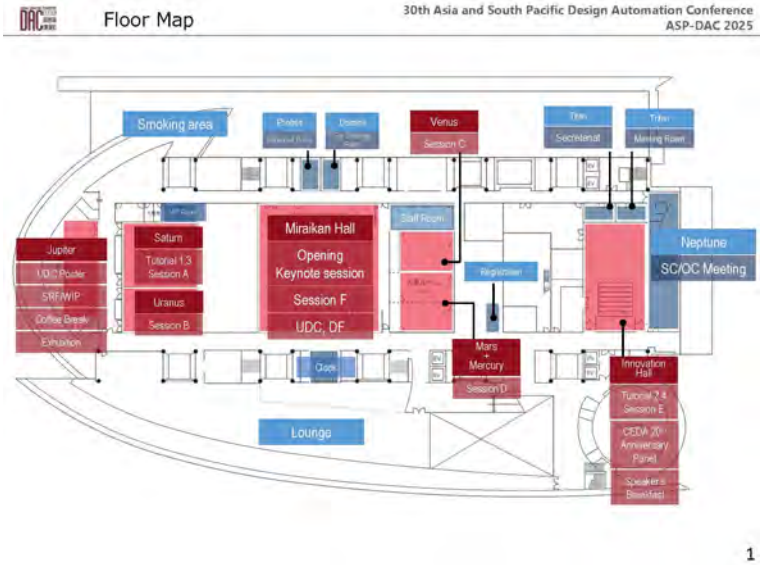
Yiyu Shi (University of Notre Dame)

Room Assignment

Room Assignment

Location	Event
Lobby	Registration and Information Desk
Cloak	Cloak
Miraikan Hall	Opening, Keynotes I,II,III, ASP-DAC 30th Anniversary, University LSI Desing Contest (UDC), Designers' Forum (DF), and Session F
Room Jupiter	UDC Poster, ACM SIGDA Student Research Forum / WIP Poster, Coffee Break, and Supporter's Exhibition
Room Saturn	Session A and Tutorials 1 & 3
Room Uranus	Session B
Room Venus	Session C
Room Mars	Session D
Room Mercury	Session D
Innovation Hall	Session E, Tutorials 2 & 4, CEDA 20th Anniversary Panel, and Speaker's Breakfast
Room Phobos	Rehearsal Room
Room Deimos	File Checking Room
Room Neptune	SC/OC Meeting Room
Hilton Tokyo Odaiba, Room Pegasus (1F)	Banquet

Floor Map of Miraikan 7F:



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Area Map for Miraikan:

Tutorials

ASP-DAC 2025 offers attendees a set of three-hour intense introductions to specific topics. If you register for the conference, you have the option to select two out of the four topics. T2 is a session with hands-on training.

	Monday, January 20	
9:30	Room Saturn	Innovation Hall
12:30	**Tutorial-1:** Automation of Standard Cell Layout Generation and Design-Technology Co-optimization	**Tutorial-2:** AHS: An EDA toolbox for Agile Chip Front-end Design
14:30	Lunch Break	
17:30	**Tutorial-3:** Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification	**Tutorial-4:** Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Tutorial-1 Monday, January 20, 9:30-12:30@Room Saturn

Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

Speaker:

Taewhan Kim (Seoul National University)

Abstract:

As the technology advances, the design rules to be considered in standard cell layout generation become much complex and the count increases very rapidly. Moreover, at the advanced nodes, it becomes much slow or very difficult to achieve the objective i.e., to deliver or find the best-yield target node design rules while ensuring PPA-excellent target chip implementation. This is the reason why, from the EDA perspective, the need for automatic cell layout generation is inevitable at the advanced nodes, and design and technology co-optimization is a key enabling technique to achieve the chip PPA objective.

In this respect, this tutorial covers EDA research area regarding two topics: (1) automation of standard cell layout generation and (2) methodologies of design and technology co-optimization utilizing diverse cell layout structures.

For standard cells, starting from the detailed layer-by-layer structure for cell layout synthesis, the complex design rules, the algorithms of cell synthesis including transistor placement and in-cell routing, and existing cell generation tools developed so far in academia with comparison of their distinct features and pros/cons will be covered. In addition, new EDA challenge of cell generation for next generation of BEOL and FEOL technologies will be discussed. For DTCO, starting from the DTCO concept utilizing standard cells, noticeable DTCO works focusing on, for target chip PPA improvement, multi-bit flip-flop cells, cells with pin inaccessibility, and cells with metal and gate poly misalignment will be covered.

Tutorial-2 Monday, January 20, 9:30-12:30@Innovation Hall

AHS: An EDA toolbox for Agile Chip Front-end Design

Speakers:

Yun (Eric) Liang (Peking University), **Youwei Xiao** (Peking University), **Ruifan Xu** (Peking University)

Abstract:

Compared to software design, hardware design is more expensive and time-consuming. This is partly because software community has developed a rich set of modern tools to help software programmers to get projects started and iterated easily and quickly. However, the tools are seriously antiquated and lacking for hardware design. Modern digital chips are still designed manually using hardware description language such as Verilog or VHDL, which requires low-level and tedious programming, debugging, and tuning. In this tutorial, we will introduce AHS: An EDA toolbox for Agile Chip Front-end Design, which includes various EDA tools for both chip design and verification.

Tutorial-3 Monday, January 20, 14:30 - 16:30@Room Saturn

Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

Speaker:
Prashant Seetharaman (Siemens Digital Industries Software)

Abstract:

As System-on-Chip (SoC) designs continue to grow in complexity and memory density, ensuring the reliability and testability of embedded memories becomes increasingly critical. This tutorial presents an in-depth exploration of Memory Built-In Self-Test (MBIST), a powerful methodology for testing and diagnosing memory faults in modern SoC designs. We will discuss the fundamentals of MBIST, advanced implementation techniques, and emerging trends in the field. The tutorial also covers key aspects of MBIST, including architecture, test algorithm selection, integration in the SoC design flow, and strategies for optimizing test coverage and reducing test time. Through theoretical analysis and practical examples, we will demonstrate how MBIST addresses the challenges of testing high-density memories in complex SoCs, balancing test quality, silicon area overhead, and test time to achieve optimal results in real-world scenarios. Additionally, we explore the application of MBIST to emerging memory technologies encompassing non-volatile memories and resistive RAMs. Finally, we will discuss future directions in memory testing, including the use of machine learning and artificial intelligence techniques.

Tutorial-4 Monday, January 20, 14:30 - 17:30@Innovation Hall

Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Speaker:
Yiyu Shi (University of Notre Dame)

Abstract:

Scaling laws guide the design of large language models (LLMs), assuming unlimited computing resources, but this is impractical for deploying personalized LLMs on resource-constrained edge devices. Critical questions arise regarding trade-offs between design factors such as learning methods, data volume, model size, compression techniques, and training time and their impact on efficiency and accuracy. This tutorial provides comprehensive guidelines for deploying LLMs on constrained devices and explores how advanced hardware architectures like Compute-in-Memory (CiM) can aid this process. Attendees will learn to make informed decisions on key topics like choosing between compressed vs. uncompressed LLMs, selecting appropriate personalization techniques, and optimizing training time under resource limitations.

Keynote Addresses

Keynote I

Tuesday, January 21, 9:00-9:45

"Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry"

Dr. Kazunari Ishimaru
(Rapidus Corporation)

As the semiconductor industry faces mounting pressure to meet both rising demand and sustainability challenges, the need for innovative design and effective collaboration with foundries has never been more critical.

The lead time from design to productization is becoming longer with each transition to the next generation, which is particularly critical in the rapidly growing AI market, where time to market is crucial. Additionally, traditional DFM (Design for Manufacturability) to address the increasingly complex device structures and manufacturing processes is also becoming more complicated, leading to longer design periods.

As a foundry, it is essential to provide feedback to the design space from a manufacturing perspective, and the realization of MFD (Manufacturing for Design) will become essential in the future. The DMCO (Design-Manufacturing Co-Optimization) proposed by Rapidus is a method to solve this issue, and collaboration with customers and ecosystem partners is crucial. Furthermore, collaborative efforts with foundries enable adopting sustainable production practices, such as reducing energy consumption, minimizing waste, and ensuring supply chain transparency.

The importance of integrating design innovation and foundry collaboration to build a semiconductor industry that is resilient, responsible, and aligned with global sustainability objectives.

Keynote II

Wednesday, January 22, 9:00-9:45

"Compilation and Architecture Optimization for Quantum Computing"

Prof. Jason Cong
(UCLA)

The rapid progress in quantum computing (QC) technologies in the past decade led to QC processors with hundreds to thousands of qubits. As a result, efficient compilation flow become both important and challenging. In this talk, I focus on the critical step of the compilation called quantum layout synthesis (QLS), which determines the space and time of computation of a quantum circuit. I first show that the existing QLS solutions, surprisingly, are far away from optimal, despite the effort of the research community for more than a decade. Then, I present recent progress on scalable and highly optimized QLS solutions for both QC processors with fixed connectivity, such as those based on the superconducting technology, and those with programmable connectivity, such as those using neutral atom arrays. Finally, I shall discuss how such optimized QLS tools can be used to guide QC processor architecture optimization, e.g. in determining the number of movable lasers and the configuration of storage vs computing zones for neutral atom arrays.

Keynote III

Thursday, January 23, 9:00-9:45

"In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects"

Dr. Abu Sebastian
(IBM Research Europe – Zurich)

Analog in-memory computing (AIMC), where synaptic weights are stored in nanoscale non-volatile memory elements and computations are carried out in the analogue or mixed-signal domain, represents a promising approach for developing the next generation of deep learning accelerators. In the first part of the presentation, I will explore the current advancements in this area, focusing on a 64-core AIMC chip built using 14nm CMOS technology with integrated phase-change memory. This chip achieves classification accuracy comparable to floating-point operations and demonstrates seamless integration of analogue and digital processing units. This work lays the foundation for a heterogeneous mixed-signal architecture. In the second part, I will cover ongoing efforts to design the next generation of AIMC chips for deep learning inference, targeting both edge and cloud applications.

University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The contest's purpose is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss innovative and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processor, (3) Microprocessors, and (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 18 designs from four countries/areas and selected 17 designs. The selected designs will be discussed in Session 2F on January 21 with short presentations and an interactive poster session. The poster session will start before lunch and continue until the coffee break. The Best Design Award and the Special Feature Award will be presented for two outstanding designs in the opening session. We sincerely acknowledge the other contributions to the contest, too. Our earnest belief is to promote and enhance research and education in LSI design in academic organizations. Please join the University LSI Design Contest and enjoy the stimulating discussions.

Date: Tuesday, January 21, 2025
Place: Tokyo Odaiba Waterfront, Japan

Oral Presentation: Miraikan Hall (13:15 - 15:20)
Poster Presentation: Room Jupiter (11:45 - 13:15)

University LSI Design Contest Committee Co-Chairs:

Mahfuzul Islam
(Institute of Science Tokyo)

Shinya Takamaeda-Yamazaki
(The University of Tokyo)

Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions for real product developments among LSI designers and EDA academia/developers. The topics discussed in this forum include Quantum Computing, Advanced Sensor Technologies and Sensor Fusion, Extending the Limits of Classical Computers using Emerging Device and Circuit Technology, and Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence.

Oral Sessions: (5F) Quantum Computing
(6F) Advanced Sensor Technologies and Sensor Fusion
(8F) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology
(9F) Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence

Session 5F (January 22, 13:15 - 14:30)
[Quantum Computing]

This session will highlight the current and future directions in quantum computing hardware, control systems, and software architecture. The first presentation will delve into the implementation gap between traditional digital logic and quantum circuits, emphasizing the need for cross-disciplinary collaboration between physicists and conventional circuit designers. This gap highlights the unique challenges in developing circuits operating analog, passive systems where software defines quantum gates. The second presentation will discuss the development of a scalable controller for approximately 100 superconducting qubits. The speaker will explain how advanced hardware and software optimizations have facilitated complex quantum operations and will outline future goals to expand this controller's capacity, making it compatible with various qubit types and pushing toward real-world quantum applications. In the third presentation, the speaker will introduce their work on quantum algorithms and software, specifically for chemistry and Computer-Aided Engineering (CAE). By introducing the QURI SDK, a software platform designed for Fault-Tolerant Quantum Computing (FTQC), the speaker will demonstrate how multi-layered quantum software development enables practical quantum applications.

Session 6F (January 22, 15:40 -16:55)
[Advanced Sensor Technologies and Sensor Fusion]

This session showcases various sensor technologies, including human sensing and image sensors with 2D/3D or 2D/event sensing capabilities. The first presentation introduces radar-based human sensing technology, including posture detection, static human localization, and vital measurement for healthcare and smart home applications. The second talk will present a time-gated SPAD image sensor with 2D interactive gating network for alignment-free sensor fusion, which has a background suppression technique. The third talk will present an RGB Hybrid Event-based Vision Sensor, in which RGB pixels and event pixels are implemented on the same sensor showing the potential for realizing neural network-based deblurring applications.

Session 8F (January 23, 13:15 -14:40)
[Extending the Limits of Classical Computers using Emerging Device and Circuit Technology]

With the rapid development of quantum computers, conventional computers are referred to as classical computers. The demand for improved performance of classical computers will continue due to their potential for industrial use and the fact that quantum computers themselves will require classical computers to operate. The ideal performance improvements based on Moore's Law are already becoming difficult to achieve, and we must seek emerging approaches to both circuits and devices. In this session, three talks will be given on circuit and device technologies for improving the performance of classical computers. The first talk will present a circuit technology that improves the flexibility of domain-specific architectures. The second talk will present a device technology that aims to integrate optical and electrical information processing. The third talk will present a superconducting device aimed at energy-efficient computing.

Session 9F (January 23, 15:20 -16:35)
[Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence]

This session introduces recent design approaches using open source and artificial intelligence (AI) to ease the design of analog integrated circuits (ICs). The first presentation introduces how to design analog ICs in the online community based on experiences from Chipathon 2023. The next presentation introduces an open PDK development methodology to develop PDK more quickly and at a lower cost. The final presentation introduces the methods for automatically designing element values for analog ICs using AI.

Designers' Forum Co-Chairs:
Takatsugu Ono (Kyusyu University) **Chihiro Yoshimura** (Hitachi, Ltd.)

ACM SIGDA Student Research Forum at ASP-DAC 2025

The Student Research Forum (SRF) at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for PhD students to present and discuss their dissertations with experts in the design automation community. Starting from 2015, the forum includes both PhD and MS students, offering a great opportunity for the students to establish contacts for their future career. In addition, the forum helps companies and academic institutes to get an overview of the latest research and discover extraordinary candidates for their employment.

Date and Time: 18:00-20:00, January 21th, 2025
Location: Room Jupiter [Food will be served.]

We would like to thank the following committee members for their support and contribution to this forum.

Technical committee:
Muhammad Alfian Aamrizal (UGM)
Daijoon Hyun (Sejong University, Korea)
Heechun Park (Ulsan National Institute of Science and Technology)
Ateet Bhalla (Independent Technology Consultant)
Yanjing Li (University of Chicago)
Taigon Song (Kyungpook National University)

ASP-DAC liaison:
Shinichi Nishizawa (Waseda University)
Masato Inagi (Hiroshima City University)

The sponsors of this forum are ACM SIGDA and Cadence Design Systems, Inc. We would also like to thank ASP-DAC 2025 for supporting this forum.

ACM SIGDA Student Research Forum Chair:

Heechun Park
(Ulsan National Institute of Science and Technology)

ACM SIGDA Student Research Forum Co-Chair:

Yanjing Li
(University of Chicago)

WIP Poster Session at ASP-DAC 2025

In ASP-DAC 2025, we will host a WIP session. Presenters provide poster presentation on their ongoing work, with fresh problems/solutions. WIP content is typically material that may not be mature or complete enough for full paper submission and will not be included in the proceedings. This is an excellent opportunity to present and discuss ongoing research with experts from the design automation community around the world. We strongly encourage presentations at this session from students and young researchers from both of academics and industries.

Date and Time: 18:00-20:00, January 21th, 2025
Location: Room Jupiter

In Cooperation with:
IEEE Council on Electronic Design Automation (CEDA) All Japan Joint Chapter
IEEE Circuits and Systems Society (CASS) Japan Joint Chapter

This session will be held in the same time of the Student Research Forum. This session is free for attendance. Presenters and Participants are not required the registration to ASP-DAC for this session only.

WIP Poster Session Chair:

Makoto Ikeda
(The University of Tokyo)

WIP Poster Session Secretary:

Hiromitsu Awano
(Kyoto University)

Supporter's Exhibition

Supporter's exhibition is held by two companies which support ASP-DAC 2025 and have exhibition booths. The supporter's exhibition is presented at Miraikan 7F Lobby from January 20 through January 23.

Exhibit Hours: **9:00 – 18:00, January 20**
9:45 – 20:00, January 21
9:45 – 18:00, January 22
9:45 – 18:00, January 23
Location: **Miraikan 7F Room Jupiter**

KIOXIA https://www.kioxia.com/en-jp/	KIOXIA Corporation, a world leader in memory solutions, is dedicated to the development, production and sales of flash memory and SSDs. KIOXIA pioneers cutting-edge memory solutions and services that enrich people's lives and expand society's horizons. The company's innovative 3D flash memory technology, BiCS FLASH™, is shaping the future of storage in high density applications including advanced smartphones, PCs, SSDs, automotive and data centers. For more information on KIOXIA, please visit `https://www.kioxia.com`
Solvbest https://www.solvbest.co.jp/	Solvbest, an EDA tools distributor of Empyrean, AnaGlobe etc., provides complete solution for Analog Design, Digital SoC Solution, RF IC Design Solution, Advanced Packaging Design Solution, Complete Solution for Flat Panel Display Design and Foundry EDA Solution, etc. These solutions enable designers to improve design efficiency and complete their designs in less time by optimizing timing, area, power, yield, reliability, aging, etc. to meet design specifications.

Monday, January 20, 2025

T1 Tutorial-1: Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

Time: 9:30 - 12:30, Monday, January 20, 2025

Location: Room Saturn

T1-1 (Time: 9:30 - 12:30)

(Tutorial) Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

*Taewhan Kim (Seoul National Univ., Republic of Korea)

T2 Tutorial-2: AHS: An EDA toolbox for Agile Chip Front-end Design

Time: 9:30 - 12:30, Monday, January 20, 2025

Location: Innovation Hall

T2-1 (Time: 9:30 - 12:30)

(Tutorial) AHS: An EDA toolbox for Agile Chip Front-end Design

Yun (Eric) Liang, Youwei Xiao, Ruifan Xu (Peking Univ., China)

T3 Tutorial-3: Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

Time: 14:30 - 16:30, Monday, January 20, 2025

Location: Room Saturn

T3-1 (Time: 14:30 - 16:30)

(Tutorial) Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

*Prashant Seetharaman (Siemens Digital Industries Software, USA)

T4 Tutorial-4: Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Time: 14:30 - 17:30, Monday, January 20, 2025

Location: Innovation Hall

T4-1 (Time: 14:30 - 17:30)

(Tutorial) Efficient Deployment of Large Language Models on Resource-Constrained Edge Computing Platforms

*Yiyu Shi (Univ. of Notre Dame, USA)

Tuesday, January 21, 2025

1K Opening and Keynote Session I

Time: 8:30 - 9:45, Tuesday, January 21, 2025

Location: Miraikan Hall

Chair: Yuichi Nakamura (NEC, Japan)

1K-1
ASP-DAC 2025 Opening

1K-2
(Keynote Address) Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry
Kazunari Ishimaru (Rapidus, Japan)

1A (T1-1) System-Level Modeling and Design Methodologies

Time: 10:05 - 11:45, Tuesday, January 21, 2025

Location: Room Saturn

Chair: Jing-Jia Liou (National Tsing Hua Univ., Taiwan)

1A-1 (Time: 10:05 - 10:30)

1A-2 (Time: 10:30 - 10:55)

1A-3 (Time: 10:55 - 11:20)

1A-4 (Time: 11:20 - 11:45)

1B (T4.2-1) Tools and Techniques for On-Device AI Deployment

Time: 10:05 - 11:45, Tuesday, January 21, 2025

Location: Room Uranus

Chairs: Jongeun Lee (Ulsan National Inst. of Science and Tech. (UNIST)), Youngsoo Shin (KAIST, Republic of Korea)

1B-1 (Time: 10:05 - 10:30)

1B-2 (Time: 10:30 - 10:55)

1B-3 (Time: 10:55 - 11:20)

Tuesday, January 21, 2025

1C (T8-1) AI and Logic Synthesis - A perfect match?

Time: 10:05 - 11:20, Tuesday, January 21, 2025

Location: Room Venus

Chairs: Christophe Dubach (McGill Univ., Canada), Andrea Costamagna (EPFL, Switzerland)

1D (T3-1) Application-Specific Computing-In-Memory

Time: 10:05 - 11:45, Tuesday, January 21, 2025

Location: Room Mars/Mercury

Chairs: Hiromitsu Awano (Kyoto Univ., Japan), Yiming Chen (Tsinghua Univ., China)

Tuesday, January 21, 2025

1E (SS-1) Machine Learning Based Physical Simulation and Physics-Aware Optimization

Time: 10:05 - 11:45, Tuesday, January 21, 2025

Location: Innovation Hall

Chairs: Wenjian Yu (Tsinghua Univ., China), Yuanqing Cheng (Beihang Univ., China)

1F (SS-CEDA) CEDA/CASS/SSCS Joint session on Silicon Photonics

Time: 10:05 - 11:45, Tuesday, January 21, 2025

Chair: Tsung-Yi Ho (Chinese Univ. of Hong Kong, Hong Kong)

2A (T5-1) Accelerating Vision and Transformer Models

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Room Saturn

Chairs: Quan Chen (Southern Univ. of Science and Tech., China), Sheldon Tan (UC Riverside, USA)

Tuesday, January 21, 2025

2B (T6-1) Shaping the Future of Analog EDA

Time: 13:15 - 14:55, Tuesday, January 21, 2025

Location: Room Uranus

Chairs: Zhou Jin (China Univ. of Petroleum, China), Nobukazu Takai (Kyoto Inst. of Tech.)

2C (T7-1) Approximate and Stochastic Computing

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Room Venus

Chair: Yue Zhang (Beihang Univ., China)

Tuesday, January 21, 2025

2D (T2-1) Next-Generation Embedded Architectures and Tools

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Room Mars/Mercury

Chair: Chao Huang (Univ. of Southampton)

2E (SS-2) Advances in 3D-IC and Ultra-Large-Scale Integration

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Innovation Hall

Chair: Yibo Lin (Peking Univ., China)

Tuesday, January 21, 2025

2F University Design Contest

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Chairs: Mahfuzul Islam (Tokyo Inst. of Tech., Japan), Shinya Takamaeda Yamazaki (Univ. of Tokyo, Japan)

Tuesday, January 21, 2025

3A (SS-3) LLM Acceleration and Specialization for Circuit Design and Edge Applications

Time: 15:40 - 17:20, Tuesday, January 21, 2025

Location: Room Saturn

Chairs: Zheyu Yan (Zhejiang Univ., China), Cheng Zhuo (Zhejiang Univ., China)

3B (T9-1) Timing Analysis and Optimization

Time: 15:40 - 17:45, Tuesday, January 21, 2025

Location: Room Uranus

Chair: Heechun Park (Ulsan National Inst. of Science and Tech., Republic of Korea)

Tuesday, January 21, 2025

3C (T12-1) Side Channel Attacks and Trusted Execution Environment

Time: 15:40 - 17:45, Tuesday, January 21, 2025

Location: Room Venus

Chairs: Qiang Liu (Tianjin Univ., China), Song Chen (Univ. of Science and Tech. of China, China)

Tuesday, January 21, 2025

3D (T3-2) Frameworks and Modeling for Computing-In-Memory

Time: 15:40 - 17:20, Tuesday, January 21, 2025

Location: Room Mars/Mercury

Chairs: Zhou Jin (China Univ. of Petroleum, China), Kentaro Yoshioka (Keio Univ., Japan)

3E (T4.1-1) AI/ML for Circuit Design and Prediction

Time: 15:40 - 17:45, Tuesday, January 21, 2025

Location: Innovation Hall

Chair: Jaeyong Chung (Yonsei Univ., Republic of Korea)

Wednesday, January 22, 2025

2K 30th Anniversary and Keynote Session II

Time: 8:30 - 9:45, Wednesday, January 22, 2025

Location: Miraikan Hall

Chair: Shinji Kimura (Waseda Univ., Japan)

2K-1
30th Anniversary

2K-2
(Keynote Address) Compilation and Architecture Optimization for Quantum Computing
Jason Cong (UCLA, USA)

4A (T4.2-2) Advanced Methods in AI Hardware Co-Design

Time: 10:05 - 11:45, Wednesday, January 22, 2025

Location: Room Saturn

Chairs: Wanyeong Jung (Korea Advanced Inst. of Science and Tech. (KAIST)), Yeseong Kim (DGIST, Republic of Korea)

4B (T1-2) Communication Networks

Time: 10:05 - 11:45, Wednesday, January 22, 2025

Location: Room Uranus

Chair: Jiang Xu (Hong Kong Univ. of Science and Tech. (GZ), Hong Kong)

Wednesday, January 22, 2025

4C (T2-2) Design and Optimization of Emerging Embedded Applications

Time: 10:05 - 11:45, Wednesday, January 22, 2025

Location: Room Venus

Chair: Fang-Jing Wu (National Taiwan Univ., Taiwan)

4D (T11-1) Verification and Testing in Machine Lerning Era

Time: 10:05 - 11:45, Wednesday, January 22, 2025

Location: Room Mars/Mercury

Chair: Michihiro Shintani (Kyoto Inst. of Tech., Japan)

4E (T3-3) Hybrid/Co-Designed Near/In Memory Computing

Time: 10:05 - 11:45, Wednesday, January 22, 2025

Location: Innovation Hall

Chairs: Bokyung Kim (Rutgers Univ., USA), Zhong Sun (Peking Univ., China)

Wednesday, January 22, 2025

4F (SS-4) ML for IC Design and Manufacturing: When Is It Real?

Time: 10:05 - 11:45, Wednesday, January 22, 2025

Chairs: Yibo Lin (Peking Univ., China), Youngsoo Shin (KAIST, Republic of Korea)

1W CEDA 20th Anniversary Panel

Time: 12:00 - 13:00, Wednesday, January 22, 2025

Location: Innovation Hall and more

Organizer: Tsung-Yi Ho (Chinese Univ. of Hong Kong, Hong Kong), Panel Moderator: Yu Wang (Tsinghua Univ., China)

5A (T5-2) Innovations in Deep Learning and Neural Network Acceleration

Time: 13:15 - 15:20, Wednesday, January 22, 2025

Location: Room Saturn

Chair: Shinya Takamaeda Yamazaki (Univ. of Tokyo, Japan)

Wednesday, January 22, 2025

5B (T7-2) Neuromorphic and Emerging Computing Techniques

Time: 13:15 - 15:20, Wednesday, January 22, 2025

Location: Room Uranus

Chair: Georgios Zervakis (Univ. of Patras, Greece)

5C (T9-2) Package and PCB

Time: 13:15 - 14:55, Wednesday, January 22, 2025

Location: Room Venus

Chair: Pei-Yu Lee (Mediatek, Taiwan)

Wednesday, January 22, 2025

5D (T12-2) Logic Locking and Hardware Watermarking

Time: 13:15 - 14:55, Wednesday, January 22, 2025

Location: Room Mars/Mercury

Chairs: Daisuke Fujimoto (NAIST, Japan), Amin Rezaei (California State Univ., Long Beach, USA)

5E (T4.1-2) AI-Driven Innovative Design Methods

Time: 13:15 - 15:20, Wednesday, January 22, 2025

Location: Innovation Hall

Chair: Jaeduk Han (Hanyang Univ., Republic of Korea)

Wednesday, January 22, 2025

5F (DF-1) Quantum Computing

Time: 13:15 - 14:30, Wednesday, January 22, 2025

Organizer: Takatsugu Ono (Kyushu Univ., Japan), Chair: Chihiro Yoshimura (Hitachi, Japan)

6A (SS-5) Beyond Digital: Advancing Design Automation for Physical Computing Systems

Time: 15:40 - 17:20, Wednesday, January 22, 2025

Location: Room Saturn

Chair: Antonino Tumeo (PNNL, USA)

6B (T9-3) Floorplan and Placement

Time: 15:40 - 17:45, Wednesday, January 22, 2025

Location: Room Uranus

Chair: Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan)

Wednesday, January 22, 2025

6C (T13-1) Let's Quantumize: Welcome to the World of Quantum

Time: 15:40 - 16:55, Wednesday, January 22, 2025

Location: Room Venus

Chairs: Chun-Yi Lee (National Taiwan Univ., Taiwan), Ulf Schlichtmann (Tech. Univ. of Munich, Germany)

6D (T10-1) Innovative Techniques for Energy-Efficient and Reliable Hardware Systems

Time: 15:40 - 17:45, Wednesday, January 22, 2025

Location: Room Mars/Mercury

Chairs: Zhiyao Xie (Hong Kong Univ. of Science and Tech., Hong Kong), Qi Sun (Zhejiang Univ., China), Shanshi Huang (Hong Kong Univ. of Science and Tech. (GZ), China)

Wednesday, January 22, 2025

6E (T4.1-3) Leveraging Large Language Models in Hardware Design

Time: 15:40 - 17:45, Wednesday, January 22, 2025

Location: Innovation Hall

Chair: Cong Hao (Georgia Tech, USA)

6F (DF-2) Advanced Sensor Technologies and Sensor Fusion

Time: 15:40 - 16:55, Wednesday, January 22, 2025

Organizer: Takashi Moue (Sony Semiconductor Solutions, Japan), Chair: Koichiro Yamashita (Fujitsu, Japan)

Wednesday, January 22, 2025

6F-3 (Time: 16:30 - 16:55)

(Designers' Forum) 1.22μm-pixel Back-illuminated Stacked RGB Hybrid Event-based Vision Sensor

*Kazutoshi Kodama, Yusuke Sato, Yuhi Yorikado, Kyoji Mizoguchi, Takahiro Miyazaki, Masahiro Tsukamoto, Yoshihisa Matoba, Hirotaka Shinozaki, Atsumi Niwa, Tetsuji Yamaguchi (Sony Semiconductor Solutions, Japan), Christian Braendli (Sony Advanced Visual Sensing, Switzerland), Hayato Wakabayashi, Yusuke Oike (Sony Semiconductor Solutions, Japan)

Thursday, January 23, 2025

3K Keynote Session III

Time: 9:00 - 9:45, Thursday, January 23, 2025

Location: Miraikan Hall

Chair: Atsushi Takahashi (Institute of Science Tokyo, Japan)

3K-1

(Keynote Address) In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects
Abu Sebastian (IBM Research Europe - Zurich, Switzerland)

7A (T1-3) Accelerator Design Methodologies

Time: 10:05 - 11:45, Thursday, January 23, 2025

Location: Room Saturn

Chair: Yaoyao Ye (Shanghai Jiao Tong Univ., China)

7A-1 (Time: 10:05 - 10:30)

7A-2 (Time: 10:30 - 10:55)

7A-3 (Time: 10:55 - 11:20)

7A-4 (Time: 11:20 - 11:45)

7B (T5-3) Advanced Architectures for Scientific and Edge Computing

Time: 10:05 - 11:45, Thursday, January 23, 2025

Location: Room Uranus

Chair: Hao Yu (SUSTech, China)

7B-1 (Time: 10:05 - 10:30)

7B-2 (Time: 10:30 - 10:55)

7B-3 (Time: 10:55 - 11:20)

7B-4 (Time: 11:20 - 11:45)

Thursday, January 23, 2025

7C (T6-2) The Science of Light: the New Advancement of Photonic Computing

Time: 10:05 - 11:45, Thursday, January 23, 2025

Location: Room Venus

Chairs: Ryosuke Matsuo (Univ. of Tokyo, Japan), Yuanqing Cheng (Beihang Univ., China)

7C-1 (Time: 10:05 - 10:30)

7C-2 (Time: 10:30 - 10:55)

7C-3 (Time: 10:55 - 11:20)

7C-4 (Time: 11:20 - 11:45)

7D (T8-2) From Math to Circuits

Time: 10:05 - 11:20, Thursday, January 23, 2025

Location: Room Mars/Mercury

Chairs: Oliver Keszöcze (Tech. Univ. of Denmark, Denmark), Yukio Miyasaka (UC Berkeley, USA)

7D-1 (Time: 10:05 - 10:30)

7D-2 (Time: 10:30 - 10:55)

7D-3 (Time: 10:55 - 11:20)

7E (T4.2-3) Innovative Techniques in AI Model Optimization and Training

Time: 10:05 - 11:20, Thursday, January 23, 2025

Location: Innovation Hall

Chairs: Dongsuk Jeon (Seoul National Univ., Republic of Korea), Ik-Joon Chang (Kyung Hee Univ.)

7E-1 (Time: 10:05 - 10:30)

7E-2 (Time: 10:30 - 10:55)

Thursday, January 23, 2025

7E-3 (Time: 10:55 - 11:20)

7F (SS-6) Rapidus' Initiatives to Half Semiconductor Development Time

Time: 10:05 - 11:20, Thursday, January 23, 2025

Chair: Koki Tsurusaki (Rapidus, Japan)

7F-1 (Time: 10:05 - 10:30)

7F-2 (Time: 10:30 - 10:55)

7F-3 (Time: 10:55 - 11:20)

8A (T1-4) System Level Modelling & Optimization

Time: 13:15 - 14:55, Thursday, January 23, 2025

Location: Room Saturn

Chair: Zhe Lin (Sun Yat-sen Univ., China)

8A-1 (Time: 13:15 - 13:40)

8A-2 (Time: 13:40 - 14:05)

8A-3 (Time: 14:05 - 14:30)

8A-4 (Time: 14:30 - 14:55)

8B (T5-4) Emerging Trends in Reconfigurable and Compute-in-Memory

Time: 13:15 - 14:55, Thursday, January 23, 2025

Location: Room Uranus

Chair: Guohao Dai (Shanghai Jiao Tong Univ., China)

8B-1 (Time: 13:15 - 13:40)

Thursday, January 23, 2025

8B-2 (Time: 13:40 - 14:05)

8B-3 (Time: 14:05 - 14:30)

8B-4 (Time: 14:30 - 14:55)

8C (T3-4) Adaptive and Flexible Memory Architecture

Time: 13:15 - 14:55, Thursday, January 23, 2025

Location: Room Venus

Chair: Chao Wu (Nanjing Univ. of Science and Tech., China)

8C-1 (Time: 13:15 - 13:40)

8C-2 (Time: 13:40 - 14:05)

8C-3 (Time: 14:05 - 14:30)

8C-4 (Time: 14:30 - 14:55)

8D (T9-4) Reliability in Physical Design

Time: 13:15 - 14:55, Thursday, January 23, 2025

Location: Room Mars/Mercury

Chair: Wenjian Yu (Tsinghua Univ., China)

8D-1 (Time: 13:15 - 13:40)

8D-2 (Time: 13:40 - 14:05)

8D-3 (Time: 14:05 - 14:30)

Thursday, January 23, 2025

8D-4 (Time: 14:30 - 14:55)

8E (SS-7) Hardware Authenticity towards a Trustworthy Society

Time: 13:15 - 14:55, Thursday, January 23, 2025

Location: Innovation Hall

Chairs: Jun Shiomi (Osaka Univ., Japan), Michihiro Shintani (Kyoto Inst. of Tech., Japan)

8E-1 (Time: 13:15 - 13:40)

8E-2 (Time: 13:40 - 14:05)

8E-3 (Time: 14:05 - 14:30)

8E-4 (Time: 14:30 - 14:55)

8F (DF-3) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology

Time: 13:15 - 14:30, Thursday, January 23, 2025

Organizer: Chihiro Yoshimura (Hitachi, Japan), Chair: Takatsugu Ono (Kyushu Univ., Japan)

8F-1 (Time: 13:15 - 13:40)

(Designers' Forum) Amorphica: Fully Connected Metamorphic Annealing Processor with Programmable Optimization Strategy

*Kazushi Kawamura (Institute of Science Tokyo, Japan), Jaehoon Yu (Samsung Advanced Inst. of Tech., Republic of Korea), Daiki Okonogi, Satoru Jimbo, Genta Inoue, Akira Hyodo (Institute of Science Tokyo, Japan), Ángel López García-Arias (NTT, Japan), Kota Ando, Bruno Hideki Fukushima-Kimura (Hokkaido Univ., Japan), Ryota Yasudo (Kyoto Univ., Japan), Thiem Van Chu, Masato Motomura (Institute of Science Tokyo, Japan)

8F-2 (Time: 13:40 - 14:05)

(Designers' Forum) Nanophotonic Devices toward Opto-Electronic Accelerator

*Akihiko Shinya (NTT, Japan)

8F-3 (Time: 14:05 - 14:30)

(Designers' Forum) Highly Energy-Efficient Processing by Controlling Flexibility of Information Carrier using Superconductor Half-Flux Quantum Logic

*Masamitsu Tanaka (Nagoya Univ., Japan)

Thursday, January 23, 2025

9A (T12-3) Homomorphic Encryption and Cloud Security

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Room Saturn

Chairs: Junghee Lee (Korea Univ., Republic of Korea), Yiran Chen (Duke Univ., USA)

9A-1 (Time: 15:20 - 15:45)

9A-2 (Time: 15:45 - 16:10)

9A-3 (Time: 16:10 - 16:35)

9A-4 (Time: 16:35 - 17:00)

9A-5 (Time: 17:00 - 17:25)

9B (T11-2) Advanced Modeling, Simulation, and Verification

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Room Uranus

Chair: Yutaka Masuda (Nagoya Univ., Japan)

9B-1 (Time: 15:20 - 15:45)

9B-2 (Time: 15:45 - 16:10)

9B-3 (Time: 16:10 - 16:35)

9B-4 (Time: 16:35 - 17:00)

Thursday, January 23, 2025

9B-5 (Time: 17:00 - 17:25)

9C (T13-2) Carbon, Light, Fluids: Emerging Technologies

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Room Venus

Chairs: Krishnendu Chakrabarty (Arizona State Univ., USA), Yangdi Lyu (HKUST (GZ), China)

9C-1 (Time: 15:20 - 15:45)

9C-2 (Time: 15:45 - 16:10)

9C-3 (Time: 16:10 - 16:35)

9C-4 (Time: 16:35 - 17:00)

9C-5 (Time: 17:00 - 17:25)

9D (T10-2) Advanced Techniques for Power Optimization and IR Prediction

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Room Mars/Mercury

Chairs: Bei Yu (Chinese Univ. of Hong Kong, Hong Kong), Yu-Guang Chen (National Central Univ., Taiwan), Hongce Zhang (Hong Kong Univ. of Science and Tech. (GZ), China)

9D-1 (Time: 15:20 - 15:45)

9D-2 (Time: 15:45 - 16:10)

9D-3 (Time: 16:10 - 16:35)

9D-4 (Time: 16:35 - 17:00)

Thursday, January 23, 2025

9D-5 (Time: 17:00 - 17:25)

Towards Functional Safety of Neural Network Hardware Accelerators: Concurrent Out-of-Distribution Detection in Hardware Using Power Side-Channel Analysis 1413

*Vincent Meyers (Karlsruhe Inst. of Tech., Germany), Michael Hefenbrock (RevoAI GmbH, Germany), Mahboobe Sadeghipourrudsari, Dennis Gnad, Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany)

9E (SS-8) Innovations and Challenges on Cryo-CMOS Devices, Circuits and Design Platforms

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Innovation Hall

Chairs: Chika Tanaka (KIOXIA/Kyoto Inst. of Tech., Japan), Nobuyuki Momo (KIOXIA, Japan)

9E-1 (Time: 15:20 - 15:45)

(Invited Paper) Physics-based Modeling to Extend a MOSFET Compact Model for Cryogenic Operation 1420

*Dondee Navarro (KIOXIA/Kyoto Inst. of Tech., Japan), Shin Taniguchi (Kyoto Inst. of Tech., Japan), Chika Tanaka (KIOXIA/Kyoto Inst. of Tech., Japan), Kazutoshi Kobayashi (Kyoto Inst. of Tech., Japan), Takashi Sato (Kyoto Univ., Japan), Michihiro Shintani (Kyoto Inst. of Tech., Japan)

9E-2 (Time: 15:45 - 16:10)

(Invited Paper) Cryo-Compact Modeling Based on Sparse Gaussian Process 1426

*Tetsuro Iwasaki (Kyoto Inst. of Tech., Japan), Takashi Sato (Kyoto Univ., Japan), Michihiro Shintani (Kyoto Inst. of Tech., Japan)

9E-3 (Time: 16:10 - 16:35)

(Invited Paper) Re-Consideration of Correlation Between Interface States and Bulk Traps Using Cryogenic Measurement ... 1432

*Yuichiro Mitani, Tatsuya Suzuki, Yohei Miyaki (Tokyo City Univ., Japan)

9E-4 (Time: 16:35 - 17:00)

(Invited Paper) Random Telegraph Noise Observed on 65-nm Bulk pMOS Transistors at 3.8K 1438

*Takuma Kawakami, Takashi Sato, Hiromitsu Awano (Kyoto Univ., Japan)

9E-5 (Time: 17:00 - 17:25)

(Invited Paper) Cryo-CMOS Analog Circuits for Spin Qubit Control 1444

*Takuji Miki (Kobe Univ., Japan)

9F (DF-4) Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence

Time: 15:20 - 16:35, Thursday, January 23, 2025

Organizer: Hiroyuki Uzawa (NTT, Japan), Chair: Takeshi Kuboki (Kumamoto Univ., Japan)

9F-1 (Time: 15:20 - 15:45)

(Designers' Forum) A Challenge to Tape-Out in Open-Source Era

*Akira Tsuchiya (Univ. of Shiga Prefecture, Japan)

9F-2 (Time: 15:45 - 16:10)

(Designers' Forum) Analog Design Democratization for Small Volume LSI Fabrication

*Seijiro Moriyama (Anagix, Japan), Shingo Ura, Tadaaki Tsuchiya (Logic Research, Japan)

9F-3 (Time: 16:10 - 16:35)

(Designers' Forum) Automatic Design of an Analog Integrated Circuits using AI

*Nobukazu Takai (Kyoto Inst. of Tech., Japan)

Information

Proceedings:
ASP-DAC 2025 will be providing an authority to access the download site for the conference proceedings. Conference registration in any of the categories will include it. The site will be open on Jan. 20, 2025. Please note that neither CD-ROM nor USB memory are provided.

Banquet:
Conference in-person registrants are invited to attend a banquet to be held on January 22, 2025. The banquet will be held from 18:30 to 20:30 at the Hilton Tokyo Odaiba 1F "Room Pegasus". Regular Member and Non-member Conference in-person registrants receive a ticket to the banquet when they register at the conference.

Free Water:
The conference venue (Miraikan) has water dispensers, so that you can drink water freely. We hope you to enjoy Japanese pure water.

Free WiFi:
Free WiFi internet service is also provided. Instruction how to connect to WiFi is put on the wall in the venue.

Free Bus Tour:
Tokyo Convention & Visitors Bureau is offering complimentary programs specially tailored to provide overseas registered participants with various experiences of Tokyo and its vicinity; from nature and culture to other attractions. Please ask Tokyo Convention & Visitors Bureau at the registration desk for more details on the tour.

Insurance:
The organizer cannot accept responsibility for accidents that might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:
The temperature in Tokyo Odaiba Waterfront during the period of the Conference ranges between 3 degrees Celsius and 10 degrees Celsius.

Currency Exchange:
Only Japanese Yen (JPY, ¥) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Tipping:
In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:
Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.
*Eastern Japan :**Tokyo**, Yokohama, Tohoku, Hokkaido
**Western Japan :Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:
The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Prayer Room:
There is a prayer room in the conference venue (5F of Miraikan). Please feel free to contact the registration desk if you would like to use it.

Nursing Room:
There is a nursing room in the conference venue (5F of Miraikan). Please feel free to contact the registration desk if you would like to use it.

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Invitation to ASP-DAC 2026

On behalf of the Organizing Committee, it is our great pleasure and honor to invite you to the 31st ASP-DAC, to be held in the vibrant city of Hong Kong from January 19-22, 2026.

Hong Kong, known as "Asia's World City," is a dynamic metropolis where East meets West, offering a unique mix of tradition, innovation, and breathtaking scenery. With world-class infrastructure, state-of-the-art conference facilities, and unmatched hospitality, Hong Kong is the perfect destination for this prestigious event.

The conference will be held at the **Hong Kong Disneyland Hotel**, a venue that seamlessly combines sophistication, modern amenities, and the enchanting charm of Disney. Conveniently located just a 15-minute drive from Hong Kong International Airport, the hotel is easily accessible and well-connected through an efficient public transportation network, ensuring a hassle-free journey for all attendees.

Beyond the conference, we encourage you to explore Hong Kong's diverse attractions. From the bustling streets of Central and the shopping paradise of Tsim Sha Tsui to the tranquil beauty of Victoria Harbour and the panoramic views from Victoria Peak, there's something for everyone. Don't miss the chance to enjoy Hong Kong's world-famous culinary scene, which spans everything from Michelin-starred restaurants to authentic local street food.

ASP-DAC 2026 will provide an excellent platform for exchanging ideas and advancing technologies in electronic design automation and embedded systems. Your active participation and submissions are key to shaping an outstanding technical program and fostering meaningful collaborations.

We look forward to welcoming you to Hong Kong, where innovation meets inspiration, and tradition blends seamlessly with modernity. Let's make ASP-DAC 2026 a truly memorable event in this remarkable city!

Tsung-Yi Ho
General Chair, ASP-DAC 2026