

FINAL PROGRAM

Date: January 20-23, 2025 Place: Miraikan 7F The National Museum of Emerging Science and Innovation



http://www.aspdac.com/

ASP-DAC 2025

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Welcome to ASP-DAC 2025

On behalf of the Organizing Committee, I would like to invite all the engineers on the LSI design and design automation fields to the 30th Asia and South Pacific Design Automation Conference (ASP-DAC 2025). We are very happy to celebrate the 30th anniversary of ASP-DAC. I want to thank all who have helped to make ASP-DAC possible for 30 years, and many thanks to all successive SC and OC members, TPC members, contributors and participants.

ASP-DAC is a high-quality and premium conference on Electronic Design Automation (EDA) like other sister conferences such as Design Automation Conference (DAC), Design, Automation & Test in Europe (DATE), International Conference on Computer Aided Design (ICCAD), and Embedded Systems Week (ESWEEK). ASP-DAC started in 1995 and has continuously offered opportunities to learn about the advancements on LSI design and design automation fields, as well as to communicate with each other for researchers and designers around Asia and South Pacific regions.

We have 3 keynotes to share the latest trends in this area, message to design engineers from foundry, CAD for quantum circuits and in-memory computing for AI:

- 1. "Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry", by Dr. Kazunari Ishimaru, Rapidus.
- 2. "Compilation and Architecture Optimization for Quantum Computing", by Prof. Jason Cong, UCLA.
- 3. "In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects", by Dr. Abu Sebastian, IBM Research Europe Zurich

We believe everyone will be very satisfied with these valuable keynote talks.

ASP-DAC 2025 includes Technical Sessions, Special Sessions, Keynotes, Designers' Forum, University Design Contest, Tutorial, and social events. ASP-DAC 2025 received 537 submissions from all over the world. Based on rigorous and thorough reviews and a face-to-face meeting by the Technical Program Committee, 168 papers have been accepted and 39 technical sessions have been organized. Nine Special Sessions have also been organized based on invited talks by the Technical Program Committee.

The Designers' Forum is a unique program that will share design experiences and solutions of actual product designs of the industry. The topics discussed in this forum include Quantum Computing, Advanced Sensor Technologies and Sensor Fusion, Extending the Limits of Classical Computers Using Emerging Device and Circuit Technology, and Integrated Circuit Design Methodologies Using Open Source and Artificial Intelligence. The University Design Contest is also an important annual event of ASP-DAC where 17 high-quality designs, all including actual silicon proof, were selected for presentation with Q&A at poster. Furthermore, at WIP (Work In Progress) poster session, you can present and discuss ongoing research with experts from the design automation community around the world.

Four tutorials have been arranged on January 20th. Each tutorial has a 3 hour presentation. The topics given in Tutorial includes Agile design methodologies and LLM on the edge. In this year you can attend the tutorial without additional tutorial fee. These tutorials will help you gain the latest knowledge about design area.

ASP-DAC 2025 offers you an ideal opportunity to touch the recent technologies and the future directions of the LSI design and design automation fields. So please do not miss ASP-DAC 2025 conference and enjoy Japan as well. Finally, we would like to express our sincere appreciation to those who have contributed to ASP-DAC 2025, including authors, speakers, reviewers, session organizers, session chairs, sponsors, supporters, and committee members.

> Yuichi Nakamura General Chair, ASP-DAC 2025

Message from the Technical Program Committee

Yu Wang

Takashi Sato

Tsung-Yi Ho

On behalf of the Technical Program Committee (TPC), it is our tremendous pleasure to welcome you to the 30th Asia and South Pacific Design Automation Conference (ASP-DAC) 2025, scheduled from January 20 to 23, 2025, at Tokyo Odaiba Miraikan, Japan.

This year, the call for papers of ASP-DAC 2025 employed a two-step procedure, where each submission first registered its abstract and subsequently submitted the full manuscript. We received total 587 abstracts, and of those registered abstracts, we re-

ceived 537 full manuscripts from 29 counties/regions. The number of submissions reaches a record high, reflecting the thriving development of our field. The highest submissions came from the Asia region, followed by North America and Europe. In addition, China and USA contributed nearly 51% of the total submission. To better reflect the submission trend in recent years, we split the design methods with & for Artificial Intelligence (AI) track into two dedicated tracks, "Tools and Design Methods with AI" and "Tools and Design Methods for AI." In addition to continued strong submissions in fundamental EDA topics such as physical design and timing analysis, system-level modeling and design methodology, design for manufacturability/reliability, etc., we received substantial submissions and support in the area of AI hardware systems and architectures. We have also seen a significant increase in new computing paradigms such as near/in memory computing, approximate and bio-inspired computing, and quantum computing. Meanwhile, hardware and embedded security continued to be a strong track as well. These submission trends are strong evidence that ASP-DAC is actively reflecting and correlating with the state-of-the-art research in both academia and industry. We organized the Technical Program Committee (TPC) with 144 professionals who are leading experts in EDA, IC design, embedded system design, memory architectures, hardware security, emerging technologies & applications, AI/ML systems, and formed 14 subcommittees. The paper selection process ensured fairness through a rigorous double-blind review process with tight control of conflicts of interest. We held a face-toface and partially hybrid TPC meeting at Marco Polo Hong Kong Hotel, Hong Kong SAR, China on August 30, 2024. Out of the 537 submissions, 168 high-quality regular papers were selected, representing a very competitive acceptance rate of 31%, further demonstrating that ASP-DAC strives to be a premier conference with technical strengths.

The complete conference program consists of the regular papers, keynote speeches, as well as strong set of special sessions, designers' forums, and design contest sessions. We have tutorials on the first day of the conference, with regular programs compiled into three-day, six parallel sessions. The keynotes are held every morning to kick off the technical sessions. Among the accepted regular papers, 13 were nominated from sub-committees for the Best Paper Award. These best paper candidates went through a thorough evaluation process by the Best Paper Award Committee which is chaired by Vice Technical Program Chair Prof. Takashi Sato, and finally two Best Papers were selected. In addition, Prof. Takashi Sato also chaired the 10-year Retrospective Most Influential Paper selection committee and selected one from papers published in the proceedings of the 20th ASP-DAC conference in 2015.

The exciting and stimulating technical program of ASP-DAC 2025 is the outcome of the hard work and efforts from the authors, reviewers, invited speakers, and TPC members. We would like to sincerely thank all of them. Special thanks go to the TPC Secretaries, Zhenhua Zhu and Jun Shiomi, the conference secretaries, Yuki Kobayashi, Jun Shiomi, and Yukihide Kohira, the publication chairs, Kohei Miyase, Shinobu Nagayama, and Tetsuya Iizuka, and web publicity chairs, Junichiro Kadomoto and Yutaka Masuda, for their extraordinary support. Additionally, we thank Satoshi Taoka for his support in the TPC and review management system. Last but not least, the deepest thanks go to the entire Organizing Committee for their excellent efforts in organizing and hosting a great conference.

We hope you all enjoy the ASP-DAC 2025 technical program and we'll meet you all in Tokyo Japan.

Yu Wang TPC Chair, ASP-DAC 2025

Takashi Sato TPC Vice Chair Tsung-Yi Ho TPC Vice Chair

Session Schedule

Monday, January 20, 2025

Room Saturn	Innovation Hall
T1 Tutorial-1: Automation of Standard Cell Layout	T2 Tutorial-2: AHS: An EDA toolbox for Agile Chip
Generation and Design-Technology Co-optimization	Front-end Design
9:30 - 12:30	9:30 - 12:30
T3 Tutorial-3: Memory Built-In Self-Test (MBIST):	T4 Tutorial-4: Efficient Deployment of Large Language
Advanced Techniques for SoC Design and Verification	Models on Resource Constrained Edge Computing
14:30 - 16:30	Platforms
	14:30 - 17:30

Tuesday, January 21, 2025

Room Saturn	Room Uranus	Room Venus	Room Mars/Mercury	Innovation Hall	Miraikan Hall	
	Mars/Mercury 1K (Miraikan Hall) Opening and Keynote Session I 8:30 - 9:45					
		Coffee 9:45 -	Break 10:05			
1A (T1-1) System-Level Modeling and Design Methodologies 10:05 - 11:45	1B (T4.2-1) Tools and Techniques for On-Device AI Deployment 10:05 - 11:45	1C (T8-1) AI and Logic Synthesis - A perfect match? 10:05 - 11:20	1D (T3-1) Application- Specific Computing-In- Memory 10:05 - 11:45	1E (SS-1) Machine Learning Based Physical Simulation and Physics-Aware Optimization	1F (SS-CEDA) CEDA/CASS/SSCS Joint session on Silicon Photonics 10:05 - 11:45	
	Lunch Break					
2A (T5-1) Accelerating Vision and Transformer Models 13:15 - 15:20	2B (T6-1) Shaping the Future of Analog EDA 13:15 - 14:55	2C (T7-1) Approximate and Stochastic Computing 13:15 - 15:20	2D (T2-1) Next-Generation Embedded Architectures and Tools 13:15 - 15:20	2E (SS-2) Advances in 3D-IC and Ultra-Large-Scale Integration 13:15 - 15:20	2F University Design Contest 13:15 - 15:20	
Coffee Break 15:20 - 15:40						
3A (SS-3) LLM Acceleration and Specialization for Circuit Design and Edge Applications 15:40 - 17:20	3B (T9-1) Timing Analysis and Optimization 15:40 - 17:45	3C (T12-1) Side Channel Attacks and Trusted Execution Environment 15:40 - 17:45	3D (T3-2) Frameworks and Modeling for Computing-In- Memory 15:40 - 17:20	3E (T4.1-1) AI/ML for Circuit Design and Prediction 15:40 - 17:45		
1S (Room Jupiter) ACM SIGDA Student Research Forum / WIP Poster Session 18:00 - 20:00						

Room Saturn	Room Uranus	Room Venus	Room Mars/Mercury	Innovation Hall	Miraikan Hall	
	2K (Miraikan Hall) 30th Anniversary and Keynote Session II 8:30 - 9:45					
		Coffee 9:45 -	Break 10:05			
4A (T4.2-2) Advanced Methods in AI Hardware Co-Design 10:05 - 11:45	4B (T1-2) Communication Networks 10:05 - 11:45	4C (T2-2) Design and Optimization of Emerging Embedded Applications	4D (T11-1) Verification and Testing in Machine Lerning Era 10:05 - 11:45	4E (T3-3) Hybrid/Co- Designed Near/In Memory Computing	4F (SS-4) ML for IC Design and Manufacturing: When Is It Real? 10:05 - 11:45	
10:05 - 11:45 10:05 - 11:45 1W (Innovation Hall and more) CEDA 20th Anniversary Panel 12:00 - 13:00 13:00						
5A (T5-2) Innovations in Deep Learning and Neural Network Acceleration 13:15 - 15:20	5B (T7-2) Neuromorphic and Emerging Computing Techniques 13:15 - 15:20	5C (T9-2) Package and PCB 13:15 - 14:55	5D (T12-2) Logic Locking and Hardware Watermarking 13:15 - 14:55	5E (T4.1-2) AI-Driven Innovative Design Methods 13:15 - 15:20	5F (DF-1) Quantum Computing 13:15 - 14:30	
	Coffee Break 15:20 - 15:40					
6A (SS-5) Beyond Digital: Advancing Design Automation for Physical Computing Systems 15:40 - 17:20	6B (T9-3) Floorplan and Placement 15:40 - 17:45	6C (T13-1) Let's Quantumize: Welcome to the World of Quantum 15:40 - 16:55	6D (T10-1) Innovative Techniques for Energy-Efficient and Reliable Hardware Systems 15:40 - 17:45	6E (T4.1-3) Leveraging Large Language Models in Hardware Design 15:40 - 17:45	6F (DF-2) Advanced Sensor Technologies and Sensor Fusion 15:40 - 16:55	
Banquet 18:30 - 20:30						

Room Saturn	Room Uranus	Room Venus	Room Mars/Mercury	Innovation Hall	Miraikan Hall	
	3K (Miraikan Hall) Keynote Session III					
		9:00	- 9:45			
		Coffee	e Break			
		9:45 -	10:05			
7A (T1-3)	7B (T5-3)	7C (T6-2) The	7D (T8-2) From	7E (T4.2-3)	7F (SS-6)	
Accelerator Design	Advanced	Science of Light:	Math to Circuits	Innovative	Rapidus'	
Methodologies	Architectures for	the New	10:05 - 11:20	Techniques in AI	Initiatives to Half	
10:05 - 11:45	Scientific and Edge	Advancement of		Model	Semiconductor	
	Computing	Photonic		Optimization and	Development Time	
	10:05 - 11:45	Computing		Training	10:05 - 11:20	
		10:05 - 11:45		10:05 - 11:20		
		Lunch	Break			
		11:45	- 13:15			
8A (T1-4) System	8B (T5-4)	8C (T3-4)	8D (T9-4)	8E (SS-7)	8F (DF-3)	
Level Modelling &	Emerging Trends	Adaptive and	Reliability in	Hardware	Extending the	
Optimization	in Reconfigurable	Flexible Memory	Physical Design	Authenticity	Limits of Classical	
13:15 - 14:55	and Compute-in-	Architecture	13:15 - 14:55	towards a	Computers using	
	Memory	13:15 - 14:55		Trustworthy	Emerging Device	
	13:15 - 14:55			Society	and Circuit	
				13:15 - 14:55	Technology	
					13:15 - 14:30	
		Coffee	e Break			
		14:45	- 15:20			
9A (T12-3)	9B (T11-2)	9C (T13-2)	9D (T10-2)	9E (SS-8)	9F (DF-4)	
Homomorphic	Advanced	Carbon, Light,	Advanced	Innovations and	Integrated Circuit	
Encryption and	Modeling,	Fluids: Emerging	Techniques for	Challenges on	Design	
Cloud Security	Simulation, and	Technologies	Power	Cryo-CMOS	Methodologies	
15:20 - 17:30	Verification	15:20 - 17:30	Optimization and	Devices, Circuits	using Open Source	
	15:20 - 17:30		IR Prediction	and Design	and Artificial	
			15:20 - 17:30	Platforms	Intelligence	
				15:20 - 17:30	15:20 - 16:35	

DF: Designers' Forum, SS: Special Session

Highlights

Opening and Keynote I

Tuesday, January 21, 2025, 9:00-9:45

Kazunari Ishimaru (Rapidus Corporation)

"Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry"

Keynote II

Wednesday, January 22, 2025, 9:00-9:45

"Compilation and Architecture Optimization for Quantum Computing"

Jason Cong (UCLA)

Keynote III

Thursday, January 23, 2025, 9:00-9:45

Abu Sebastian (IBM Research Europe – Zurich)

"In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects"

Special Sessions

- **1E (SS-1): (Invited Talks) Machine Learning Based Physical Simulation and Physics-Aware Optimization** Tuesday, January 21, 2025, 10:05-11:45
- **1F (SS-CEDA): (Invited Talks) CEDA/CASS/SSCS Joint session on Silicon Photonics** Tuesday, January 21, 2025, 10:05-11:45
- **2E (SS-2): (Invited Talks) Advances in 3D-IC and Ultra-Large-Scale Integration** Tuesday, January 21, 2025, 13:15-15:20
- **2F: (Presentation + Poster Discussion) University Design Contest** Tuesday, January 21, 2025, 13:15-15:20
- **3A (SS-3): (Invited Talks) LLM Acceleration and Specialization for Circuit Design and Edge Applications** Tuesday, January 21, 2025, 15:40-17:20
- **4F (SS-4): (Invited Talks) ML for IC Design and Manufacturing: When Is It Real?** Wednesday, January 22, 2025, 10:05-11:45
- 1W: (Panel Discussion) CEDA 20th Anniversary Panel Wednesday, January 22, 2025, 12:00-13:00
- 6A (SS-5): (Invited Talks) Beyond Digital: Advancing Design Automation for Physical Computing Systems Wednesday, January 22, 2025, 15:40-17:20
- **7A (SS-6): (Invited Talk) Rapidus' Initiatives to Half Semiconductor Development Time** Thursday, January 23, 2025, 10:05-11:20
- **8E (SS-7): (Invited Talks) Hardware Authenticity towards a Trustworthy Society** Thursday, January 23, 2025, 13:15-14:55
- **9E (SS-8): (Invited Talks) Innovations and Challenges on Cryo-CMOS Devices, Circuits and Design Platforms** Thursday, January 23, 2025, 15:20-17:30

Designers' Forum

5F (DF-1): (Oral Session) Quantum Computing

Wednesday, January 22, 2025, 13:15-14:30

6F (DF-2): (Oral Session) Advanced Sensor Technologies and Sensor Fusion

Wednesday, January 22, 2025, 15:40-16:55

8F (DF-3): (Oral Session) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology

Thursday, January 23, 2025, 13:15-14:30

9E (DF-4): (Panel Discussion) Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence

Thursday, January 23, 2025, 15:20-16:35

Tutorials

ASP-DAC 2025 offers attendees a set of three-hour intense introductions to specific topics. If you register for the conference, you have the option to select two out of the four topics. T2 is a session with hands-on training.

Tutorial-1: Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

Monday, January 20, 2025, 9:30-12:30 @ Room Saturn

Speaker:

Taewhan Kim (Seoul National University)

Tutorial-2: AHS: An EDA toolbox for Agile Chip Front-end Design

Monday, January 20, 2025, 9:30-12:30 @ Innovation Hall

Speakers:

Yun (Eric) Liang (Peking University) Youwei Xiao (Peking University) Ruifan Xu (Peking University)

Tutorial-3: Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

Monday, January 20, 2025, 14:30-16:30 @ Room Saturn

Speaker:

Prashant Seetharaman (Siemens Digital Industries Software)

Tutorial-4: Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Monday, January 20, 2025, 14:30-17:30 @ Innovation Hall

Speaker:

Yiyu Shi (University of Notre Dame)

Room Assignment

Room Assignment

Location	Event
Lobby	Registration and Information Desk
Cloak	Cloak
Miraikan Hall	Opening, Keynotes I,II,III, ASP-DAC 30th Anniversary, University LSI Desing Contest (UDC), Designers' Forum (DF), and Session F
Room Jupiter	UDC Poster, ACM SIGDA Student Research Forum / WIP Poster, Coffee Break, and Supporter's Exhibition
Room Saturn	Session A and Tutorials 1 & 3
Room Uranus	Session B
Room Venus	Session C
Room Mars	Session D
Room Mercury	Session D
Innovation Hall	Session E, Tutorials 2 & 4, CEDA 20th Anniversary Panel, and Speaker's Breakfast
Room Phobos	Rehearsal Room
Room Deimos	File Checking Room
Room Neptune	SC/OC Meeting Room
Hilton Tokyo Odaiba, Room Pegasus (1F)	Banquet

Floor Map of Miraikan 7F:

Floor Map

30th Asia and South Pacific Design Automation Conference ASP-DAC 2025

Tutorials

ASP-DAC 2025 offers attendees a set of three-hour intense introductions to specific topics. If you register for the conference, you have the option to select two out of the four topics. T2 is a session with hands-on training.

	Monday, January 20			
9.30	Room Saturn	Innovation Hall		
2.20	Tutorial-1:	Tutorial-2:		
	Automation of Standard Cell Layout Generation and	AHS: An EDA toolbox for Agile Chin Front-end Design		
12:30	Design-Technology Co-optimization	Ans. An LDA tooloox for Agile Chip Hone-chi Design		
Lunch Break		Break		
2.100	Tutorial-3:	Tutorial-4:		
	Memory Built-In Self-Test (MBIST): Advanced	Efficient Deployment of Large Language Models on		
17:30	Techniques for SoC Design and Verification	Resource Constrained Edge Computing Platforms		

Tutorial-1 Monday, January 20, 9:30-12:30@Room Saturn

Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

Speaker:

Taewhan Kim (Seoul National University)

Abstract:

As the technology advances, the design rules to be considered in standard cell layout generation become much complex and the count increases very rapidly. Moreover, at the advanced nodes, it becomes much slow or very difficult to achieve the objective i.e., to deliver or find the best-yield target node design rules while ensuring PPA-excellent target chip implementation. This is the reason why, from the EDA perspective, the need for automatic cell layout generation is inevitable at the advanced nodes, and design and technology co-optimization is a key enabling technique to achieve the chip PPA objective.

In this respect, this tutorial covers EDA research area regarding two topics: (1) automation of standard cell layout generation and (2) methodologies of design and technology co-optimization utilizing diverse cell layout structures.

For standard cells, starting from the detailed layer-by-layer structure for cell layout synthesis, the complex design rules, the algorithms of cell synthesis including transistor placement and in-cell routing, and existing cell generation tools developed so far in academia with comparison of their distinct features and pros/cons will be covered. In addition, new EDA challenge of cell generation for next generation of BEOL and FEOL technologies will be discussed. For DTCO, starting from the DTCO concept utilizing standard cells, noticeable DTCO works focusing on, for target chip PPA improvement, multi-bit flip-flop cells, cells with pin inaccessibility, and cells with metal and gate poly misalignment will be covered.

Tutorial-2 Monday, January 20, 9:30-12:30@Innovation Hall AHS: An EDA toolbox for Agile Chip Front-end Design

Speakers:

Yun (Eric) Liang (Peking University), Youwei Xiao (Peking University), Ruifan Xu (Peking University)

Abstract:

Compared to software design, hardware design is more expensive and time-consuming. This is partly because software community has developed a rich set of modern tools to help software programmers to get projects started and iterated easily and quickly. However, the tools are seriously antiquated and lacking for hardware design. Modern digital chips are still designed manually using hardware description language such as Verilog or VHDL, which requires low-level and tedious programming, debugging, and tuning. In this tutorial, we will introduce AHS: An EDA toolbox for Agile Chip Front-end Design, which includes various EDA tools for both chip design and verification.

Tutorial-3 Monday, January 20, 14:30 - 16:30@Room Saturn

Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

Speaker:

Prashant Seetharaman (Siemens Digital Industries Software)

Abstract:

As System-on-Chip (SoC) designs continue to grow in complexity and memory density, ensuring the reliability and testability of embedded memories becomes increasingly critical. This tutorial presents an in-depth exploration of Memory Built-In Self-Test (MBIST), a powerful methodology for testing and diagnosing memory faults in modern SoC designs. We will discuss the fundamentals of MBIST, advanced implementation techniques, and emerging trends in the field. The tutorial also covers key aspects of MBIST, including architecture, test algorithm selection, integration in the SoC design flow, and strategies for optimizing test coverage and reducing test time. Through theoretical analysis and practical examples, we will demonstrate how MBIST addresses the challenges of testing high-density memories in complex SoCs, balancing test quality, silicon area overhead, and test time to achieve optimal results in real-world scenarios. Additionally, we explore the application of MBIST to emerging memory technologies encompassing non-volatile memories and resistive RAMs. Finally, we will discuss future directions in memory testing, including the use of machine learning and artificial intelligence techniques.

Tutorial-4 Monday, January 20, 14:30 - 17:30@Innovation Hall

Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Speaker:

Yiyu Shi (University of Notre Dame)

Abstract:

Scaling laws guide the design of large language models (LLMs), assuming unlimited computing resources, but this is impractical for deploying personalized LLMs on resource-constrained edge devices. Critical questions arise regarding trade-offs between design factors such as learning methods, data volume, model size, compression techniques, and training time and their impact on efficiency and accuracy. This tutorial provides comprehensive guidelines for deploying LLMs on constrained devices and explores how advanced hardware architectures like Compute-in-Memory (CiM) can aid this process. Attendees will learn to make informed decisions on key topics like choosing between compressed vs. uncompressed LLMs, selecting appropriate personalization techniques, and optimizing training time under resource limitations.

Keynote Addresses

Keynote I

Tuesday, January 21, 9:00-9:45

"Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry"

Dr. Kazunari Ishimaru (Rapidus Corporation)

As the semiconductor industry faces mounting pressure to meet both rising demand and sustainability challenges, the need for innovative design and effective collaboration with foundries has never been more critical.

The lead time from design to productization is becoming longer with each transition to the next generation, which is particularly critical in the rapidly growing AI market, where time to market is crucial. Additionally, traditional DFM (Design for Manufacturability) to address the increasingly complex device structures and manufacturing processes is also becoming more complicated, leading to longer design periods.

As a foundry, it is essential to provide feedback to the design space from a manufacturing perspective, and the realization of MFD (Manufacturing for Design) will become essential in the future. The DMCO (Design-Manufacturing Co-Optimization) proposed by Rapidus is a method to solve this issue, and collaboration with customers and ecosystem partners is crucial. Furthermore, collaborative efforts with foundries enable adopting sustainable production practices, such as reducing energy consumption, minimizing waste, and ensuring supply chain transparency.

The importance of integrating design innovation and foundry collaboration to build a semiconductor industry that is resilient, responsible, and aligned with global sustainability objectives.

Keynote II

Wednesday, January 22, 9:00-9:45

"Compilation and Architecture Optimization for Quantum Computing"

Prof. Jason Cong

(UCLA)

The rapid progress in quantum computing (QC) technologies in the past decade led to QC processors with hundreds to thousands of qubits. As a result, efficient compilation flow become both important and challenging. In this talk, I focus on the critical step of the compilation called quantum layout synthesis (QLS), which determines the space and time of computation of a quantum circuit. I first show that the existing QLS solutions, surprisingly, are far away from optimal, despite the effort of the research community for more than a decade. Then, I present recent progress on scalable and highly optimized QLS solutions for both QC processors with fixed connectivity, such as those based on the superconducting technology, and those with programmable connectivity, such as those using neutral atom arrays. Finally, I shall discuss how such optimized QLS tools can be used to guide QC processor architecture optimization, e.g. in determining the number of movable lasers and the configuration of storage vs computing zones for neutral atom arrays.

Keynote III

Thursday, January 23, 9:00-9:45

"In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects"

Dr. Abu Sebastian

(IBM Research Europe - Zurich)

Analog in-memory computing (AIMC), where synaptic weights are stored in nanoscale non-volatile memory elements and computations are carried out in the analogue or mixed-signal domain, represents a promising approach for developing the next generation of deep learning accelerators. In the first part of the presentation, I will explore the current advancements in this area, focusing on a 64-core AIMC chip built using 14nm CMOS technology with integrated phase-change memory. This chip achieves classification accuracy comparable to floating-point operations and demonstrates seamless integration of analogue and digital processing units. This work lays the foundation for a heterogeneous mixed-signal architecture. In the second part, I will cover ongoing efforts to design the next generation of AIMC chips for deep learning inference, targeting both edge and cloud applications.

University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The contest's purpose is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss innovative and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processor, (3) Microprocessors, and (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 18 designs from four countries/areas and selected 17 designs. The selected designs will be discussed in Session 2F on January 21 with short presentations and an interactive poster session. The poster session will start before lunch and continue until the coffee break. The Best Design Award and the Special Feature Award will be presented for two outstanding designs in the opening session. We sincerely acknowledge the other contributions to the contest, too. Our earnest belief is to promote and enhance research and education in LSI design in academic organizations. Please join the University LSI Design Contest and enjoy the stimulating discussions.

Date: Tuesday, January 21, 2025 Place: Tokyo Odaiba Waterfront, Japan

Oral Presentation: Miraikan Hall (13:15 - 15:20) Poster Presentation: Room Jupiter (11:45 - 13:15)

University LSI Design Contest Committee Co-Chairs:

Mahfuzul Islam (Institute of Science Tokyo)

Shinya Takamaeda-Yamazaki (The University of Tokyo)

Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions for real product developments among LSI designers and EDA academia/developers. The topics discussed in this forum include Quantum Computing, Advanced Sensor Technologies and Sensor Fusion, Extending the Limits of Classical Computers using Emerging Device and Circuit Technology, and Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence.

Oral Sessions: (5F) Quantum Computing

- (6F) Advanced Sensor Technologies and Sensor Fusion
- (8F) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology
- (9F) Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence

Session 5F (January 22, 13:15 - 14:30) [Quantum Computing]

This session will highlight the current and future directions in quantum computing hardware, control systems, and software architecture. The first presentation will delve into the implementation gap between traditional digital logic and quantum circuits, emphasizing the need for cross-disciplinary collaboration between physicists and conventional circuit designers. This gap highlights the unique challenges in developing circuits operating analog, passive systems where software defines quantum gates. The second presentation will discuss the development of a scalable controller for approximately 100 superconducting qubits. The speaker will explain how advanced hardware and software optimizations have facilitated complex quantum operations and will outline future goals to expand this controller's capacity, making it compatible with various qubit types and pushing toward real-world quantum applications. In the third presentation, the speaker will introduce their work on quantum algorithms and software, specifically for chemistry and Computer-Aided Engineering (CAE). By introducing the QURI SDK, a software platform designed for Fault-Tolerant Quantum Computing (FTQC), the speaker will demonstrate how multi-layered quantum software development enables practical quantum applications.

Session 6F (January 22, 15:40 -16:55)

[Advanced Sensor Technologies and Sensor Fusion]

This session showcases various sensor technologies, including human sensing and image sensors with 2D/3D or 2D/event sensing capabilities. The first presentation introduces radar-based human sensing technology, including posture detection, static human localization, and vital measurement for healthcare and smart home applications. The second talk will present a time-gated SPAD image sensor with 2D interactive gating network for alignment-free sensor fusion, which has a background suppression technique. The third talk will present an RGB Hybrid Event-based Vision Sensor, in which RGB pixels and event pixels are implemented on the same sensor showing the potential for realizing neural network-based deblurring applications.

Session 8F (January 23, 13:15 -14:40)

[Extending the Limits of Classical Computers using Emerging Device and Circuit Technology]

With the rapid development of quantum computers, conventional computers are referred to as classical computers. The demand for improved performance of classical computers will continue due to their potential for industrial use and the fact that quantum computers themselves will require classical computers to operate. The ideal performance improvements based on Moore's Law are already becoming difficult to achieve, and we must seek emerging approaches to both circuits and devices. In this session, three talks will be given on circuit and device technologies for improving the performance of classical computers. The first talk will present a circuit technology that improves the flexibility of domain-specific architectures. The second talk will present a device technology that aims to integrate optical and electrical information processing. The third talk will present a superconducting device aimed at energy-efficient computing.

Session 9F (January 23, 15:20 -16:35) [Integrated Circuit Design Methodologies using Open Source and Artificial Intelligence]

This session introduces recent design approaches using open source and artificial intelligence (AI) to ease the design of analog integrated circuits (ICs). The first presentation introduces how to design analog ICs in the online community based on experiences from Chipathon 2023. The next presentation introduces an open PDK development methodology to develop PDK more quickly and at a lower cost. The final presentation introduces the methods for automatically designing element values for analog ICs using AI.

Designers' Forum Co-Chairs: Takatsugu Ono (Kyusyu University)

Chihiro Yoshimura (Hitachi, Ltd.)

ACM SIGDA Student Research Forum at ASP-DAC 2025

The Student Research Forum (SRF) at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for PhD students to present and discuss their dissertations with experts in the design automation community. Starting from 2015, the forum includes both PhD and MS students, offering a great opportunity for the students to establish contacts for their future career. In addition, the forum helps companies and academic institutes to get an overview of the latest research and discover extraordinary candidates for their employment.

Date and Time: 18:00-20:00, January 21th, 2025 Location: Room Jupiter [Food will be served.]

We would like to thank the following committee members for their support and contribution to this forum.

Technical committee: **Muhammad Alfian Aamrizal** (UGM) **Daijoon Hyun** (Sejong University, Korea) **Heechun Park** (Ulsan National Institute of Science and Technology)

Ateet Bhalla (Independent Technology Consultant) Yanjing Li (University of Chicago) Taigon Song (Kyungpook National University)

ASP-DAC liaison: Shinichi Nishizawa (Waseda University) Masato Inagi (Hiroshima City University)

The sponsors of this forum are ACM SIGDA and Cadence Design Systems, Inc. We would also like to thank ASP-DAC 2025 for supporting this forum.

ACM SIGDA Student Research Forum Chair:

Heechun Park

(Ulsan National Institute of Science and Technology)

ACM SIGDA Student Research Forum Co-Chair:

Yanjing Li (University of Chicago)

WIP Poster Session at ASP-DAC 2025

In ASP-DAC 2025, we will host a WIP session. Presenters provide poster presentation on their ongoing work, with fresh problems/solutions. WIP content is typically material that may not be mature or complete enough for full paper submission and will not be included in the proceedings. This is an excellent opportunity to present and discuss ongoing research with experts from the design automation community around the world. We strongly encourage presentations at this session from students and young researchers from both of academics and industries.

Date and Time: 18:00-20:00, January 21th, 2025 Location: Room Jupiter

In Cooperation with:

IEEE Council on Electronic Design Automation (CEDA) All Japan Joint Chapter IEEE Circuits and Systems Society (CASS) Japan Joint Chapter

This session will be held in the same time of the Student Research Forum. This session is free for attendance. Presenters and Participants are not required the registration to ASP-DAC for this session only.

WIP Poster Session Chair:

Makoto Ikeda (The University of Tokyo)

WIP Poster Session Secretary:

Hiromitsu Awano (Kyoto University)

Supporter's Exhibition

Supporter's exhibition is held by two companies which support ASP-DAC 2025 and have exhibition booths. The supporter's exhibition is presented at Miraikan 7F Lobby from January 20 through January 23.

Exhibit Hours:	9:00 – 18:00, January 20
	9:45 – 20:00, January 21
	9:45 – 18:00, January 22
	9:45 – 18:00, January 23
Location:	Miraikan 7F Room Jupiter
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Monday, January 20, 2025

T1 Tutorial-1: Automation of Standard Cell Layout Generation and Design-Technology Co-optimization

Time: 9:30 - 12:30, Monday, January 20, 2025

Location: Room Saturn

T1-1 (Time: 9:30 - 12:30)

(Tutorial) Automation of Standard Cell Layout Generation and Design-Technology Co-optimization *Taewhan Kim (Seoul National Univ., Republic of Korea)

T2 Tutorial-2: AHS: An EDA toolbox for Agile Chip Front-end Design

Time: 9:30 - 12:30, Monday, January 20, 2025

Location: Innovation Hall

T2-1 (Time: 9:30 - 12:30)

(Tutorial) AHS: An EDA toolbox for Agile Chip Front-end Design Yun (Eric) Liang, Youwei Xiao, Ruifan Xu (Peking Univ., China)

T3 Tutorial-3: Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification

Time: 14:30 - 16:30, Monday, January 20, 2025

Location: Room Saturn

T3-1 (Time: 14:30 - 16:30)

(Tutorial) Memory Built-In Self-Test (MBIST): Advanced Techniques for SoC Design and Verification *Prashant Seetharaman (Siemens Digital Industries Software, USA)

T4 Tutorial-4: Efficient Deployment of Large Language Models on Resource Constrained Edge Computing Platforms

Time: 14:30 - 17:30, Monday, January 20, 2025 Location: Innovation Hall

T4-1 (Time: 14:30 - 17:30)

(Tutorial) Efficient Deployment of Large Language Models on Resource-Constrained Edge Computing Platforms *Yiyu Shi (Univ. of Notre Dame, USA)

1K Opening and Keynote Session I

Time: 8:30 - 9:45, Tuesday, January 21, 2025

Location: Miraikan Hall

Chair: Yuichi Nakamura (NEC, Japan)

1K-1

ASP-DAC 2025 Opening

1K-2

(Keynote Address) Design Innovation and Collaboration with Foundries: Towards a Sustainable Semiconductor Industry Kazunari Ishimaru (Rapidus, Japan)

1.4 (T1.1) System Level Modeling and Design Methodologies	
Times 10:05 11:45 Treader January 21 2025	
Leasting Deem Seture	
Chain Ling Ling (Mational Taing Hus Hain Taing)	
Chair: Jing-Jia Liou (National Ising Hua Univ., Taiwan)	
 1A-1 (Time: 10:05 - 10:30) MACO: A HW-Mapping Co-optimization Framework for DNN Accelerators	1
1A-2 (Time: 10:30 - 10:55)KAPLA: Scalable NN Accelerator Dataflow Design Space Structuring and Fast Exploring	8
1A-3 (Time: 10:55 - 11:20)	
Dynamic Co-Optimization Compiler: Leveraging Multi-Agent Reinforcement Learning for Enhanced DNN Accelerator	
Performance	16
1A-4 (Time: 11:20 - 11:45)	
(Guangdong Institute of Intelligence Science and Technology, China), Jiawei Xu (Royal Inst. of Tech., Sweden), Qitao Tan (Univ. of Georgia, USA), Jun Liu (Northeastern Univ., USA), Ao Li (Univ. of Arizona, USA), Xulong Tang (Univ. of Pittsburgh, USA), Lirong Zheng (Fudan Univ., China), Geng Yuan (Univ. of Georgia, USA), Zhuo Zou (Fudan Univ., China)	
1B (T4.2-1) Tools and Techniques for On-Device AI Deployment	
Time: 10:05 - 11:45, Tuesday, January 21, 2025	
Location: Room Uranus	
Chairs: Jongeun Lee (Ulsan National Inst. of Science and Tech. (UNIST)), Youngsoo Shin (KAIST, Republic of Korea)	
1B-1 (Time: 10:05 - 10:30)	
Sequential Printed Multilayer Perceptron Circuits for Super-TinyML Multi-Sensory Applications	30
1B-2 (Time: 10:30 - 10:55)	
Learning to Prune and Low-Rank Adaptation for Compact Language Model Deployment	36
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LightCL: Compact Continual Learning with Low Memory Footprint For Edge Device	43

*Zeqing Wang, Fei Cheng, Kangye Ji, Bohu Huang (Xidian Univ., China)

1B-4 (Time: 11:20 - 11:45)

(T8-1) AI and Logic Synthesis - A perfect match? **1C** 10:05 - 11:20, Tuesday, January 21, 2025 Time: Location: Room Venus Chairs: Christophe Dubach (McGill Univ., Canada), Andrea Costamagna (EPFL, Switzerland) 1C-1 (Time: 10:05 - 10:30) High-Effort Logic Synthesis Using Randomized Transduction 58 *Yukio Miyasaka (UC Berkeley/X, the moonshot factory, USA), Alan Mishchenko, John Wawrzynek (UC Berkeley, USA), Dino Ruić, Xiaoqing Xu (X, the moonshot factory, USA) 1C-2 (Time: 10:30 - 10:55) *Guande Dong, Jianwang Zhai, Hongtao Cheng, Xiao Yang, Chuan Shi, Kang Zhao (Beijing Univ. of Posts and Telecommunications, China) 1C-3 (Time: 10:55 - 11:20) Faezeh Faez, Raika Karimi, *Yingxue Zhang (Huawei Noah's Ark Lab, Canada), Xing Li, Lei Chen, Mingxuan Yuan (Huawei Noah's Ark Lab, China), Mahdi Biparva (Huawei Noah's Ark Lab, Canada) (T3-1) Application-Specific Computing-In-Memory 1D Time: 10:05 - 11:45, Tuesday, January 21, 2025 Location: Room Mars/Mercury Chairs: Hiromitsu Awano (Kyoto Univ., Japan), Yiming Chen (Tsinghua Univ., China) 1D-1 (Time: 10:05 - 10:30) Tsung-Yu Liu (Academia Sinica, Taiwan), Yen An Lu (Cornell Univ., USA), James Yu (Georgia Tech, USA), *Chin-Fu Nien (National Yang Ming Chiao Tung Univ., Taiwan), Hsiang-Yun Cheng (Academia Sinica, Taiwan) 1D-2 (Time: 10:30 - 10:55) *Bing Li, Huaijun Liu (Capital Normal Univ., China), Yibo Du (Chinese Academy of Sciences/Univ. of Chinese Academy of Sciences, China), Ying Wang (Chinese Academy of Sciences, China) 1D-3 (Time: 10:55 - 11:20) Efficient and Reliable Vector Similarity Search Using Asymmetric Encoding with NAND-Flash for Many-Class Few-Shot *Hao-Wei Chiang, Chi-Tse Huang (National Taiwan Univ., Taiwan), Hsiang-Yun Cheng (Academia Sinica, Taiwan), Po-Hao Tseng, Ming-Hsiu Lee (Macronix International, Taiwan), An-Yeu (Andy) Wu (National Taiwan Univ., Taiwan) 1D-4 (Time: 11:20 - 11:45)

DCiROM: A Fully Digital Compute-in-ROM Design Approach to High Energy Efficiency of DNN Inference at Task Level . . 100 *Tianyi Yu, Tianyu Liao, Mufeng Zhou, Xiaotian Chu, Guodong Yin, Mingyen Lee, Yongpan Liu, Huazhong Yang, Xueqing Li (Tsinghua Univ., China)

1E (SS-1) Machine Learning Based Physical Simulation and Physics-Aware Optimization
Time: 10:05 - 11:45, Tuesday, January 21, 2025
Location: Innovation Hall
Chairs: Wenjian Yu (Tsinghua Univ., China), Yuanqing Cheng (Beihang Univ., China)
1E-1 (Time: 10:05 - 10:30) (Invited Paper) Deep Learning Inspired Capacitance Extraction Techniques *Wenjian Yu, Shan Shen, Dingcheng Yang, Haoyuan Li, Jiechen Huang, Chunyan Pei (Tsinghua Univ., China)
 1E-2 (Time: 10:30 - 10:55) (Invited Paper) Enhanced Operator Learning for Scalable and Ultra-fast Thermal Simulation in 3D-IC Design
 1E-3 (Time: 10:55 - 11:20) (Invited Paper) Boosting the Performance of Transistor-Level Circuit Simulation with GNN Jiqing Jiang, Yongqiang Duan, *Zhou Jin (China Univ. of Petroleum-Beijing, China)
1E-4 (Time: 11:20 - 11:45) (Invited Paper) Emag-Aware ML-Based Layout Optimization for High-Speed IC Design *Garth Sundberg (ANSYS, USA), Rodger Luo (ANSYS, China)
1F (SS-CEDA) CEDA/CASS/SSCS Joint session on Silicon Photonics
Time: 10:05 - 11:45, Tuesday, January 21, 2025
Chair: Tsung-Yi Ho (Chinese Univ. of Hong Kong, Hong Kong)
 1F-1 (Time: 10:05 - 10:30) (Invited Paper) Bridging EDA and Silicon Photonics Design: Enabling Robust-by-Design Photonic Integrated Circuits Zahra Ghanaatian, Asif Mirza, Amin Shafiee, Sudeep Pasricha, *Mahdi Nikdast (Colorado State Univ., USA)
 1F-2 (Time: 10:30 - 10:55) (Invited Paper) SPICE-Compatible Modeling and Design for Electronic-Photonic Integrated Circuits
 1F-3 (Time: 10:55 - 11:20) (Invited Paper) Modeling and Simulation of Silicon Photonics Systems in SystemVerilog/XMODEL
 1F-4 (Time: 11:20 - 11:45) (Invited Paper) Si Photonic Ring-Resonator-Based WDM Transceivers
2A (T5-1) Accelerating Vision and Transformer Models
Time: 13:15 - 15:20, Tuesday, January 21, 2025
Location: Room Saturn
Chairs: Quan Chen (Southern Univ. of Science and Tech., China), Sheldon Tan (UC Riverside, USA)
2A-1 (Time: 13:15 - 13:40)

2A-2 (Time: 13:40 - 14:05)

2A-3 (Time: 14:05 - 14:30)

UEDA: A Universal And Efficient Deformable	Attention Accelerator For Various Vision Tasks	163
Kairui Sun, *Meiqi Wang, Junhai Zhou,	Zhongfeng Wang (Sun Yat-sen Univ., China)	

2A-4 (Time: 14:30 - 14:55)

Deploying Diffusion Models with Scheduling Space Search and Memory Overflow Prevention Based on Graph Optimization 170 *Hao Zhou, Yang Liu, Hongji Wang (Fudan Univ., China), EnHao Tang (Nanjing Univ., China), Shun Li (Southeast Univ., China), Yifan Zhang (Fudan Univ., China), Guohao Dai (Shanghai Jiao Tong Univ., China), Yongpan Liu (Tsinghua Univ., China)

2A-5 (Time: 14:55 - 15:20)

TWDP: A Vision Transformer Accelerator with Token-Weight Dual-Pruning Strategy for Edge Device Deployment 177 *Guang Yang, Xinming Yan, Hui Kou, Zihan Zou, Qingwen Wei, Hao Cai, Bo Liu (Southeast Univ., China)

2B (T6-1) Shaping the Future of Analog EDA Time: 13:15 - 14:55, Tuesday, January 21, 2025 Location: Room Uranus Zhou Jin (China Univ. of Petroleum, China), Nobukazu Takai (Kyoto Inst. of Tech.) Chairs: 2B-1 (Time: 13:15 - 13:40) *Baiyu Chen, Jiawen Cheng, Wenjian Yu (Tsinghua Univ., China) 2B-2 (Time: 13:40 - 14:05) *Jintao Li (Univ. of Electronic Science and Tech. of China, China), Haochang Zhi (Southeast Univ., China), Jiang Xiao (Univ. of Electronic Science and Tech. of China, China), Yanhan Zeng (Guangzhou Univ., China), Weiwei Shan (Southeast Univ., China), Yun Li (Univ. of Electronic Science and Tech. of China, China) 2B-3 (Time: 14:05 - 14:30) *Haochang Zhi (Southeast Univ., China), Jintao Li, Yun Li (Shenzhen Institute for Advanced Study, UESTC, China),

Weiwei Shan (Southeast Univ., China)

2B-4 (Time: 14:30 - 14:55)

2C (T7-1) Approximate and Stochastic Computing

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Room Venus

Chair: Yue Zhang (Beihang Univ., China)

2C-1 (Time: 13:15 - 13:40)

Stochastic Multivariate Universal-Radix Finite-State Machine: a Theoretically and Practically Elegant Nonlinear Function	
Approximator	11
*Xincheng Feng (Univ. of Hong Kong, Hong Kong), Guodong Shen, Jianhao Hu (Univ. of Electronic Science and	
Tech. of China, China), Meng Li (Peking Univ., China), Ngai Wong (Univ. of Hong Kong, Hong Kong)	
2C-2 (Time: 13:40 - 14:05)	
ACLAM: Accuracy-Configurable Logarithmic Approximate Floating-point Multiplier	18
*Zhongyu Guan, Qiang Liu (Tianjin Univ., China), Guangdong Lin (Anhui Siliepoch Technology Company, China)	
2C-3 (Time: 14:05 - 14:30)	
AmPEC: Approximate MRAM with Partial Error Correction for Fine-grained Energy-quality Trade-off	24
*Lan-yang Sun (Southeast Univ., China), Yaoru Hou (Hong Kong Univ. of Science and Tech., Hong Kong), Hao Cai	
(Southeast Univ., China)	
2C-4 (Time: 14:30 - 14:55)	

2C-5 (Time: 14:55 - 15:20)

2D (T2-1) Next-Generation Embedded Architectures and Tools

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Room Mars/Mercury

Chair: Chao Huang (Univ. of Southampton)

2D-1 (Time: 13:15 - 13:40)

PULSE: Progressive Utilization of Log-Structured Techniques to Ease SSD Write Amplification in B-epsilon-tree
Huai-De Peng (National Central Univ., Taiwan), *Yi-Shen Chen (National Taiwan Univ. of Science and Tech.,
Taiwan), Tseng-Yi Chen (National Central Univ., Taiwan), Yuan-Hao Chang (Academia Sinica, Taiwan)
2D-2 (Time: 13:40 - 14:05)
Rethinking $B^{\mathcal{E}}$ tree Indexing Structure over NVM with the Support of Multi-write Modes
Hui-Tang Luo, *Tseng-Yi Chen (National Central Univ., Taiwan)
2D-3 (Time: 14:05 - 14:30)
End-to-end Compilation is All FPGAs Need: A Unified Overlay-based FPGA Compiler for Deep Learning
*Kai Qian, Haodong Lu (Fudan Univ., China), Yinqiu Liu (Nanyang Technological Univ., Singapore), Zexu Zhang,

Kun Wang (Fudan Univ., China)

2D-4 (Time: 14:30 - 14:55)

2D-5 (Time: 14:55 - 15:20)

HAMMER: Hardware-aware Runtime Program Execution Acceleration through runtime reconfigurable CGRAs 272 Qilin Si, *Benjamin Carrion Schafer (Univ. of Texas, Dallas, USA)

2E (SS-2) Advances in 3D-IC and Ultra-Large-Scale Integration

Time: 13:15 - 15:20, Tuesday, January 21, 2025

Location: Innovation Hall

Chair: Yibo Lin (Peking Univ., China)

2E-1 (Time: 13:15 - 13:40)

2E-1 (Time: 13:15 - 13:40)	
Invited Paper) Fast Routing Algorithm for Mask Stitching Region of Ultra Large Wafer Scale Integration	
2E-2 (Time: 13:40 - 14:05)	
Invited Paper) The Survey of 2.5D Integrated Architecture: An EDA perspective	
2E-3 (Time: 14:05 - 14:30)	
Invited Paper) Toward Advancing 3D-ICs Physical Design: Challenges and Opportunities	
2E-4 (Time: 14:30 - 14:55)	
Invited Paper) Processing-Near-Memory with Chip Level 3D-IC	
 2E-5 (Time: 14:55 - 15:20) (Invited Paper) Clustering-Driven Bonding Terminal Legalization with Reinforcement Learning for F2F 3D ICs	

2F University Design Contest Time: 13:15 - 15:20, Tuesday, January 21, 2025 Chairs: Mahfuzul Islam (Tokyo Inst. of Tech., Japan), Shinya Takamaeda Yamazaki (Univ. of Tokyo, Japan) 2F-1 (Time: 13:15 - 13:20) A 10.60 µW 150 GOPS Mixed-Bit-Width Sparse CNN Accelerator for Life-Threatening Ventricular Arrhythmia Detection ... 315 Yifan Qin, Zhenge Jia, Zheyu Yan (Univ. of Notre Dame, USA), Jay Mok, Manto Yung, Yu Liu, Xuejiao Liu (Hong Kong Univ. of Science and Tech./AI Chip Center for Emerging Smart System, Hong Kong), Wujie Wen (North Carolina State Univ., USA), Luhong Liang, Kwang-Ting Tim Cheng (Hong Kong Univ. of Science and Tech./AI Chip Center for Emerging Smart System, Hong Kong), Xiaobo Sharon Hu, *Yiyu Shi (Univ. of Notre Dame, USA) 2F-2 (Time: 13:20 - 13:25) Zhiwei Zhong (Northwestern Univ., USA), Yijie Wei (Kilby Labs, Texas Instruments, USA), Lance Go, Yiqi Li, *Jie Gu (Northwestern Univ., USA) 2F-3 (Time: 13:25 - 13:30) Humanoid Robot Control: A Mixed-Signal Footstep Planning SoC with ZMP Gait Scheduler and Neural Inverse Kinematics 321 Qiankai Cao, Yiqi Li, Juin Chuen Oh, *Jie Gu (Northwestern Univ., USA) 2F-4 (Time: 13:30 - 13:35) A Coarse- and Fine-Grained LUT Segmentation Method Enabling Single FPGA Implementation of Wired-Logic DNN *Yuxuan Pan, Dongzhu Li, Mototsugu Hamada, Atsutake Kosuge (Univ. of Tokyo, Japan) 2F-5 (Time: 13:35 - 13:40) *Heming Sun, Jing Wang (Yokohama National Univ., Japan), Silu Liu, Shinji Kimura (Waseda Univ., Japan), Masahiro Fujita (Univ. of Tokyo, Japan) 2F-6 (Time: 13:40 - 13:45) Transformer Hetero-CiM: Heterogeneous Integration of ReRAM CiM and SRAM CiM for Vision Transformer at Edge *Naoko Misawa, Tao Wang, Chihiro Matsui, Ken Takeuchi (Univ. of Tokyo, Japan) 2F-7 (Time: 13:45 - 13:50) A High-Density Hybrid Buck Converter with a Charge Converging Phase Reducing Inductor Current for 12V Power Supply *Yichao Ji, Ji Jin, Lin Cheng (Univ. of Science and Tech. of China, China) 2F-8 (Time: 13:50 - 13:55) A 500-MS/s 8-bit SAR ADC Generated from an Automated Layout Generation Framework in 14-nm FinFET Technology ... 338 *Yunseong Jo, Taeseung Kang (Hanyang Univ., Republic of Korea), Jeonghyu Yang (Ramschip, Republic of Korea), Jaeduk Han (Hanyang Univ., Republic of Korea) 2F-9 (Time: 13:55 - 14:00) A 4-Stream 8-Element Time-Division MIMO Phased-Array Receiver for 5G NR and Beyond Achieving 9.6Gbps Data Rate . 342 *Yi Zhang, Minzhe Tang, Zheng Li, Dongfan Xu, Kazuaki Kunihiro, Hiroyuki Sakai, Atsushi Shirane, Kenichi Okada (Institute of Science Tokyo, Japan) 2F-10 (Time: 14:00 - 14:05) *Yuyang Zhu, Zunsong Yang, Zhenyu Cheng, Md Shamim Sarker, Hiroyasu Yamahara, Munetoshi Seki, Hitoshi Tabata, Tetsuya Iizuka (Univ. of Tokyo, Japan) 2F-11 (Time: 14:05 - 14:10) *Koji Kikuta, Takashi Hisakado (Kyoto Univ., Japan), Mahfuzul Islam (Tokyo Inst. of Tech., Japan) 2F-12 (Time: 14:10 - 14:15) *Dongfan Xu, Minzhe Tang, Yi Zhang, Zheng Li, Jian Pang, Atsushi Shirane, Kenichi Okada (Institute of Science Tokyo, Japan)

2F-13 (Time: 14:15 - 14:20)

2F-14 (Time: 14:20 - 14:25)

Low quiescent current LDO with FBPEC to improve PSRR specific frequency band for wearable EEG recording devices 356 *Kenji Mii, Daisuke Kanemoto, Tetsuya Hirose (Osaka Univ., Japan)

2F-15 (Time: 14:25 - 14:30)

2F-16 (Time: 14:30 - 14:35)

2F-17 (Time: 14:35 - 14:40)

3A (SS-3) LLM Acceleration and Specialization for Circuit Design and Edge Applications

Time: 15:40 - 17:20, Tuesday, January 21, 2025

Location: Room Saturn

Chairs: Zheyu Yan (Zhejiang Univ., China), Cheng Zhuo (Zhejiang Univ., China)

3A-1 (Time: 15:40 - 16:05)

3A-2 (Time: 16:05 - 16:30)

3A-3 (Time: 16:30 - 16:55)

3A-4 (Time: 16:55 - 17:20)

3B (T9-1) Timing Analysis and Optimization Time: 15:40 - 17:45, Tuesday, January 21, 2025 Location: Room Uranus Chair: Heechun Park (Ulsan National Inst. of Science and Tech., Republic of Korea)

3B-1 (Time: 15:40 - 16:05)

 3B-2 (Time: 16:05 - 16:30) SI-Aware Wire Timing Prediction at Pre-Routing Stage with Multi-Corner Consideration	
 3B-3 (Time: 16:30 - 16:55) iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis	
 3B-4 (Time: 16:55 - 17:20) PathGen: An Efficient Parallel Critical Path Generation Algorithm	
 3B-5 (Time: 17:20 - 17:45) Yield-driven Clock Skew Scheduling Based on Generalized Extreme Value Distribution	
3C (T12-1) Side Channel Attacks and Trusted Execution Environment	
Time: 15:40 - 17:45, Tuesday, January 21, 2025	
Location: Room Venus	
Chairs: Qiang Liu (Tianjin Univ., China), Song Chen (Univ. of Science and Tech. of China, China)	
 3C-1 (Time: 15:40 - 16:05) Making Legacy Hardware Robust against Side Channel Attacks via High-Level Synthesis	
 3C-2 (Time: 16:05 - 16:30) Machine Learning-Based Real-Time Detection of Power Analysis Attacks Using Supply Voltage Comparisons	
 3C-3 (Time: 16:30 - 16:55) Side-channel Collision Attacks on Hyper-Dimensional Computing based on Emerging Resistive Memories	
 3C-4 (Time: 16:55 - 17:20) Dep-TEE: Decoupled Memory Protection for Secure and Scalable Inter-enclave Communication on RISC-V	
 3C-5 (Time: 17:20 - 17:45) Through Fabric: A Cross-world Thermal Covert Channel on TEE-enhanced FPGA-MPSoC Systems	

Henkel (KIT, Germany)

3D (T3-2) Frameworks and Modeling for Computing-In-Memory
Time: 15:40 - 17:20, Tuesday, January 21, 2025
Location: Room Mars/Mercury
Chairs: Zhou Jin (China Univ. of Petroleum, China), Kentaro Yoshioka (Keio Univ., Japan)
 3D-1 (Time: 15:40 - 16:05) Theoretical Optimal Specifications of Memcapacitors for Charge-Based In-Memory Computing
 3D-2 (Time: 16:05 - 16:30) An Island Style Multi-Objective Evolutionary Framework for Synthesis of Memristor-Aided Logic
 3D-3 (Time: 16:30 - 16:55) PIMutation: Exploring the Potential of Real PIM Architecture for Quantum Circuit Simulation
 3D-4 (Time: 16:55 - 17:20) A Fail-Slow Detection Framework for HBM devices
3E (T4.1-1) AI/ML for Circuit Design and Prediction
Time: 15:40 - 17:45, Tuesday, January 21, 2025
Location: Innovation Hall
Chair: Jaeyong Chung (Yonsei Univ., Republic of Korea)
 3E-1 (Time: 15:40 - 16:05) DeepSeq2: Enhanced Sequential Circuit Learning with Disentangled Representations
 3E-2 (Time: 16:05 - 16:30) A Self-Supervised, Pre-Trained, and Cross-Stage-Aligned Circuit Encoder Provides a Foundation for Various Design Tasks . 505 *Wenji Fang, Shang Liu (Hong Kong Univ. of Science and Tech., Hong Kong), Hongce Zhang (Hong Kong Univ. of Science and Tech. (GZ), China), Zhiyao Xie (Hong Kong Univ. of Science and Tech., Hong Kong)
 3E-3 (Time: 16:30 - 16:55) ParaFormer: A Hybrid Graph Neural Network and Transformer Approach for Pre-Routing Parasitic RC Prediction
 3E-4 (Time: 16:55 - 17:20) Static IR Drop Prediction with Limited Data from Real Designs
 3E-5 (Time: 17:20 - 17:45) Towards Big Data in AI for EDA Research: Generation of New Pseudo-Circuits at RTL Stage

2K 30th Anniversary and Keynote Session II

Time: 8:30 - 9:45, Wednesday, January 22, 2025

Location: Miraikan Hall

Chair: Shinji Kimura (Waseda Univ., Japan)

2K-1

30th Anniversary

2K-2

(Keynote Address) Compilation and Architecture Optimization for Quantum Computing Jason Cong (UCLA, USA)

4A (T4	2-2) Advanced Methods in AI Hardware Co-Design
Time:	10:05 - 11:45, Wednesday, January 22, 2025
Location	: Room Saturn
Chairs:	Wanyeong Jung (Korea Advanced Inst. of Science and Tech. (KAIST)), Yeseong Kim (DGIST, Republic of Korea)
4A-1 (Time: 10 Accelerator fo *Jiamin	0:05 - 10:30) or LLM-Enhanced GNN with Product Quantization and Unified Indexing
4A-2 (Time: 10 MICSim: A M *Cong):30 - 10:55) Iodular Simulator for Mixed-signal Compute-in-Memory based AI Accelerator
4A-3 (Time: 10 DIAG: A Refi *Haojia):55 - 11:20) ned Four-layer Agile Hardware Developing Flow for Generating Flexible Reconfigurable Architectures 548 Hui, Jiangyuan Gu, Xunbo Hu, Shaojun Wei, Shouyi Yin (Tsinghua Univ., China)
4A-4 (Time: 1 MPICC: Mult *Leran Wei, We	1:20 - 11:45) iple-Precision Inter-Combined MAC Unit with Stochastic Rounding for Ultra-Low-Precision Training 554 Huang (Tsinghua Shenzhen International Graduate School, China), Yongpan Liu, Xinyuan Lin, Chenhan enyu Sun, Zengwei Wang, Boran Cao, Chi Zhang, Xiaoxia Fu, Wentao Zhao (Tsinghua Univ., China)
4B (T1-	2) Communication Networks
Time:	10:05 - 11:45, Wednesday, January 22, 2025
Location	: Room Uranus
Chair:	Jiang Xu (Hong Kong Univ. of Science and Tech. (GZ), Hong Kong)
4B-1 (Time: 10 Physically Aw Sequence-Bas *Wei-Y	2:05 - 10:30) Vare Wavelength-Routed Optical NoC Design for Customized Topologies with Parallel Switching Elements and ed Models
4B-2 (Time: 10 Zipper: Laten *Shibo USA)	0:30 - 10:55) cy-Tolerant Optimizations for High-Performance Buses
4B-3 (Time: 10 A Buffer Rese *Zixuar	0:55 - 11:20) rvation Scheduling Strategy for Enhancing Performance of NoC Router Bypassing
4B-4 (Time: 1 RUNoC: Re-i *Xingh Fudan I	1:20 - 11:45) nject into the Underground Network to Alleviate Congestion in Large-Scale NoC

4C (T2-2) Design and Optimization of Emerging Embedded Applications
Time: 10:05 - 11:45, Wednesday, January 22, 2025
Location: Room Venus
Chair: Fang-Jing Wu (National Taiwan Univ., Taiwan)
 4C-1 (Time: 10:05 - 10:30) A Hierarchical Dataflow-Driven Heterogeneous Architecture for Wireless Baseband Processing
 4C-2 (Time: 10:30 - 10:55) Exploiting Differential-Based Data Encoding for Enhanced Query Efficiency
 4C-3 (Time: 10:55 - 11:20) Automated Power-saving User-interfaces for Application Designers
 4C-4 (Time: 11:20 - 11:45) An Edge AI and Adaptive Embedded System Design for Agricultural Robotics Applications
4D (T11-1) Verification and Testing in Machine Lerning Era
Time: 10:05 - 11:45, Wednesday, January 22, 2025
Location: Room Mars/Mercury
Chair: Michihiro Shintani (Kyoto Inst. of Tech., Japan)
 4D-1 (Time: 10:05 - 10:30) AssertLLM: Generating Hardware Verification Assertions from Design Specifications via Multi-LLMs
 4D-2 (Time: 10:30 - 10:55) Learning Gate-level Netlist Testability in the Presence of Unknowns through Graph Neural Networks
 4D-3 (Time: 10:55 - 11:20) Efficient ML-Based Transient Thermal Prediction for 3D-ICs
 4U-4 (Time: 11:20 - 11:45) Device-Aware Test for Anomalous Charge Trapping in FeFETs
4E (T3-3) Hybrid/Co-Designed Near/In Memory Computing
Time: 10:05 - 11:45, Wednesday, January 22, 2025
Location: Innovation Hall
Chairs: Bokyung Kim (Rutgers Univ., USA), Zhong Sun (Peking Univ., China)
4E-1 (Time: 10:05 - 10:30) 3D-METRO: Deploy Large-Scale Transformer Model on a Chip Using Transistor-Less 3D-Metal-ROM-Based Compute-in- Memory Macro
riming Chen, *Xirui Du, Guodong Yin, wenjun lang, Yongpan Liu, Huazhong Yang, Xueqing Li (Tsinghua Univ.,

China)

4E-2 (Time: 10:30 - 10:55)

 HCiM: ADC-Less Hybrid Analog-Digital Compute in Memory Accelerator for Deep Learning Workloads
 4E-3 (Time: 10:55 - 11:20) MDNMP: Metapath-Driven Software-Hardware Co-Design for HGNN Acceleration with Near-Memory Processing
 4E-4 (Time: 11:20 - 11:45) A 24.65 TOPS/W@INT8 Hybrid Analog-Digital Multi-core SRAM CIM Macro with Optimal Weight Dividing and Resource Allocation Strategies
4F (SS-4) ML for IC Design and Manufacturing: When Is It Real?
Time: 10:05 - 11:45, Wednesday, January 22, 2025
Chairs: Yibo Lin (Peking Univ., China), Youngsoo Shin (KAIST, Republic of Korea)
 4F-1 (Time: 10:05 - 10:30) (Invited Paper) Use Cases and Deployment of ML in IC Physical Design
 4F-2 (Time: 10:30 - 10:55) (Invited Paper) Leveraging Machine Learning Techniques to Enhance Traditional EDA Workflows
 4F-3 (Time: 10:55 - 11:20) (Invited Paper) ML-Assisted RF IC Design Enablement: the New Frontier of AI for EDA
4F-4 (Time: 11:20 - 11:45) (Invited Paper) ML for Computational Lithography: Practical Recipes
1W CEDA 20th Anniversion Denel

1W CEDA 20th Anniversary Panel

Time: 12:00 - 13:00, Wednesday, January 22, 2025

Location: Innovation Hall and more

Organizer: Tsung-Yi Ho (Chinese Univ. of Hong Kong, Hong Kong), Panel Moderator: Yu Wang (Tsinghua Univ., China)

1W-1 (Time: 12:00 - 13:00)

(Panel Discussion) CEDA 20th Anniversary Panel

Panelists: Yao-Wen Chang (National Taiwan Univ., Taiwan), Kwang-Ting Cheng (Hong Kong Univ. of Science and Tech., Hong Kong), Shinji Kimura (Waseda Univ., Japan), Jeong-Taek Kong (Sungkyunkwan Univ., Republic of Korea)

5A (T5-2) Innovations in Deep Learning and Neural Network Acceleration

Time: 13:15 - 15:20, Wednesday, January 22, 2025

Location: Room Saturn

Chair: Shinya Takamaeda Yamazaki (Univ. of Tokyo, Japan)

5A-1 (Time: 13:15 - 13:40)

5A-2 (Time: 13:40 - 14:05)

5A-3 (Time: 14:05 - 14:30)

5A-4 (Time: 14:30 - 14:55)

LUTMUL: Exceed Conventional FPGA Roofline Limit by LUT-based Efficient Multiplication for Neural Network Inference 713 Yanyue Xie (Northeastern Univ., USA), Zhengang Li (Adobe, USA), Dana Diaconu, Suranga Handagala, Miriam Leeser, *Xue Lin (Northeastern Univ., USA)

5A-5 (Time: 14:55 - 15:20)

(T7-2) Neuromorphic and Emerging Computing Techniques 5B Time: 13:15 - 15:20, Wednesday, January 22, 2025 Location: Room Uranus Georgios Zervakis (Univ. of Patras, Greece) Chair: 5B-1 (Time: 13:15 - 13:40) Yitian Zhou, Yue Li, *Yang Hong (Shanghai Jiao Tong Univ., China) 5B-2 (Time: 13:40 - 14:05) *Haomin Li, Fangxin Liu (Shanghai Jiao Tong Univ., China), Zewen Sun (Tianjin Univ., China), Zongwu Wang, Shiyuan Huang, Ning Yang, Li Jiang (Shanghai Jiao Tong Univ., China) 5B-3 (Time: 14:05 - 14:30) Bo Li, *Yue Liu, Wei Liu, Jinghai Wang, Xiao Huang, Zhiyi Yu, Shanlin Xiao (Sun Yat-sen Univ., China) 5B-4 (Time: 14:30 - 14:55) *Jiaqi Liu (Hong Kong Univ. of Science and Tech., Hong Kong), Yiwen Ma (Chinese Academy of Sciences, China) 5B-5 (Time: 14:55 - 15:20) *Paula Carolina Lozano Duarte (Karlsruhe Inst. of Tech., Germany), Florentia Afentaki, Georgios Zervakis (Univ. of Patras, Greece), Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany) **5**C (T9-2) Package and PCB Time: 13:15 - 14:55, Wednesday, January 22, 2025 Location: Room Venus

Chair: Pei-Yu Lee (Mediatek, Taiwan)

5C-1 (Time: 13:15 - 13:40)

5C-2 (Time: 13:40 - 14:05)

5C-3 (Time: 14:05 - 14:30)

On Awareness of Offset-Via and Teardrop in Advanced Packaging Interconnect Synthesis	. 774
5C-4 (Time: 14:30 - 14:55)	
PCBAgent: An Agent-based Framework for High-Density Printed Circuit Board Placement	781
5D (T12-2) Logic Locking and Hardware Watermarking	
Time: 13:15 - 14:55, Wednesday, January 22, 2025	
Location: Room Mars/Mercury	
Chairs: Daisuke Fujimoto (NAIST, Japan), Amin Rezaei (California State Univ., Long Beach, USA)	
5D-1 (Time: 13:15 - 13:40) NoXLock: SiP Activation and Licensing through Obfuscated on-Chip Network and Fuzzy Traffic	. 788
 5D-2 (Time: 13:40 - 14:05) K-Gate Lock: Multi-Key Logic Locking Using Input Encoding Against Oracle-Guided Attacks	. 794
 5D-3 (Time: 14:05 - 14:30) A Hybrid Machine Learning and Numeric Optimization Approach to Analog Circuit Deobfuscation	. 801
 5D-4 (Time: 14:30 - 14:55) RTLMarker: Protecting LLM-Generated RTL Copyright via a Hardware Watermarking Framework	. 808
5E (T4.1-2) AI-Driven Innovative Design Methods	
Time: 13:15 - 15:20. Wednesday. January 22, 2025	
Location: Innovation Hall	
Chair: Jaeduk Han (Hanyang Univ., Republic of Korea)	
 5E-1 (Time: 13:15 - 13:40) LIBMixer: An all-MLP Architecture for Cell Library Characterization towards Design Space Optimization	. 814
 5E-2 (Time: 13:40 - 14:05) DefectTrackNet: Efficient Root Cause Analysis of Wafer Defects in Semiconductor Manufacturing Using a Lightweight CNN Transformer Architecture	. 821
 5E-3 (Time: 14:05 - 14:30) Hybrid Compact Modeling Strategy: A Fully-Automated and Accurate Compact Model with Physical Consistency	. 828
$\mathbf{D}\mathbf{E}^{-4}$ (11110: 14:50 - 14:53)	

CAR-Net: Solving Electrical Crosstalk Problem in Capacitive Sensing Array	835
*Qinghang Zhao, Tao Li (Xidian Univ., China)	

5E-5 (Time: 14:55 - 15:20)

5F (DF-1) Quantum Computing

Time: 13:15 - 14:30, Wednesday, January 22, 2025

Organizer: Takatsugu Ono (Kyushu Univ., Japan), Chair: Chihiro Yoshimura (Hitachi, Japan)

5F-1 (Time: 13:15 - 13:40)

(Designers' Forum) Design of Superconducting Quantum Computers: Similarity and Dissimilarity *Yutaka Tabuchi (RIKEN Center for Quantum Computing, Japan)

5F-2 (Time: 13:40 - 14:05)

(Designers' Forum) Challenges in Developing Practical Qubit Control Systems *Takefumi Miyoshi (QuEL/QIQB Osaka Univ./e-trees.Japan, Japan)

5F-3 (Time: 14:05 - 14:30)

(Designers' Forum) A Layered Approach to Quantum Computing Software Platforms for the FTQC Era *Toru Kawakubo (QunaSys, Japan)

6A (SS-5) Beyond Digital: Advancing Design Automation for Physical Computing Systems

Time: 15:40 - 17:20, Wednesday, January 22, 2025

Location: Room Saturn

Chair: Antonino Tumeo (PNNL, USA)

6A-1 (Time: 15:40 - 16:05)

6B (T9-3) Floorplan and Placement

Time: 15:40 - 17:45, Wednesday, January 22, 2025

Location: Room Uranus

Chair: Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan)

6B-1 (Time: 15:40 - 16:05)

6B-2 (Time: 16:05 - 16:30)

ETAED: A East	(J-10.50) through Awara Electrolanner for Higrarchical Davian of Larga Scale SoCa	006
Zirui Li, Shixiong Kang Zha	*Kanglin Tian, Jianwang Zhai, Zixuan Li (Beijing Univ. of Posts and Telecommunications, China), Kai, Siyuan Xu (Huawei Noah's Ark Lab, China), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong), o (Beijing Univ. of Posts and Telecommunications, China)	500
6B-3 (Time: 16:3	30 - 16:55)	
Mixed-Size Plac *Cheng-Y Wang, Yao Taiwan)	cement Prototyping Based on Reinforcement Learning with Semi-Concurrent Optimization Zu Chiang, Yi-Hsien Chiang, Chao-Chi Lan, Yang Hsu, Che-Ming Chang, Shao-Chi Huang, Sheng-Hua o-Wen Chang (National Taiwan Univ., Taiwan), Hung-Ming Chen (National Yang Ming Chiao Tung Univ.,	893
6B-4 (Time: 16:5	55 - 17:20)	
ThePlace: Therr *Xinfei L Kong), So	nal-Aware Placement With Operator Learning-Based Ultra-Fast Simulator	900
6B-5 (Time: 17:2	20 - 17:45)	
An MIP-based F *Zewen L Univ./Sun	Force-directed Large Scale Placement Refinement Algorithm	907
6C (T13-	1) Let's Quantumize: Welcome to the World of Quantum	
Time:	15:40 - 16:55, Wednesday, January 22, 2025	
Location: 1	Room Venus	
Chairs:	Chun-Yi Lee (National Taiwan Univ., Taiwan), Ulf Schlichtmann (Tech. Univ. of Munich, Germany)	
60 1 (Times 15.4		
$IC-D^2S$ A Hybr	id Ising-Classical-Machines Data-Driven OUBO Solver Method	914
Armin Ab	bollahi, Mehdi Kamal, *Massoud Pedram (Univ. of Southern California, USA)	<i>,</i> ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
6C-2 (Time: 16:0)5 - 16:30)	
Compilation for Daniel Bo California	Dynamically Field-Programmable Qubit Arrays with Efficient and Provably Near-Optimal Scheduling Schen Tan (Univ. of California, Los Angeles/Harvard Univ., USA), Wan-Hsuan Lin, *Jason Cong (Univ. of a, Los Angeles, USA)	921
6C-3 (Time: 16:3	30 - 16:55)	
Back-end-aware *Mingfei Giovanni	Pault-tolerant Quantum Oracle Synthesis Yu, Alessandro Tempia Calvino (EPFL, Switzerland), Mathias Soeken (Microsoft Quantum, Switzerland), De Micheli (EPFL, Switzerland)	930
6D (T10-	1) Innovative Techniques for Energy-Efficient and Reliable Hardware Systems	
Time:	15:40 - 17:45, Wednesday, January 22, 2025	
Location: I	Room Mars/Mercury	
Chairs: 2	Zhiyao Xie (Hong Kong Univ. of Science and Tech., Hong Kong), Qi Sun (Zhejiang Univ., China), Shanshi Huang (Hong Kong Univ. of Science and Tech. (GZ), China)	

6D-1 (Time: 15:40 - 16:05)

6D-2 (Time: 16:05 - 16:30)

6D-3 (Time: 16:30 - 16:55)

Compact Interleaved Thermal Control for Improving Throughput and Reliability of Networks-on-Chip
 6D-4 (Time: 16:55 - 17:20) E-QUARTIC: Energy Efficient Edge Ensemble of Convolutional Neural Networks for Resource-Optimized Learning 959 Le Zhang, Onat Gungor, *Flavio Ponzina, Tajana Rosing (Univ. of California, San Diego, USA)
 6D-5 (Time: 17:20 - 17:45) Hardware Error Detection with In-Situ Monitoring of Control Flow-Related Specifications
6E (T4.1-3) Leveraging Large Language Models in Hardware Design
Time: 15:40 - 17:45, Wednesday, January 22, 2025
Location: Innovation Hall
Chair: Cong Hao (Georgia Tech, USA)
 6E-1 (Time: 15:40 - 16:05) LLSM: LLM-enhanced Logic Synthesis Model with EDA-guided CoT Prompting, Hybrid Embedding and AIG-tailored Acceleration
 6E-2 (Time: 16:05 - 16:30) OPL4GPT: An Application Space Exploration of Optimal Programming Language for Hardware Design by LLM
 6E-3 (Time: 16:30 - 16:55) Exploring Code Language Models for Automated HLS-based Hardware Generation: Benchmark, Infrastructure and Analysis 988 Jiahao Gai (Univ. of Cambridge/Imperial College London, UK), *Hao Chen (Imperial College London, UK), Zhican Wang (Shanghai Jiaotong Univ., China), Hongyu Zhou (Univ. of Sydney, Australia), Wanru Zhao, Nicholas Lane (Univ. of Cambridge, UK), Hongxiang Fan (Imperial College London/Univ. of Cambridge, UK)
6E-4 (Time: 16:55 - 17:20) MetRex: A Benchmark for Verilog Code Metric Reasoning Using LLMs
6E-5 (Time: 17:20 - 17:45)
SimEval: Investigating the Similarity Obstacle in LLM-based Hardware Code Generation
6F (DF-2) Advanced Sensor Technologies and Sensor Fusion

Time: 15:40 - 16:55, Wednesday, January 22, 2025

Organizer: Takashi Moue (Sony Semiconductor Solutions, Japan), Chair: Koichiro Yamashita (Fujitsu, Japan)

6F-1 (Time: 15:40 - 16:05)

(Designers' Forum) Human Sensing Using Millimeter Wave Radar

*Hongchun Li, Jun Tian, Qian Zhao, Lili Xie, Yingju Xia (Fujitsu Research & Development Center, China)

6F-2 (Time: 16:05 - 16:30)

(Designers' Forum) 3D-Stacked 1Megapixel Time-Gated SPAD Image Sensor with 2D Interactive Gating Network for Image Alignment-Free Sensor Fusion

Kazuhiro Morimoto, Naoki Isoda, Hiroshi Sekine, Tomoya Sasago, Yu Maehashi, Satoru Mikajiri, Kenzo Tojima, Mahito Shinohara, Ayman Abdelghafar, Hiroyuki Tsuchiya, Kazuma Inoue, Satoshi Omodani, *Kazuma Chida, Alice Ehara, Junji Iwata, Tetsuya Itano, Yasushi Matsuno, Katsuhito Sakurai, Takeshi Ichikawa (Canon, Japan)

6F-3 (Time: 16:30 - 16:55)

(Designers' Forum) 1.22µm-pixel Back-illuminated Stacked RGB Hybrid Event-based Vision Sensor

*Kazutoshi Kodama, Yusuke Sato, Yuhi Yorikado, Kyoji Mizoguchi, Takahiro Miyazaki, Masahiro Tsukamoto, Yoshihisa Matoba, Hirotaka Shinozaki, Atsumi Niwa, Tetsuji Yamaguchi (Sony Semiconductor Solutions, Japan), Christian Braendli (Sony Advanced Visual Sensing, Switzerland), Hayato Wakabayashi, Yusuke Oike (Sony Semiconductor Solutions, Japan)

3K Keynote Session III

Time: 9:00 - 9:45, Thursday, January 23, 2025

Location: Miraikan Hall

Chair: Atsushi Takahashi (Institute of Science Tokyo, Japan)

3K-1

(Keynote Address) In-Memory Computing-based Deep Learning Accelerators: An Overview and Future Prospects Abu Sebastian (IBM Research Europe - Zurich, Switzerland)

7A (T1-3) Accelerator Design Methodologies
Time: 10:05 - 11:45, Thursday, January 23, 2025
Location: Room Saturn
Chair: Yaoyao Ye (Shanghai Jiao Tong Univ., China)
7A-1 (Time: 10:05 - 10:30)
In-Storage Read-Centric Seed Location Filtering Using 3D-NAND Flash for Genome Sequence Analysis
7A-2 (Time: 10:30 - 10:55)
A Synthesis Methodology for Intelligent Memory Interfaces in Accelerator Systems
7A-3 (Time: 10:55 - 11:20)
Towards Efficient Data Parallelism on Spatial CGRA via Constraint Satisfaction and Graph Coloring
7A-4 (Time: 11:20 - 11:45)
 HyperG: Multilevel GPU-Accelerated k-way Hypergraph Partitioner
7B (T5-3) Advanced Architectures for Scientific and Edge Computing
Time: 10:05 - 11:45, Thursday, January 23, 2025
Location: Room Uranus
Chair: Hao Yu (SUSTech, China)
7B-1 (Time: 10:05 - 10:30)
Exploring and Exploiting Runtime Reconfigurable Floating Point Precision in Scientific Computing: a Case Study for Solving
PDEs
7B-2 (Time: 10:30 - 10:55)
A Holistic FPGA Architecture Exploration Framework for Deep Learning Acceleration
7B-3 (Time: 10:55 - 11:20)
OpenGeMM: A High-Utilization GeMM Accelerator Generator with Lightweight RISC-V Control and Tight Memory
Coupling
7B-4 (Time: 11:20 - 11:45)
Pointer: An Energy-Efficient ReRAM-based Point Cloud Recognition Accelerator with Inter-layer and Intra-layer Optimizations
*Qijun Zhang, Zhiyao Xie (Hong Kong Univ. of Science and Tech., Hong Kong)

7C (T6-2) The Science of Light: the New Advancement of Photonic Computing	
Time: 10:05 - 11:45, Thursday, January 23, 2025	
Location: Room Venus	
Chairs: Ryosuke Matsuo (Univ. of Tokyo, Japan), Yuanqing Cheng (Beihang Univ., China)	
7C-1 (Time: 10:05 - 10:30)	
An Efficient General-Purpose Optical Accelerator for Neural Networks	1070
7C-2 (Time: 10:30 - 10:55)	
Zero-Shot Automated Circuit Topology Search for Pareto-Optimal Photonic Tensor Cores	1077
7C-3 (Time: 10:55 - 11:20)	
Reuse and Blend: A Weight-Sharing Energy-Efficient Optical Neural Network	. 1084
7C-4 (Time: 11:20 - 11:45)	
PhotonGraph: High-performance Photonic Graph Processing Accelerator	1091
7D (T8-2) From Math to Circuits	
Time: 10:05 - 11:20, Thursday, January 23, 2025	
Location: Room Mars/Mercury	
Chairs: Oliver Keszöcze (Tech. Univ. of Denmark, Denmark), Yukio Miyasaka (UC Berkeley, USA)	
7D-1 (Time: 10:05 - 10:30)	
An Algebraic Approach to Partial Synthesis of Arithmetic Circuits	1097
7D-2 (Time: 10:30 - 10:55)	
Hardware Synthesizable Exceptions using Continuations	1104
7D-3 (Time: 10:55 - 11:20)	
 Area-Oriented Optimization After Standard-Cell Mapping *Andrea Costamagna, Alessandro Tempia Calvino (EPFL, Switzerland), Alan Mishchenko (UC Berkeley, USA), Giovanni De Micheli (EPFL, Switzerland) 	. 1112
7E (T4.2-3) Innovative Techniques in AI Model Optimization and Training	
Time: 10:05 - 11:20, Thursday, January 23, 2025	
Location: Innovation Hall	
Chairs: Dongsuk Jeon (Seoul National Univ., Republic of Korea), Ik-Joon Chang (Kyung Hee Univ.)	
7E-1 (Time: 10:05 - 10:30)	
ROBIN: A Novel Framework for Accelerating Robust Multi-Variant Training	1120
7E-2 (Time: 10:30 - 10:55)	
Dual-branch cross-modal fusion with local-to-global learning for UAV object detection	. 1126

Binyi Fang, *Yixin Yang, Jingjing Chang, Ziyang Gao, Hai-Bao Chen (Shanghai Jiao Tong Univ., China)

7E-3 (Time: 10:55 - 11:20)

H4H: Hybrid Convolution-Transformer Architecture Search for NPU-CIM Heterogeneous Systems for AR/VR Applications 1133 *Yiwei Zhao (Carnegie Mellon Univ., USA), Jinhui Chen (Reality Labs Research, Meta, USA), Sai Qian Zhang (New York Univ., USA), Syed Shakib Sarwar, Kleber Hugo Stangherlin, Jorge Tomas Gomez, Jae-Sun Seo, Barbara De Salvo, Chiao Liu (Reality Labs Research, Meta, USA), Phillip B. Gibbons (Carnegie Mellon Univ., USA), Ziyun Li (Reality Labs Research, Meta, USA)

7F (SS-6) Rapidus' Initiatives to Half Semiconductor Development Time	
Time: 10:05 - 11:20, Thursday, January 23, 2025	
Chair: Koki Tsurusaki (Rapidus, Japan)	
7F-1 (Time: 10:05 - 10:30)	
(Invited Paper) Raads: Rapidus's AI/ML based assisted design flow to reduce design period halved	1142
7F-2 (Time: 10:30 - 10:55)	
(Invited Paper) DMCO: A Strategy for Design-Manufacturing Co-optimization	1143
7F-3 (Time: 10:55 - 11:20)	
(Invited Paper) Advanced Packaging Technology and Design Methodology for Next Generation Chiplets	. 1144
8A (T1-4) System Level Modelling & Optimization	
Time: 13:15 - 14:55, Thursday, January 23, 2025	
Location: Room Saturn	
Chair: Zhe Lin (Sun Yat-sen Univ., China)	
8A-1 (Time: 13:15 - 13:40)	
FirePower: Towards a Foundation with Generalizable Knowledge for Architecture-Level Power Modeling	. 1145
8A-2 (Time: 13:40 - 14:05)	
DISS: A Novel Data Invalidation Scheme for Swap-Data on Flash Storage Systems	1153
8A-3 (Time: 14:05 - 14:30)	
Response Range Optimization for Run-Time Requirement Enforcement on MPSoCs	1160
8A-4 (Time: 14:30 - 14:55)	
TL-CSE: Microarchitecture-Compiler Co-design Space Exploration via Transfer Learning	. 1167
8B (T5-4) Emerging Trends in Reconfigurable and Compute-in-Memory	
Time: 13:15 - 14:55, Thursday, January 23, 2025	
Location: Room Uranus	
Chair: Guohao Dai (Shanghai Jiao Tong Univ., China)	
8B-1 (Time: 13:15 - 13:40)	

*Gunil Kang (Korea Univ. & Samsung Electronics, Republic of Korea), Dahoon Park, Hojin Lee (Korea Univ., Republic of Korea), Sangwoo Jung (DGIST, Republic of Korea), Jiyong Park (Korea Univ., Republic of Korea), Jung Gyu Min, Youngjoo Lee (POSTECH, Republic of Korea), Jaeha Kung (Korea Univ., Republic of Korea)

8B-2 (Time: 13:40 - 14:05) *Shaobo Ma, Chao Fang, Haikuo Shao, Zhongfeng Wang (Nanjing Univ., China) 8B-3 (Time: 14:05 - 14:30) *Thinh Nguyen Quang, Kosuke Matsuyama, Keisuke Shimizu, Hiroki Sugano, Eiji Kurimoto (Sharp, Japan), Hasitha Muthumala Waidyasooriya, Masanori Hariyama, Masayuki Ohzeki (Tohoku Univ., Japan) 8B-4 (Time: 14:30 - 14:55) Pol Puigdemont (Univ. Politècnica de Catalunya (UPC), Spain), *Enrico Russo (Univ. of Catania, Italy), Axel Wassington, Abhijit Das, Sergi Abadal (Univ. Politècnica de Catalunya (UPC), Spain), Maurizio Palesi (Univ. of Catania, Italy) 8C (T3-4) Adaptive and Flexible Memory Architecture 13:15 - 14:55, Thursday, January 23, 2025 Time: Location: Room Venus Chair: Chao Wu (Nanjing Univ. of Science and Tech., China) 8C-1 (Time: 13:15 - 13:40) FPBA: Flexible Percentile-Based Allocation for Multiple-Bits-Per-Cell RRAM1202 *Junfei Liu (Univ. of Rochester/Univ. of California, San Diego, USA), Anson Kahng (Univ. of Rochester, USA) 8C-2 (Time: 13:40 - 14:05) Mpache: Interaction Aware Multi-level Cache Bypassing on GPUs1209 *Mengyue Xi, Tianyu Guo, Xuanteng Huang, Zejia Lin, Xianwei Zhang (Sun Yat-sen Univ., China) 8C-3 (Time: 14:05 - 14:30) Cheng-Yen Lee, *Sunil P. Khatri (Texas A&M Univ., USA), Ali Ghrayeb (Texas A&M Univ. at Qatar, Qatar) 8C-4 (Time: 14:30 - 14:55) TRIFP-DCIM: A Toggle-Rate-Immune Floating-point Digital Compute-in-Memory Design with Adaptive-Asymmetric Xing Wang, Tianhui Jiao, Shaochen Li, Yuchen Ma, *Zhican Zhang, Zhichao Liu, Xi Chen, Xin Si (Southeast Univ., China)

8D (T9-4) Reliability in Physical Design

13:15 - 14:55, Thursday, January 23, 2025 Time:

Location: Room Mars/Mercury

Wenjian Yu (Tsinghua Univ., China) Chair:

8D-1 (Time: 13:15 - 13:40)

*Yichen Cai, Linyu Zhu (Shanghai Jiao Tong Univ., China), Xinfei Guo (Shanghai Jiao Tong Univ./State Key Laboratory of Integrated Chips and Systems (SKLICS), China)

8D-2 (Time: 13:40 - 14:05)

*Man-Ling Hong, Ying-Jie Jiang, Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan)

8D-3 (Time: 14:05 - 14:30)

Jiun-Cheng Tsai, *Hsuan-Ming Huang, Wei-Min Hsu, Pei-Ting Lee, Jen-Hang Yang, Heng-Liang Huang (MediaTek, Taiwan), Yen-Ju Su, Charles H. -P. Wen (NYCU, Taiwan)

8D-4 (Time: 14:30 - 14:55)

8E (SS-7) Hardware Authenticity towards a Trustworthy Society

Time: 13:15 - 14:55, Thursday, January 23, 2025

Location: Innovation Hall

Chairs: Jun Shiomi (Osaka Univ., Japan), Michihiro Shintani (Kyoto Inst. of Tech., Japan)

8E-1 (Time: 13:15 - 13:40)

8E-2 (Time: 13:40 - 14:05)

8E-3 (Time: 14:05 - 14:30)

(Invited Paper) Current Consumption Model for More Efficient Side-channel Tolerant Design at FPGA Design Stage 1270 *Daisuke Fujimoto, Yuichi Hayashi (NAIST, Japan)

8E-4 (Time: 14:30 - 14:55)

8F (DF-3) Extending the Limits of Classical Computers using Emerging Device and Circuit Technology

Time: 13:15 - 14:30, Thursday, January 23, 2025

Organizer: Chihiro Yoshimura (Hitachi, Japan), Chair: Takatsugu Ono (Kyushu Univ., Japan)

8F-1 (Time: 13:15 - 13:40)

(Designers' Forum) Amorphica: Fully Connected Metamorphic Annealing Processor with Programmable Optimization Strategy

*Kazushi Kawamura (Institute of Science Tokyo, Japan), Jaehoon Yu (Samsung Advanced Inst. of Tech., Republic of Korea), Daiki Okonogi, Satoru Jimbo, Genta Inoue, Akira Hyodo (Institute of Science Tokyo, Japan), Ángel López García-Arias (NTT, Japan), Kota Ando, Bruno Hideki Fukushima-Kimura (Hokkaido Univ., Japan), Ryota Yasudo (Kyoto Univ., Japan), Thiem Van Chu, Masato Motomura (Institute of Science Tokyo, Japan)

8F-2 (Time: 13:40 - 14:05)

(Designers' Forum) Nanophotonic Devices toward Opto-Electronic Accelerator

*Akihiko Shinya (NTT, Japan)

8F-3 (Time: 14:05 - 14:30)

(Designers' Forum) Highly Energy-Efficient Processing by Controlling Flexibility of Information Carrier using Superconductor Half-Flux Quantum Logic

*Masamitsu Tanaka (Nagoya Univ., Japan)

9A (T12-3) Homomorphic Encryption and Cloud Security	
Time: 15:20 - 17:30 Thursday January 23 2025	
Location: Poom Saturn	
Chairse Junches Les (Korse Univ. Depublie of Korse) Viran Chen (Duke Univ. USA)	
Chairs. Junghee Lee (Korea Univ., Republic of Korea), Tiran Chen (Duke Univ., USA)	
9A-1 (Time: 15:20 - 15:45)	
Efficient and Secure Cloud-based Split Logic Synthesis Chaitali Sathe, Yiorgos Makris, *Benjamin Carrion Schafer (Univ. of Texas, Dallas, USA)	. 1282
9A-2 (Time: 15:45 - 16:10)	
Efficient Key Switching Accelerator for Fully Homomorphic Encryption	. 1288
9A-3 (Time: 16:10 - 16:35)	
The Unlikely Hero: Nonidealities in Analog Photonic Neural Networks as Built-in Adversarial Defenders	. 1295
9A-4 (Time: 16:35 - 17:00)	
Low Multiplicative Depth Polynomial Evaluation Architectures for Homomorphic Encrypted Data	1302
9A-5 (Time: 17:00 - 17:25)	
PRICING: Privacy-Preserving Circuit Data Sharing Framework for Lithographic Hotspot Detection Chen-Chia Chang (Duke Univ., USA), Wan-Hsuan Lin (UCLA, USA), Jingyu Pan, Guanglei Zhou (Duke Univ., USA), Zhiyao Xie (HKUST, Hong Kong), Jiang Hu (TAMU, USA), *Yiran Chen (Duke Univ., USA)	1308
9B (T11-2) Advanced Modeling, Simulation, and Verification	

Time:15:20 - 17:30, Thursday, January 23, 2025Location:Room UranusChair:Yutaka Masuda (Nagoya Univ., Japan)

9B-1 (Time: 15:20 - 15:45)

9B-2 (Time: 15:45 - 16:10)

9B-3 (Time: 16:10 - 16:35)

9B-4 (Time: 16:35 - 17:00)

9B-5 (Time: 17:00 - 17:25)

9C (T13-2) Carbon, Light, Fluids: Emerging Technologies

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Room Venus

Chairs: Krishnendu Chakrabarty (Arizona State Univ., USA), Yangdi Lyu (HKUST (GZ), China)

9C-1 (Time: 15:20 - 15:45)

CACTI-CNFET: an Analytical Tool for Timing, Power, and Area of SRAMs with Carbon Nanotube Field Effect Transistors . 1350 *Shinobu Miwa, Eiichiro Sekikawa, Tongxin Yang (Univ. of Electro-Communications, Japan), Ryota Shioya (Univ. of Tokyo, Japan), Hayato Yamaki, Hiroki Honda (Univ. of Electro-Communications, Japan)

9C-2 (Time: 15:45 - 16:10)

9C-3 (Time: 16:10 - 16:35)

9C-4 (Time: 16:35 - 17:00)

A Backup Resource Customization and Allocation Method for Wavelength-Routed Optical Networks-on-Chip Topologies ...1372 *Zhidan Zheng, You-Jen Chang, Liaoyuan Cheng, Tsun-Ming Tseng, Ulf Schlichtmann (Tech. Univ. of Munich, Germany)

9C-5 (Time: 17:00 - 17:25)

9D (T10-2) Advanced Techniques for Power Optimization and IR Prediction

Time: 15:20 - 17:30, Thursday, January 23, 2025

Location: Room Mars/Mercury

Chairs: Bei Yu (Chinese Univ. of Hong Kong, Hong Kong), Yu-Guang Chen (National Central Univ., Taiwan), Hongce Zhang (Hong Kong Univ. of Science and Tech. (GZ), China)

9D-1 (Time: 15:20 - 15:45)

*Yikang Ouyang, Yuchao Wu, Dongsheng Zuo (Hong Kong Univ. of Science and Tech. (GZ), China), Subhendu Roy (Cadence Design Systems, USA), Tinghuan Chen (The Chinese Univ. of Hong Kong, Shenzhen, China), Zhiyao Xie (Hong Kong Univ. of Science and Tech., Hong Kong), Yuzhe Ma (Hong Kong Univ. of Science and Tech. (GZ), China)

9D-3 (Time: 16:10 - 16:35)

9D-4 (Time: 16:35 - 17:00)

9D-5 (Time: 17:00 - 17:25)

*Vincent Meyers (Karlsruhe Inst. of Tech., Germany), Michael Hefenbrock (RevoAI GmbH, Germany), Mahboobe Sadeghipourrudsari, Dennis Gnad, Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany)

9E (SS-8) Innovations and Challenges on Cryo-CMOS Devices, Circuits and Design
Platforms
Time: 15:20 - 17:30, Thursday, January 23, 2025
Location: Innovation Hall
Chairs: Chika Tanaka (KIOXIA/Kyoto Inst. of Tech., Japan), Nobuyuki Momo (KIOXIA, Japan)
9E-1 (Time: 15:20 - 15:45)
 (Invited Paper) Physics-based Modeling to Extend a MOSFET Compact Model for Cryogenic Operation
9E-2 (Time: 15:45 - 16:10)
(Invited Paper) Cryo-Compact Modeling Based on Sparse Gaussian Process
9E-3 (Time: 16:10 - 16:35)
(Invited Paper) Re-Consideration of Correlation Between Interface States and Bulk Traps Using Cryogenic Measurement 1432 *Yuichiro Mitani, Tatsuya Suzuki, Yohei Miyaki (Tokyo City Univ., Japan)
9E-4 (Time: 16:35 - 17:00)
(Invited Paper) Random Telegraph Noise Observed on 65-nm Bulk pMOS Transistors at 3.8K
9E-5 (Time: 17:00 - 17:25)
(Invited Paper) Cryo-CMOS Analog Circuits for Spin Qubit Control
9F (DF-4) Integrated Circuit Design Methodologies using Open Source and Artificial

Intelligence

Time: 15:20 - 16:35, Thursday, January 23, 2025

Organizer: Hiroyuki Uzawa (NTT, Japan), Chair: Takeshi Kuboki (Kumamoto Univ., Japan)

9F-1 (Time: 15:20 - 15:45)

(Designers' Forum) A Challenge to Tape-Out in Open-Source Era *Akira Tsuchiya (Univ. of Shiga Prefecture, Japan)

9F-2 (Time: 15:45 - 16:10)

(Designers' Forum) Analog Design Democratization for Small Volume LSI Fabrication *Seijiro Moriyama (Anagix, Japan), Shingo Ura, Tadaaki Tsuchiya (Logic Research, Japan)

9F-3 (Time: 16:10 - 16:35)

(Designers' Forum) Automatic Design of an Analog Integrated Circuits using AI *Nobukazu Takai (Kyoto Inst. of Tech., Japan)

Information

Proceedings:

ASP-DAC 2025 will be providing an authority to access the download site for the conference proceedings. Conference registration in any of the categories will include it. The site will be open on Jan. 20, 2025. Please note that neither CD-ROM nor USB memory are provided.

Banquet:

Conference in-person registrants are invited to attend a banquet to be held on January 22, 2025. The banquet will be held from 18:30 to 20:30 at the Hilton Tokyo Odaiba 1F "Room Pegasus". Regular Member and Non-member Conference in-person registrants receive a ticket to the banquet when they register at the conference.

Free Water:

The conference venue (Miraikan) has water dispensers, so that you can drink water freely. We hope you to enjoy Japanese pure water.

Free WiFi:

Free WiFi internet service is also provided. Instruction how to connect to WiFi is put on the wall in the venue.

Free Bus Tour:

Tokyo Convention & Visitors Bureau is offering complimentary programs specially tailored to provide overseas registered participants with various experiences of Tokyo and its vicinity; from nature and culture to other attractions. Please ask Tokyo Convention & Visitors Bureau at the registration desk for more details on the tour.

Insurance:

The organizer cannot accept responsibility for accidents that might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Tokyo Odaiba Waterfront during the period of the Conference ranges between 3 degrees Celsius and 10 degrees Celsius.

Currency Exchange:

Only Japanese Yen (JPY, Ξ) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Tipping:

In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:

Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.

*Eastern Japan : Tokyo, Yokohama, Tohoku, Hokkaido

**Western Japan :Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:

The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Prayer Room:

There is a prayer room in the conference venue (5F of Miraikan). Please feel free to contact the registration desk if you would like to use it.

Nursing Room:

There is a nursing room in the conference venue (5F of Miraikan). Please feel free to contact the registration desk if you would like to use it.

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Invitation to ASP-DAC 2026

On behalf of the Organizing Committee, it is our great pleasure and honor to invite you to the 31st ASP-DAC, to be held in the vibrant city of Hong Kong from January 19-22, 2026.

Hong Kong, known as "Asia's World City," is a dynamic metropolis where East meets West, offering a unique mix of tradition, innovation, and breathtaking scenery. With world-class infrastructure, state-of-the-art conference facilities, and unmatched hospitality, Hong Kong is the perfect destination for this prestigious event.

The conference will be held at the **Hong Kong Disneyland Hotel**, a venue that seamlessly combines sophistication, modern amenities, and the enchanting charm of Disney. Conveniently located just a 15-minute drive from Hong Kong International Airport, the hotel is easily accessible and well-connected through an efficient public transportation network, ensuring a hassle-free journey for all attendees.

Beyond the conference, we encourage you to explore Hong Kong's diverse attractions. From the bustling streets of Central and the shopping paradise of Tsim Sha Tsui to the tranquil beauty

of Victoria Harbour and the panoramic views from Victoria Peak, there's something for everyone. Don't miss the chance to enjoy Hong Kong's world-famous culinary scene, which spans everything from Michelin-starred restaurants to authentic local street food.

ASP-DAC 2026 will provide an excellent platform for exchanging ideas and advancing technologies in electronic design automation and embedded systems. Your active participation and submissions are key to shaping an outstanding technical program and fostering meaningful collaborations.

We look forward to welcoming you to Hong Kong, where innovation meets inspiration, and tradition blends seamlessly with modernity. Let's make ASP-DAC 2026 a truly memorable event in this remarkable city!

Tsung-Yi Ho General Chair, ASP-DAC 2026