

# Call for Participation



**Date:** Jan. 19-22, 2026

**Place:** Hong Kong Disneyland Hotel

**Early Registration Due:** Friday, December 12, 2025 (AOE)

**Registration Site:** <https://www.aspdac.com/aspdac2026/reg>

## Aims of the Conference

ASP-DAC is the largest conference in Asia and South-Pacific regions on Electronic Design Automation (EDA) area for VLSI and systems. ASP-DAC has been started at 1995 and this ASP-DAC 2026 is 31st conference. ASP-DAC 2026 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas by technical papers and tutorials. ASP-DAC also holds Designers' Forum to make presentations about the latest designs for designers. Please do not miss ASP-DAC 2026.

## Features of ASP-DAC 2026

### ■ Keynote Speeches

- 1. January 20: Chenming Hu** (University of California, Berkeley), “FinFET - from Lab to Foundry to EDA/Fabless”; **Yiran Chen** (Duke University), “Edge AI: Everything, Everywhere, All at Once”; **Patrick Groeneveld** (Stanford University), “When Moore Surpasses Mind: The Impact of 6 decades of Relentless Design Automation”
- 2. January 21: Yuan Xie** (Hong Kong University of Science and Technology), “From 2D IC to 3D IC and Chiplet : A Retrospective View”; **Charles Alpert** (Cadence Design Systems, Inc.), “Harnessing Agentic AI to Accelerate Designer Productivity”
- 3. January 22: Jim Chang** (3DIC Design Methodology Development, TSMC), “Unlocking Hyper-Scale AI: Navigating the Future of 3DIC Design Solutions”; **Takefumi Miyoshi** (e-trees.Japan, Inc., The University of Osaka, QuEL, Inc.), “Design and Implementation of Control System for Quantum Computers”

### ■ Tutorials

ASP-DAC 2026 offers attendees a set of 3 hours intense introductions to specific topics. If you register for the conference, you have the option to select two out of the six topics.

**Tutorial-1:** On-Device AI to Better Mobile and Implantable Devices in Healthcare

**Tutorial-2:** Design Methodologies and Toolchains for Compute-in-Memory: From Architectures to Systems

**Tutorial-3:** Design Automation for the Early Fault Tolerant Quantum Computing

**Tutorial-4:** Bi-Directional Synergy: A Tutorial on Hardware Design for Agentic AI and Agentic AI for Hardware Design

**Tutorial-5:** APS: An MLIR-Based Hardware-Software Co-design Framework for Agile Processor Specialization

**Tutorial-6:** Post-Silicon Validation & Hardware Security in Modern Processors

### ■ Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA academia/developers. This forum will take place on January 21 and 22. This year has 4 oral sessions:

**Designer Forum 1:** Toward Autonomous Chip Design: From Foundation Models to Agentic EDA;

**Designer Forum 2:** AI in Production EDA: Digital, Custom, and Manufacturing Use Cases;

**Designer Forum 3:** Chiplets Go Mainstream: Design Automation for 2.5D/3D Systems;

**Panel:** AI Accelerators at a Crossroads: Who Will Power the Next Decade of AI?

### ■ University LSI Design Contest

In University LSI Design Contest, state-of-the-art LSI and/or system designs compete on their design excellence and implementation quality. 7 high-quality designs all including actual measurement proof will be introduced at the design contest session on **January 20**.

### ■ Technical Sessions

There are 187 high quality papers selected from 625 submissions. We also plan 6 special sessions: “100 Years of the FET: From Technology Foundations to EDA Innovation”, “From Uniform to Adaptive: The Precision-Scalable Computing Era for Edge Intelligence”, “Design Automation for Quantum Error Correction: From Algorithms to Architectures”, “Advances in AI-Driven Circuit Verification and Reliability Analysis”, “Toward Fully Automated DTCO: ML Frameworks across Technology, Cell, and Library Layers”, “From Solvers to Layout: Cross-Layer Approaches for Reliable and Scalable IC Design”

**Sponsored by:** SIGDA, CEDA, IEEE

**Supported by:** Huawei, Cadence, Synopsys, Infinigence, Amedac, Shanghai LEDA Technology, MediaTek, Siemens, Empyrean, Primarius, Footprintku, Xpedic, The Hong Kong University of Science and Technology (Guangzhou), The Chinese University of Hong Kong

**Conference Secretariat**  
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