ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

ASP-DAC 2026

31st Asia and South Pacific Design Automation Conference

Date: January 19-22, 2026 Place: Hong Kong Disneyland Hotel

FINAL PROGRAM

Sponsored by

SIGDA (acm) CEDA IEEE Council on Electronic Design Automation CAS

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XPEEDIC ACCELERATE YOUR IC DESIGN 芯和半导体 Easylogic 香港科技大学（广州） THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY (GUANGZHOU)

香港中文大學 The Chinese University of Hong Kong

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Welcome to ASP-DAC 2026

Welcome to ASP-DAC 2026 — the 31st Asia and South Pacific Design Automation Conference

It is our great pleasure to welcome you to ASP-DAC 2026, held from January 19 to 22, 2026, at the Hong Kong Disneyland Hotel. This year marks the 31st edition of ASP-DAC, the premier international forum in the Asia and South Pacific region for research, development, and innovation in electronic design automation (EDA) and VLSI systems. Hosting ASP-DAC in Hong Kong reflects the region's vibrant semiconductor ecosystem and its growing role in shaping the future of design technologies.

ASP-DAC brings together researchers, practitioners, and industry leaders from around the world to exchange ideas, present high-impact research, and explore emerging directions in design automation and system design. The conference serves as a unique platform for fostering collaboration across academia and industry, while advancing both foundational research and real-world applications.

ASP-DAC 2026 features a rich and diverse technical program, including peer-reviewed papers covering the full spectrum of EDA and system design, one panel, three designers' forums, six tutorials, six special sessions, the Student Research Forum, and the University LSI Design Contest. To commemorate the milestone of 100 Years of the Field-Effect Transistor (FET100), we are honored to host the CEDA-EDS Special Session: "100 Years of the FET: From Technology Foundations to the EDA Ecosystem," highlighting the profound and lasting impact of the FET on modern electronics and design automation.

We are also delighted to present an outstanding keynote program featuring seven distinguished speakers from academia and industry. Their talks span a broad range of timely and forward-looking topics, including FinFET technology, edge AI, large-scale design automation, chiplets and 3D integration, agentic AI for designer productivity, hyper-scale AI systems, and control systems for quantum computers. These keynotes will provide valuable perspectives on how EDA continues to evolve in response to emerging technologies and application demands.

The success of ASP-DAC depends on the active participation of its community. We hope this conference provides a stimulating environment to reconnect with colleagues, build new collaborations, and exchange ideas that will shape the future of EDA and system design.

We also invite you to enjoy Hong Kong, a dynamic international city where innovation, culture, and tradition come together, and to make the most of your time here beyond the technical sessions.

Finally, we sincerely thank our sponsors, organizing and technical program committees, and the many volunteers whose dedication and hard work have made ASP-DAC 2026 possible.

Welcome to ASP-DAC 2026. We wish you a productive, inspiring, and memorable conference.

Tsung-Yi Ho
General Chair, ASP-DAC 2026

Message from the Technical Program Committee

On behalf of the Technical Program Committee (TPC), it is our great pleasure to welcome you to the 31st Asia and South Pacific Design Automation Conference (ASP-DAC) 2026. We are delighted to host this year's ASP-DAC from January 19 to 22, 2026, at the magical Hong Kong Disneyland in Hong Kong.

The ASP-DAC 2026 call for papers adopted a comprehensive two-step process: abstract registration, followed by full manuscript submission. We received a total of 749 abstracts from 34 countries and regions. Of these, 639 full manuscripts were submitted, and 612 advanced to the review stage. The number of full manuscript submissions marked a record high, approximately a 19% increase compared with last year. This remarkable growth underscores the continued vitality and expanding influence of our research community. While the largest number of submissions came from Asia, we also received strong contributions from North America and Europe. As machine learning-based and AI-assisted design have become increasingly prevalent, papers on AI/LLM-assisted tools and design methodologies were directed to their respective tracks to ensure expert and design-phase-appropriate review. Consequently, the "Hardware Systems and Architectures for AI" and "Physical Design and Timing Analysis" tracks emerged as the most popular this year.

Alongside sustained strong submissions in core EDA topics, such as logic synthesis, physical design, analog-mixed signal design including RF and photonic, system-level modeling, testing, simulation, design for manufacturability and reliability, we also received substantial contributions in hardware systems and related areas. In particular, the "Memory Architecture and Near/In Memory Computing" and "Hardware and Embedded Security" tracks attracted a very large number of submissions. Emerging computing paradigms, including near-/in-memory computing, approximate and bio-inspired computing, and quantum computing, continue to draw significant interest from contributing authors, and these are likely to become important drivers for ASP-DAC in the future. These trends demonstrate how ASP-DAC continues to showcase and connect with state-of-the-art research across both academia and industry.

The TPC consisted of 176 leading experts in EDA, IC design, embedded systems, memory architectures, hardware security, emerging technologies, and AI/ML systems, organized into 13 subcommittees. The paper review process was conducted with fairness and rigor through a strict double-blind policy and careful management of conflicts of interest. We held a face-to-face and partially hybrid TPC meeting at the Yoshida Campus of Kyoto University in Kyoto, Japan, on August 29, 2025. From the 612 reviewed submissions, 176 high-quality regular papers were selected, yielding an acceptance rate of 28.7%. This reflects ASP-DAC's continued commitment to maintaining premier technical excellence.

The full conference program comprises regular papers, keynote speeches, and a strong set of special sessions, designers' forums, and design contest sessions. As in previous years, tutorials are offered on the first day, followed by three days of regular programs arranged into six parallel tracks. Each morning begins with two keynote speeches that set the tone for the day's technical activities. Among the accepted regular papers, 14 were nominated by the subcommittees for the Best Paper Award. These nominees were thoroughly evaluated by the Best Paper Award Committee, chaired by Vice Technical Program Chair Prof. Seokhyeong Kang, and two papers were ultimately selected. Prof. Kang also chaired the 10-Year Retrospective Most Influential Paper selection committee, selecting one influential paper from the proceedings of the 21st ASP-DAC in 2016.

The exciting and stimulating technical program of ASP-DAC 2026 is the result of the dedicated efforts of our authors, reviewers, invited speakers, and TPC members. We extend our heartfelt gratitude to all of them. We especially thank our TPC Secretaries, Hiromitsu Awano and Jun Shiomi; the Conference Secretary, Bei Yu; the Publication Chair, Nan Guan; and the Publicity Chair, Ngai Wang, for their outstanding support. We also deeply appreciate the assistance of Sophie Guan and Joyce Zhong in managing the paper submission and review process, as well as the review management system. Finally, our deepest thanks go to the entire Organizing Committee for their exceptional work in preparing an excellent conference.

We sincerely hope you enjoy the ASP-DAC 2026 technical program and look forward to welcoming you in Hong Kong.

Takashi Sato
Technical Program Chair, ASP-DAC 2026

Takashi Sato

Session Schedule

Monday, January 19, 2026

Sleeping Beauty 1/2	Sleeping Beauty 3	Sleeping Beauty 5
Tutorial-1 On-Device AI to Better Mobile and Implantable Devices in Healthcare 09:00-12:00	Tutorial-2 Design Methodologies and Toolchains for Compute-in-Memory: From Architectures to Systems 09:00-12:00	Tutorial-3 Design Automation for the Early Fault Tolerant Quantum Computing 09:00-12:00
Coffee Break 12:00-14:00		
Tutorial-4 Bi-Directional Synergy: A Tutorial on Hardware Design for Agentic AI and Agentic AI for Hardware Design 14:00-17:00	Tutorial-5 APS: An MLIR-Based Hardware-Software Co-design Framework for Agile Processor Specialization 14:00-17:00	Tutorial-6 Post-Silicon Validation & Hardware Security in Modern Processors 14:00-17:00

Tuesday, January 20, 2026

Cinderella Ballroom 1/6/7/8					
Opening 08:05-08:20					
Keynote I: Prof. Chenming Hu (University of California, Berkeley) 08:20-09:05					
Keynote II: Prof. Yiran Chen (Duke University) 09:05-09:50					
Coffee Break 09:50-10:20					
Snow White 1	**Snow White 2**	**Snow White 3**	**Sleeping Beauty 1/2**	**Sleeping Beauty 3**	**Sleeping Beauty 5**
1A (T4-C) AI Applications for Edge and Domain-Specific Systems 10:20-12:00	1B (SS-4) Toward Fully Automated DTCO: ML Frameworks across Technology, Cell, and Library Layers 10:20-11:35	1C (T12-D) Physical Attacks and Countermeasures 10:20-12:00	1D (SS-2) Design Automation for Quantum Error Correction: From Algorithms to Architectures 10:20-12:00	1E (T11-A) Ensuring High Quality Designs through Simulation and Verification Advances 10:20-11:35	1F (T7-A) Efficient Design of Spiking Neural Network Accelerators 10:20-12:00
Lunch & CEDA Distinguish Lecture 12:00-13:30					
Luncheon Talk: Dr. Patrick Groeneveld (AMD) 12:30-13:15					
2A (T5-B) Vision and Transformer Acceleration Architectures 13:30-15:35	2B (CEDA-EDS Special Session: 100 Years of the FET: From Technology Foundations to the EDA Ecosystem) 13:30-15:35	2C (T13-B) From HDL to Hardware: Scalable Design Automation for Quantum Computing 13:30-15:35	2D University Design Contest 13:30-15:35	2E (T10-A) Reliability-Driven and Low-Power Design 13:30-15:35	2F (T8-C) Application of Generative and Predictive Methods to Design Optimization 13:30-15:35
Coffee Break & University LSI Design Contest Poster Session 15:35-15:55					
3A (T5-A) Advanced Accelerators for Emerging AI Workloads 15:55-18:00	3B (T1-C) Advances in Agile Design Acceleration 15:55-18:00	3C (T13-A) Beyond Silicon: Emerging Paradigms in EDA for Atomic Scale Computing, Photonics, and Microfluidics 15:55-18:00	3D (SS-3) Advances in AI-Driven Circuit Verification and Reliability Analysis 15:55-17:35	3E (T9-E) Timing Analysis and Timing-Aware Physical Synthesis 15:55-18:00	3F (T8-B) Advanced Performance Optimization for High-level Synthesis and Scheduling 15:55-18:00
ACM SIGDA Student Research Forum at ASP-DAC 2026 @ Cinderella Ballroom 2//3/5 18:15-20:15					

Wednesday, January 21, 2026

Cinderella Ballroom 1/6/7/8					
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Keynote IV: Dr. Charles Alpert (Cadence) 09:05-09:50					
Coffee Break 09:50-10:20					
Snow White 1	**Snow White 2**	**Snow White 3**	**Sleeping Beauty 1/2**	**Sleeping Beauty 3**	**Sleeping Beauty 5**
4A (T4-B) AI for Hardware, Systems, and Verification 10:20-12:00	4B (T3-D) Accelerating LLMs with Near- and In-Memory Computing 10:20-12:00	4C (T11-C) Tackling Reliability Issues across the Layers 10:20-11:35	4D (SS-1a) Mixed-precision: Silicon-to-Model Turbo Knob 10:20-11:35	4E (T10-B) Explainable and Generative AI for Lithography and Yield Optimization 10:20-12:00	4F (T6-B) Smart Techniques for Analog & Mixed-Signal Design 10:20-11:35
Lunch & Invited Talk 12:00-13:30					
5A (T3-B) Emerging Memory Architectures and Their Applications 13:30-15:35	5B (SS-1b) From Uniform to Adaptive: The Precision-Scalable Computing Era for Edge Intelligence 13:30-14:45	5C (T12-C) System-Level Security and Secure Communication 13:30-15:35	5D (Designer Forum 1) Toward Autonomous Chip Design: From Foundation Models to Agentic EDA 13:30-15:35	5E (T9-D) Performance-Driven Floorplanning and Global Placement 13:30-15:35	5F (T8-A) Advances in Logic Optimization and Technology Mapping 13:30-15:35
Coffee Break 15:35-15:55					
6A (T3-C) Circuit- and Device-Aware Design for CIM 15:55-18:00	6B (T1-B) Accelerator and mapping innovations for LLMs and Neural Networks 15:55-18:00	6C (T12-B) Logic Locking and Hardware Trojan Detection 15:55-18:00	6D (Designer Forum 2) AI in Production EDA: Digital, Custom, and Manufacturing Use Cases 15:55-17:35	6E (T9-C) Cell Placement and Generation for Advanced Technologies 15:55-18:00	6F (T5-E) Hardware-Software Co-Design and Optimization Frameworks 15:55-18:00
Banquet 18:30-20:30					

Thursday, January 22, 2026

Cinderella Ballroom 1/6/7/8					
Keynote V: Dr. Chih-Wei Jim Chang (TSMC) 08:20-09:05					
Keynote VI: Dr. Takefumi Miyoshi (e-trees.Japan, Inc. & QuEL & The University of Osaka) 09:05-09:50					
Coffee Break 09:50-10:20					
Snow White 1	**Snow White 2**	**Snow White 3**	**Sleeping Beauty 1/2**	**Sleeping Beauty 3**	**Sleeping Beauty 5**
7A (T4-A) Efficient AI Model Design and Training 10:20-12:00	7B (T2-B) Designing Predictable and Reliable Real-Time Systems 10:20-12:00	7C (T11-B) Scaling up Physical Design Optimization to Heterogeneous Systems 10:20-11:35	7D (SS-5) From Solvers to Layout: Cross-Layer Approaches for Reliable and Scalable IC Design 10:20-12:00	7E (T7-B) Emerging Computing Architectures and Learning Systems 10:20-12:00	7F (T6-A) RF and Photonic IC 10:20-12:00
Lunch & Invited Talk 12:00-13:30					
8A (T3-A) Hybrid CIM Architectures and Flexible Dataflows 13:30-15:35	8B (T1-A) Exploring interconnect design, power modeling, and system prototyping 13:30-15:35	8C (T12-A) Privacy-Preserving & Secure AI Computation 13:30-15:35	8D (Designer Forum 3) Chiplets Go Mainstream: Design Automation for 2.5D/3D Systems 13:30-15:35	8E (T9-B) Advances in Routing for Chips and Advanced Packaging 13:30-15:35	8F (T5-D) Memory-Centric and Compute-in-Memory Innovations 13:30-15:35
Coffee Break 15:35-15:55					
9A (T2-A) Advanced Embedded System Design and Optimization 15:55-18:00	/	9C (T10-C) Advanced Thermal Analysis for Advanced Chips 15:55-18:00	9D (Panel) AI Accelerators at a Crossroads: Who Will Power the Next Decade of AI? 15:55-18:00	9E (T9-A) Machine Learning and Optimization in Physical Design 15:55-18:00	9F (T5-C) Ultra-Low Precision and Quantization Techniques 15:55-18:00

Highlights

Opening Ceremony

Tuesday, January 20, 2026, 08:05-08:20 @ Cinderella Ballroom 1/6/7/8

Keynote Speech I

Tuesday, January 20, 2026, 08:20-09:05 @ Cinderella Ballroom 1/6/7/8

Prof. Chenming Hu (University of California, Berkeley)

"FinFET - from Lab to Foundry to EDA/Fabless"

Keynote Speech II

Tuesday, January 20, 2026, 09:05-09:50 @ Cinderella Ballroom 1/6/7/8

Prof. Yiran Chen (Duke University)

"Edge AI: Everything, Everywhere, All at Once"

Luncheon Talk

Tuesday, January 20, 12:30-13:15 @ Cinderella Ballroom 1/6/7/8

Dr. Patrick Groeneveld (AMD)

"When Moore Surpasses Mind: The Impact of 6 decades of Relentless Design Automation"

Keynote Speech III

Wednesday, January 21, 08:20-09:05 @ Cinderella Ballroom 1/6/7/8

Prof. Yuan Xie (The Hong Kong University of Science and Technology)

"Déjà Vu: From 3D to Chiplet and PIM/NDP — A Historical Perspective"

Keynote Speech IV

Wednesday, January 21, 09:05-09:50 @ Cinderella Ballroom 1/6/7/8

Dr. Charles Alpert (Cadence)

"Harnessing Agentic AI to Accelerate Designer Productivity"

Keynote Speech V

Thursday, January 22, 08:20-09:05 @ Cinderella Ballroom 1/6/7/8

Dr. Chih-Wei Jim Chang (TSMC)

"Unlocking Hyper-Scale AI: Navigating the Future of 3DIC Design Solutions"

Keynote Speech VI

Thursday, January 22, 09:05-09:50 @ Cinderella Ballroom 1/6/7/8

Dr. Takefumi Miyoshi (e-trees.Japan, Inc. & QuEL & The University of Osaka)

"Design and Implementation of Control System for Quantum Computers"

Special Session

1B (SS-4) Toward Fully Automated DTCO: ML Frameworks across Technology, Cell, and Library Layers

Tuesday, January 20, 2026, 10:20-11:35 @ Snow White 2

1D (SS-2) Design Automation for Quantum Error Correction: From Algorithms to Architectures

Tuesday, January 20, 2026, 10:20-12:00 @ Sleeping Beauty 1/2

2B (CEDA-EDS Special Session: 100 Years of the FET: From Technology Foundations to the EDA Ecosystem)

Tuesday, January 20, 2026, 13:30-15:35 @ Snow White 2

3D (SS-3) Advances in AI-Driven Circuit Verification and Reliability Analysis

Tuesday, January 20, 2026, 15:55-17:35 @ Sleeping Beauty 1/2

4D (SS-1a) Mixed-precision: Silicon-to-Model Turbo Knob

Wednesday, January 21, 2026, 10:20-11:35 @ Sleeping Beauty 1/2

5B (SS-1b) From Uniform to Adaptive: The Precision-Scalable Computing Era for Edge Intelligence

Wednesday, January 21, 2026, 13:30-14:45 @ Snow White 2

7D (SS-5) From Solvers to Layout: Cross-Layer Approaches for Reliable and Scalable IC Design

Tuesday, January 22, 2026, 10:20-12:00 @ Sleeping Beauty 1/2

Designers' Forum

5D (Designer Forum 1) Toward Autonomous Chip Design: From Foundation Models to Agentic EDA

Wednesday, January 21, 2026, 13:30-15:35 @ Sleeping Beauty 1/2

6D (Designer Forum 2) AI in Production EDA: Digital, Custom, and Manufacturing Use Cases

Wednesday, January 21, 2026, 15:55-17:35 @ Sleeping Beauty 1/2

8D (Designer Forum 3) Chiplets Go Mainstream: Design Automation for 2.5D/3D Systems

Wednesday, January 21, 2026, 13:30-15:35 @ Sleeping Beauty 1/2

9D (Panel) AI Accelerators at a Crossroads: Who Will Power the Next Decade of AI?

Thursday, January 22, 2026, 15:55-18:00 @ Sleeping Beauty 1/2

Tutorials

ASP-DAC 2026 offers attendees a set of 3 hours intense introductions to specific topics. If you register for the conference, you have the option to select two out of the six topics.

Tutorial-1: On-Device AI to Better Mobile and Implantable Devices in Healthcare

Monday, January 19, 2026, 09:00-12:00 @ Sleeping Beauty 1/2

Speaker: Yiyu Shi (University of Notre Dame)

Tutorial-2: Design Methodologies and Toolchains for Compute-in-Memory: From Architectures to Systems

Monday, January 19, 2026, 09:00-12:00 @ Sleeping Beauty 3

Speakers:

Xiaoming Chen (Institute of Computing Technology, Chinese Academy of Sciences)

Jianlei Yang (Beihang University)

Zhenhua Zhu (Tsinghua University, The Hong Kong University of Science and Technology)

Tutorial-3: Design Automation for the Early Fault Tolerant Quantum Computing

Monday, January 19, 2026, 09:00-12:00 @ Sleeping Beauty 5

Speakers:

Shigeru Yamashita (Ritsumeikan University)

He Li (Southeast University)

Zhiding Liang (CUHK)

Robert Wille (Technical University of Munich)

Tutorial-4: Bi-Directional Synergy: A Tutorial on Hardware Design for Agentic AI and Agentic AI for Hardware Design

Monday, January 19, 2026, 14:00-17:00 @ Sleeping Beauty 1/2

Speakers:

Chaojian Li (The Hong Kong University of Science and Technology)

Zhongzhi Yu (NVIDIA Research)

Zhiyao Xie (The Hong Kong University of Science and Technology)

Tutorial-5: APS: An MLIR-Based Hardware-Software Co-design Framework for Agile Processor Specialization

Monday, January 19, 2026, 14:00-17:00 @ Sleeping Beauty 3

Speakers:

Yun (Eric) Liang (Peking University)

Youwei Xiao (Peking University)

Yuyang Zou (Peking University)

Tutorial-6: Post-Silicon Validation & Hardware Security in Modern Processors

Monday, January 19, 2026, 14:00-17:00 @ Sleeping Beauty 5

Speaker:Ravi Monani (Senior System Design Engineer, AMD; former Intel)

University LSI Design Contest

Session 2D Oral Presentation

Tuesday, January 20, 2026, 13:30-15:35 @ Sleeping Beauty 1/2

Poster Presentation

Tuesday, January 20, 2026, 15:35-15:55 @Foyer

Invited Talk

Invited Talk I

Wednesday, January 21, 2026, 12:00-13:30 @ Cinderella Ballroom 1/6/7/8

Speaker: Shulin Zeng, Infinigence-AI

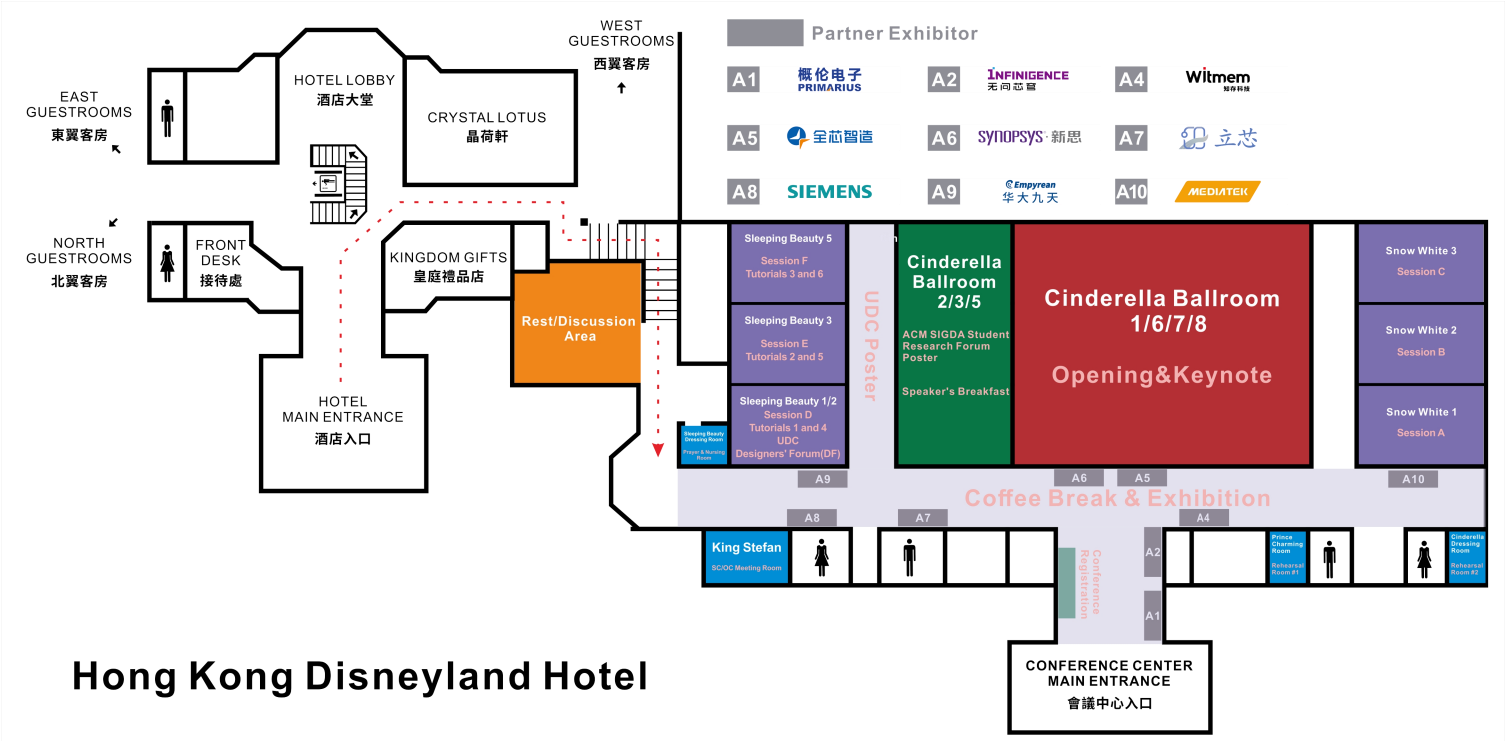
Invited Talk II

Thursday, January 22, 2026, 12:00-13:30 @ Cinderella Ballroom 1/6/7/8

Speaker: Xiaodong Meng, Advanced Manufacturing EDA Co., Ltd.

Room Assignment

Location	Event
Lobby	Registration, Conference Materials Collection, Information Desk
Cinderella Ballroom 1/6/7/8	Opening, Keynote I-VI, CEDA Distinguish Lecture, Luncheon Talk, Invited Talk, Lunch, Banquet
Snow White 1	Session A
Snow White 2	Session B, Special Session 4
Snow White 3	Session C
Sleeping Beauty 1/2	Session D, Tutorial 1&4, Special Session 1a, 2, 3&5, University LSI Design Contest Oral Session, Designer Forum 1, 2&3, Panel
Sleeping Beauty 3	Session E, Tutorial 2&5, Special Session 1b, CEDA-EDS Special Session
Sleeping Beauty 5	Session F, Tutorial 3&6
Foyer	Coffee Break, University LSI Design Contest Poster Session, Supporter's Exhibition
Prince Charming	Rehearsal Room #1
Cinderella Dressing Room 1	Rehearsal Room #2
Cinderella Ballroom 2/3/5	Speaker's Breakfast, ACM SIGDA Student Research Forum
King Stefan	SC/OC Meeting Room
Sleeping Beauty Dressing	Prayer Room, Nursing Room



Hong Kong Disneyland Hotel

Tutorials

ASP-DAC 2026 offers attendees a set of 3 hours intense introductions to specific topics. If you register for the conference, you have the option to select two out of the six topics.

Monday, January 19, 2026			
	Sleeping Beauty 1/2	**Sleeping Beauty 3**	**Sleeping Beauty 5**
09:00-12:00	Tutorial-1 On-Device AI to Better Mobile and Implantable Devices in Healthcare	Tutorial-2 Design Methodologies and Toolchains for Compute-in-Memory: From Architectures to Systems	Tutorial-3 Design Automation for the Early Fault Tolerant Quantum Computing
14:00-17:00	Tutorial-4 Bi-Directional Synergy: A Tutorial on Hardware Design for Agentic AI and Agentic AI for Hardware Design	Tutorial-5 APS: An MLIR-Based Hardware-Software Co-design Framework for Agile Processor Specialization	Tutorial-6 Post-Silicon Validation & Hardware Security in Modern Processors

Tutorial-1: On-Device AI to Better Mobile and Implantable Devices in Healthcare

Monday, January 19, 2026, 09:00 -12:00

Speaker: Yiyu Shi (University of Notre Dame)

Abstract: The increasing prevalence of chronic diseases, an aging population, and a shortage of healthcare professionals have prompted the widespread adoption of mobile and implantable devices to effectively manage various health conditions. In recent years, there is growing interest in leveraging rapid advances in artificial intelligence (AI) to enhance the performance of these devices, resulting in better patient outcomes, reduced healthcare costs, and improved patient autonomy. Due to privacy, security, and safety considerations, inferences must often be performed on the edge, with limited hardware resources. This challenge is compounded by inter-patient and intra-patient variability, heavy dependence on medical domain knowledge, and lack of diversified training data.

In this tutorial, we will explore how hardware−AI co-design techniques, such as joint hardware and neural architecture optimization and fairness-aware pruning, can fundamentally transform mobile and implantable devices. We will share case studies, including the world′s first smart Implantable Cardioverter Defibrillator (ICD) enabled by our research, illustrating how advanced edge AI methodologies can make these devices safer, more efficient, and more personalized. Attendees will gain actionable insights into deploying AI models under stringent constraints while addressing fairness, adaptability, and reliability challenges unique to healthcare applications.

Tutorial-2:Design Methodologies and Toolchains for Compute-in-Memory: From Architectures to Systems

Monday, January 19, 2026, 09:00 -12:00

Speakers:

Xiaoming Chen (Institute of Computing Technology, Chinese Academy of Sciences)

Jianlei Yang (Beihang University)

Zhenhua Zhu (Tsinghua University, The Hong Kong University of Science and Technology)

Abstract: As the demand for computational efficiency in modern AI applications continues to rise, Compute-in-Memory (CIM) has emerged as a promising computation paradigm. By performing computations directly within memory arrays, CIM architectures overcome the von-Neumann bottleneck within traditional architectures. While recent CIM hardware

designs have demonstrated impressive efficiency gains for neural network workloads, architectural innovation has significantly outpaced the development of cohesive software toolchains necessary to program, optimize, and evaluate these novel architectures.

This tutorial addresses a critical gap in system-level CIM design by presenting comprehensive design methodologies and software frameworks, which bridge the divide between algorithm development and hardware implementation. Specifically, it aims to:

☆ Introduce the fundamentals of CIM design and analyze the algorithmic and architectural design space for CIM systems.

☆ Present state-of-the-art open-source frameworks that enable end-to-end design, simulation, compilation, and evaluation.

☆Demonstrate practical workflows for algorithm mapping, performance modeling, and hardware-aware optimization.

Through detailed examination of existing design tools, intuitive examples, and hands-on demonstrations, this tutorial will offer attendees an opportunity to gain comprehensive insights into the current landscape of CIM design automation and methodologies that are essential for developing efficient AI accelerators.

Tutorial-3: Design Automation for the Early Fault Tolerant Quantum Computing

Monday, January 19, 2026, 09:00-12:00

Speakers:

Shigeru Yamashita (Ritsumeikan University)

He Li (Southeast University)

Zhiding Liang (CUHK)

Robert Wille (Technical University of Munich)

Abstract: As quantum computing transitions from NISQ experimentation to the early fault-tolerant (Early FTQC) era, progress hinges on crosslayer methods that can solve critical design automation challenges. Success in Early FTQC will require (i) reducing expensive non-Clifford resources (T-count/T-depth), (ii) co-designing algorithms and ansätze with problem structure and hardware constraints, and (iii) sustaining low physical error rates through scalable, hardware-aware calibration. This tutorial brings together four complementary perspectives to address these needs. We will explore T-depth-aware decomposition for MCT-intensive oracles, application-driven algorithm/ansatz co-design using contextual subspace strategies, and fine-grained, graph-parallel calibration protocols validated on real devices. Finally, we will present a unifying design-automation (QDA) view that connects today′s tools to the emerging requirements of Early FTQC. Attendees will leave with concrete techniques, open-source pointers, and evaluation checklists to apply immediately in their research and development.

Tutorial-4:Bi-Directional Synergy: A Tutorial on Hardware Design for Agentic AI and Agentic AI for Hardware Design

Monday, January 19, 2026, 14:00-17:00

Speakers:

Chaojian Li (The Hong Kong University of Science and Technology)

Zhongzhi Yu (NVIDIA Research)

Zhiyao Xie (The Hong Kong University of Science and Technology)

Abstract: Agentic AI systems, capable of reasoning, planning, and autonomous decision-making, are transforming how we design and deploy both AI algorithms and hardware systems. This tutorial focuses on the bi-directional synergy between hardware design for agentic AI and agentic AI for hardware design. We will cover three representative works: (1) ORCHES, which accelerates Large Language Model (LLM) reasoning for agentic AI using collaborative GPU –

Processing-In-Memory(PIM) heterogeneous architectures, (2) Spec2RTL-Agent, an LLM-agent system that automates RTL code generation from complex design specifications, and (3) SLM-Agents, which makes the case that Small Language Models (SLMs) will be the future of agentic AI because of their efficiency and scalability. Participants will gain insights into (1) hardware challenges and opportunities in supporting reasoning-centric agentic AI applications, (2) LLM-based multi-agent workflows that can revolutionize hardware design automation, and (3) the significance of SLMs in shaping efficient and sustainable agentic AI systems. The tutorial concludes with a discussion on how hardware design and agentic AI can together drive a virtuous cycle of progress.

Tutorial-5:APS: An MLIR-Based Hardware-Software Co-design Framework for Agile Processor Specialization

Monday, January 19, 2026, 14:00-17:00

Speakers:

Yun (Eric) Liang (Peking University)

Youwei Xiao (Peking University)

Yuyang Zou (Peking University)

Abstract: The rapid evolution of domain-specific applications demands specialized processors with competitive performance and efficiency. While the open RISC-V instruction set architecture (ISA) simplifies the adoption of custom instruction extensions (ISAXs), the overall process of processor specialization remains challenging. It involves a complex interplay of multiple tasks, including behavioral architecture description, hardware synthesis and implementation, processor-ISAX adaptation, and compiler co-generation. Existing RISC-V ecosystems often address these challenges manually, lacking a fully automated and integrated solution. This tutorial introduces APS for agile processor specialization based on Multi-Level Intermediate Representation (MLIR). MLIR can support multiple different requirements in a unified infrastructure. APS provides a unified framework of powerful, open-source EDA tools for seamless hardware-software co-design, empowering designers to navigate the complexities of specialization with greater ease and efficiency.

Tutorial-6: Post-Silicon Validation & Hardware Security in Modern Processors

Monday, January 19, 2026, 14:00-17:00

Speaker: Ravi Monani (Senior System Design Engineer, AMD; former Intel)

Abstract: Modern processors face a dual challenge: achieving peak performance while ensuring robust security and reliability. With increasing complexity in CPU/GPU/SoC architectures, post-silicon validation has become critical in detecting design flaws, mitigating microarchitectural vulnerabilities, and balancing power-performance tradeoffs. This tutorial provides a practitioner′s perspective, drawing on experiences from AMD and Intel, to bridge the gap between academic research and industrial practice. Topics will include silicon bring-up methodologies, case studies of hardware security vulnerabilities (e.g., speculative execution, side-channel attacks), debug and measurement techniques, and future challenges in secure processor design. Participants will gain insights into practical validation flows, security-hardening strategies, and opportunities for research collaboration with industry.

Keynote Addresses

Keynote I: FinFET - from Lab to Foundry to EDA/Fabless

Tuesday, January 20, 2026, 08:20-09:05 @ Cinderella Ballroom 1/6/7/8

Chenming Hu
TSMC Distinguished Professor Emeritus
University of California, Berkeley

Abstract: 25 years ago, the keynote speaker of the 2001 ISSCC in San Francisco projected that processor chips would dissipate more heat per area than nuclear reactor cores and rocket engine nozzles in a decade. His projection echoed the 1996 industry concensus of an end to Moore's Law in 2007 "with no known solution" (in ITRS - International Technology Rodmap of Semiconductors).
What was the cause of that chip heating crisis? How did FinFET prevent it from happening? How did FinFET find its way from the research laboratory to fabs, and the EDA/DAC and fabless communities? These and other FinFET stories will be told.

Keynote II: Edge AI: Everything, Everywhere, All at Once

Tuesday, January 20, 2026, 09:05-09:50 @ Cinderella Ballroom 1/6/7/8

Yiran Chen
John Cocke Distinguished Professor
Duke University

Abstract: Edge Artificial Intelligence (Edge AI) refers to systems that execute AI models directly on devices located at or near the point of data generation. Operating locally, these interconnected systems collect and process diverse forms of data, offering distinct advantages such as enhanced privacy and reduced latency. However, deploying AI models on resource-constrained platforms remains a major challenge. Such devices are limited in computing power, memory, energy, and communication capacity, creating a gap between the demands of advanced AI models and the capabilities of current hardware — ultimately hindering the widespread adoption of Edge AI systems. In this talk, we will explore algorithmic and hardware innovations that enable Edge AI to process multimodal data efficiently and effectively (Everything), operate reliably under stringent resource constraints (Everywhere), and collaborate seamlessly across heterogeneous platforms (All at Once).

Luncheon Talk: When Moore Surpasses Mind: The Impact of 6 decades of Relentless Design Automation

Tuesday, January 20, 2026, 12:30-13:15 @ Cinderella Ballroom 1/6/7/8

Patrick Groeneveld
Senior Fellow at AMD
Adjunct Professor, Stanford University

Abstract: After sixty years of scaling, we've crossed a symbolic threshold: a single chip now contains more transistors than the human brain has neurons. Machines built from these devices are beginning to rival — or surpass — human intelligence. This transformation forces us to revisit a question raised at the very first Design Automation Conference in 1964: how does automation reshape our work and our society? Today, that question is more urgent than ever—not only for electronic designers but for the broader world that depends on automation. Decades of progress in Electronic Design Automation made these trillion-transistor systems possible. Synthesis, placement, and routing of billions of components — while balancing cost, performance, power, and reliability — represent one of the most intricate engineering achievements in human history.

Keynote III: Déjà Vu: From 3D to Chiplet and PIM/NDP — A Historical Perspective

Wednesday, January 21, 2026, 08:20-09:05 @ Cinderella Ballroom 1/6/7/8

Yuan Xie
Fang Professor of Engineering
Chair Professor, Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology

Abstract: In this talk, the speaker reflects on a career journey marked by exploration at the intersection of technology and architecture, transitioning between academia and industry. The discussion highlights how technological advancements can drive architectural innovation, while architectural choices, in turn, influence the adoption and evolution of new technologies. Drawing from personal experience, the speaker offers a historical perspective on the dynamic interplay between 3D integration, chiplet-based design, and Processing-in-Memory (PIM) / Near-Data Processing (NDP) paradigms.

Keynote IV: Harnessing Agentic AI to Accelerate Designer Productivity

Wednesday, January 21, 2026, 09:05-09:50 @ Cinderella Ballroom 1/6/7/8

Charles Alpert
Cadence AI Fellow
Cadence Design Systems, Inc.

Abstract: As the complexity of chip designs continues to escalate and design cycles shrink, the demand for enhancing designer productivity becomes imperative. Currently, designers are entrenched in manual tasks such as writing RTL, creating verification test plans, and arduously debugging physical design flows. The industry is eagerly turning to agentic AI to elevate the abstraction level for design engineers. This talk delves into how to leverage frontier models to address vexing EDA problems and outlines the challenges ahead. By harnessing the power of agentic AI, we can accelerate the design process, reduce manual effort, and optimize outcomes, meeting the growing demands of the industry.

Keynote V: Unlocking Hyper-Scale AI: Navigating the Future of 3DIC Design Solutions

Thursday, January 22, 2026, 08:20-09:05 @ Cinderella Ballroom 1/6/7/8

Jim Chang
TSMC Academician/Deputy Director
3DIC Design Methodology Development, TSMC

Abstract: The era of hyper-scale AI demands a radical rethinking of 3DIC design, a paradigm shift unlocking unprecedented opportunities for architectural innovation for superior system performance. Yet, this explosion of possibility brings an exponential surge in design complexity, challenging even the most seasoned engineers.

This presentation will delve into the forefront of this revolution. We begin with a review of the TSMC 3DFabric™ family of solutions, specifically engineered to power the most advanced AI systems on the market today. We will then pivot to a comprehensive exploration of the critical 3DIC design challenges that emerge at this bleeding edge: from intricate 3D integration and feasibility assessment to robust implementation, power integrity, physical verification, thermal analysis, and substrate design optimization.

Join us to discover how a cohesive suite of solutions is forming the foundation for designing the AI systems of tomorrow - systems that will redefine what's possible. This is your essential guide to conquering complexity and harnessing the full potential of 3DIC for the next generation of intelligent machines.

Keynote VI: Design and Implementation of Control System for Quantum Computers

Thursday, January 22, 2026, 09:05-09:50 @ Cinderella Ballroom 1/6/7/8

Takefumi Miyoshi
Director at e-trees.Japan, Inc.
Adjunct Professor, The University of Osaka
Founder, QuEL, Inc.

Abstract: Quantum computing has advanced rapidly in recent years, raising strong expectations for its transformative impact on information processing. As quantum processors scale in size and complexity, progress in their control systems becomes increasingly essential.

This talk first introduces the roles of control systems in quantum computing and then presents our efforts in developing scalable and precise quantum computer controllers featuring high-accuracy microwave transceivers and synchronization mechanisms for reliable qubit manipulation and measurement. As we approach fault-tolerant quantum computing (FTQC), the scalability and efficiency of control electronics emerge as major challenges.

To address these challenges, compact, high-performance, and energy-efficient LSI-based control systems are required, supported by advanced design methodologies and electronic design automation (EDA) tools. Promising directions such as cryogenic CMOS integration may also open new possibilities for co-design between quantum and classical electronics. The talk will highlight how innovations in digital and analog integrated circuit design and system integration can accelerate the realization of large-scale quantum computing.

University LSI Design Contest

The University LSI Design Contest is a unique program at ASP-DAC. The contest aims to encourage research in LSI design at universities and connect the EDA community with LSI designers by providing opportunities to present and discuss innovative and state-of-the-art designs. The scope of the contest covers circuit techniques for (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC. Methods or technology used for implementation include: (a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

This year, 7 excellent designs will be presented, covering LLM / AI Inference, FPGA Acceleration, power management, ADC, Neuromorphic Computing, Wireless Interconnect, and Analog IC. The selected designs will be discussed on January 20 with short presentations and an interactive poster session. The interactive session will be held during coffee break, so you can enjoy the poster session with the delicious food. Please come and enjoy the cutting-edge design techniques. The banquet will present the Best Design Award and two Special Feature Awards for three outstanding designs. We sincerely acknowledge the contributions of all program committee and organizing committee members. We earnestly believe in promoting and enhancing research and education of LSI design in academic organizations through collaboration between circuit and EDA researchers. Please join the University LSI Design Contest and enjoy the stimulating discussions.

Date: Tuesday, January 20, 2026

Oral Presentation: Session 2D, Sleeping Beauty 1/2 (13:30 ~ 15:35)

Poster Presentation: Foyer (15:35-15:55)

	Title
2D-1	A 100V 86.2% Efficiency Fibonacci-Dickson Hybrid Boost Converter for Acoustic Screen Applications
2D-2	A 5-to-1V DLDO-Hybrid-Sigma Converter Achieving Fast Transient for High-Density Power Delivery
2D-3	Full-Stack System Design and Prototyping for Fully Programmable Electronic-Photonic Neurocomputing
2D-4	Analysis and Design of Oblong Coils and Standard-Cell-Based Receiver for Area-Efficient Edge-Coupled Inductive Coupling Transceiver
2D-5	A RHP-Zero-Free Hybrid Step-Up Converter With 95.1% Peak Efficiency for Fast-Transient Applications
2D-6	A Relaxation Oscillator with 2.93μJ/cycle Energy Efficiency and 0.068% Period Jitter
2D-7	TFLOP: Towards Energy-Efficient LLM Inference: An FPGA-Affinity Accelerator with Unified LUT-based Optimization

University LSI Design Contest Committee

Chair

Fengbin Tu (The Hong Kong University of Science and Technology)

Members

Yanan Sun (Shanghai Jiao Tong University)

Jun-Seok Park (Samsung Electronics)

Hailong Jiao (Peking University)

Xin Si (Southeast University)

Arindam Basu (City University of Hong Kong)

Dajiang Liu (Chongqing University)

Bing Li (Institute of Microelectronics, Chinese Academy of Sciences)

Wei-Han Yu (University of Macau)

Tianyu Jia (Peking University)

Patrick Yue (The Hong Kong University of Science and Technology)

Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions for real product developments among LSI designers and EDA academia/developers. The topics discussed in this forum include Autonomous Chip Design using Agentic AI, AI applications in Production EDA, Design Automation for Chiplet and 2.5D/3D Systems, and the future trajectory of AI Accelerators.

5D (Designer Forum 1) Toward Autonomous Chip Design: From Foundation Models to Agentic EDA

Wednesday, January 21, 2026, 13:30-15:10 @ Sleeping Beauty 1/2

This session explores the transformative shift from traditional algorithmic optimization to autonomous, agent-based workflows in chip design. The presentations will discuss integrating agentic AI into the core of EDA systems to dynamically adjust strategies across design stages, from floorplanning to timing closure. Speakers will highlight how Large Language Models (LLMs) and autonomous agents can redefine design productivity, enable intelligent orchestration of complex toolchains, and bridge the gap between generative AI and verified industrial synthesis.

6D (Designer Forum 2) AI in Production EDA: Digital, Custom, and Manufacturing Use Cases

Wednesday, January 21, 2026, 15:55-17:35 @ Sleeping Beauty 1/2

This session focuses on the practical deployment of AI technologies in production-grade EDA flows. It covers a broad spectrum of applications, including AI-supercharged digital implementation for faster design closure and the shaping of full-custom design ecosystems through industry-academia collaboration. The session also addresses AI-driven solutions for analog/mixed-signal design automation and the application of machine learning in accelerating critical manufacturing steps such as model and mask optimization for advanced technology nodes.

8D (Designer Forum 3) Chiplets Go Mainstream: Design Automation for 2.5D/3D Systems

Thursday, January 22, 2026, 13:30-15:35 @ Sleeping Beauty 1/2

With AI hardware driving the evolution of advanced packaging, this session delves into the critical design automation challenges for 2.5D and 3D systems. Presentations will cover "shift-left" integrated System Technology Co-Optimization (STCO) methods that incorporate multi-physics constraints early in the design phase. The session will also explore breakthroughs in electromagnetic simulation and optimization for chiplet-based designs, as well as integrated full-custom 3DIC design methodologies and flows essential for next-generation heterogeneous integration.

9D (Panel) AI Accelerators at a Crossroads: Who Will Power the Next Decade of AI?

Thursday, January 22, 2026, 15:55-18:00 @ Sleeping Beauty 1/2

As AI models continue to scale exponentially, the hardware powering them faces a critical juncture. This panel brings together leading experts from academia and industry to debate the future of AI accelerators. The discussion will examine the architectural innovations, memory hierarchies, and system-level optimizations required to sustain the growth of AI, addressing the question of which technologies and paradigms will dominate the next decade of intelligent computing.

Designers' Forum Co-Chair:
Qiang Xu (The Chinese University of Hong Kong)

ACM SIGDA Student Research Forum at ASP-DAC 2026

The Student Research Forum at the ASP-DAC is a traditional poster session hosted by ACM SIGDA for PhD students to present and discuss their dissertations with experts in the design automation community. Starting from 2015, the forum has included both PhD and MS students, offering a great opportunity for the students to establish contacts for their future careers. In addition, the forum helps companies and academic institutes to get an overview of the latest research and discover extraordinary candidates for their employment.
The forum welcomes all students, professors, and industrial professionals from the relevant research community.

Date and Time: 18:15-20:15, Tuesday, January 20, 2026
Location: Cinderella Ballroom 2/3/5

We would like to thank the following committee members for their support and contribution to this forum.

Technical committee:

Zhiyao Xie (The Hong Kong University of Science and Technology)
Jianlei Yang (Beihang University)
Zhenge Jia (Shandong University)
Lang Feng (Sun Yat-sen University)
Shiju Lin (The Hong Kong University of Science and Technology (Guangzhou))
Hongce Zhang (The Hong Kong University of Science and Technology (Guangzhou))
Yuzhe Ma (The Hong Kong University of Science and Technology (Guangzhou))
Qi Sun (Zhejiang University)
Bonan Yan (Peking University)
Zhiang Wang (Fudan University)
Zhiding Liang (The Chinese University of Hong Kong)
Cong Callie Hao (Georgia Institute of Technology)
Yibo Lin (Peking University)
Vidya A. Chhabria (Arizona State University)
Xiang Chen (Peking University)
Andy Yu-Guang Chen (National Central University)
Zhe Lin (Sun Yat-sen University)
Zhaori Bi (Fudan University)
Shao-Yun Fang (National Taiwan University of Science and Technology)
Jiaqi Gu (Arizona State University)
Keren Zhu (Fudan University)
Kang Liu (Huazhong University of Science and Technology)
Zheyu Yan (Zhejiang University)
Xinfei Guo (Shanghai Jiao Tong University

The sponsors of this forum are ACM SIGDA and Cadence Design Systems, Inc. We would also like to thank ASP-DAC 2026 for supporting this forum.

ACM SIGDA Student Research Forum Chair:
Zhiyao Xie (The Hong Kong University of Science and Technology)

Poster ID	Title	Authors and Affiliation
1	Efficient Compute-in-Memory based Accelerators for Point Cloud Neural Networks	Xipeng Lin (The Hong Kong University of Science and Technology, (Guangzhou))
2	Towards Robust and Efficient Machine Learning Systems Against Uncertainty	Dongning Ma (Villanova University)
3	Gau++: Algorithm and Hardware Co-Optimized Accelerator Towards Efficient 3D Gaussian Splatting Deployment and Application	Lizhou Wu (Fudan University)

4	Research on Energy-Efficiency-Driven Design-Technology Co-Optimization Methods	Tianliang Ma (Shanghai Jiao Tong University)
5	A Study of Performance Optimization Techniques of Digital Integrated Circuit Test Generation System	Zhiteng Chao (Chinese Academy of Sciences)
6	Design of Predictable and Reliable Computing Architecture for Robotic Systems:Includes work accepted at GLSVLSI '25, ICRA '25 and JFR	Wenhao Sun (Institute of Computing Technology, Chinese Academy of Sciences)
7	Mask Optimization in EDA: Mathematical Approaches	Ziyang Yu (The Chinese University of Hong Kong)
8	Fully Digital Hybrid Compute-in-ROM/SRAM Architecture for On-Chip Deployment of Large-Scale Deep Neural Networks	Tianyi Yu (Tsinghua University)
9	Multi-objective Full-Process Design Space Exploration for Chiplet Heterogeneous Integration	Shixin Chen (The Chinese University of Hong Kong)
10	Physically Aware Synthesis: From Optimization and Technology Mapping to Logic Resynthesis	Hongyang Pan (Fudan University)
11	Ferroelectric Compute-in-Memory Framework for Combinatorial Optimization Problems	Yu Qian (Zhejiang University)
12	Bridging Uncertainty in EDA with GNNs: Harnessing Consistency As the Key	Ziyi Wang (The Chinese University of Hong Kong)
13	Towards Performance-driven Analog Layout Design	Peng Xu (The Chinese University of Hong Kong)
14	E2S: Exploiting Effective, Efficient, and Secure Brain-Inspired Computing System	Haomin Li (Shanghai Jiao Tong University)
15	Optimizing Design Closure with Learning-Driven Approaches	Xinyun Zhang (The Chinese University of Hong Kong)
16	Reliable and Secure Analog Circuit Design and Optimization for Ultra-Resource-Constrained Edge Intelligence	Priyanjana Pal (Karlsruhe Institute of Techology Germany)
17	Design Tools for Adiabatic Superconducting Logic Circuits Toward Energy-Efficient Computing	Rongliang Fu (The Chinese University of Hong Kong)
18	Multiphysics Simulation and Optimization for Chiplet Integration Systems	Qipan Wang (Peking University)
19	Towards Better VLSI Mask Optimization	Su Zheng (The Chinese University of Hong Kong)
20	Modernizing Storage System Designs with Emerging Storage Abstractions	Yingjia Wang (The Chinese University of Hong Kong)
21	A Study of Hardware Accelerator Design Methodologies for Lattice-Based Cryptographic Algorithms	Jianan Mu (Institute of Computing Technology, Chinese Academy of Sciences)
22	Scalable and Multimodal Circuit Representation Learning	Zhengyuan Shi (The Chinese University of Hong Kong)
23	Intelligence-Native Integrated Systems: A Vertical Approach from Automated CIM to Neural SoCs	Fengshi Tian (The Hong Kong University of Science and Technology)
24	Empowering Chip Design Optimization and Verification with CPU-GPU Heterogeneous Computing	Zizheng Guo (Peking University)
25	Intelligent Computational Lithography Across Masks, Sources, and Geometries	Xiaoxiao Liang (The Hong Kong University of Science and Technology, (Guangzhou))
26	Hardware-Software Co-Design Methodology for Digital SRAM-based Processing-in-Memory Architectures	Cenlin Duan (Beihang University)
27	Software-Hardware Co-design Methodology for Compute-In-Memory Architecture Evaluation and Exploration	Yingjie Qi (Beihang University)
28	Multi-Dimensional Hardware Architecture for Artificial Intelligence	Jun Liu (Shanghai Jiao Tong University)
29	ECS: Exploiting Encoding-Centric, Efficient and Secure Computing System	Ning Yang (Shanghai Jiao Tong University)

Supporter's Exhibition

Supporter's exhibition is held by nine companies which support ASP-DAC 2026 and have exhibition booths. The supporter's exhibition is presented at Foyer of the Conference Center at Hong Kong Disneyland Hotel from January 20 through January 22.

Exhibit Hours:
08:30–18:00, January 20-22
Location: Foyer of the Conference Center at Hong Kong Disneyland Hotel

INFINIGENCE 无问芯穹

https://cloud.infini-ai.com/platform/ai

Infinigence AI, as a leading AI infrastructure enterprise in China, is committed to becoming the preferred computational resource provider in the intelligence age. Leveraging our core technological advantages in Heterogeneous Computing and Hardware-Software Co-optimization, Infinigence AI efficiently deploys various intelligent algorithms on different hardware platforms. Based on the heterogeneous computing, Infinigence AI Heterogeneous Cloud(cloud.infini-ai.com) provides engineers and innovators with the high performance compute resources and AI native toolchain, which reduces the cost and increases the efficiency of creation and innovation.

Infinigence AI embraces the mission of" Infinity Computing Accelerating the Future of AGI." We aim to make AI accessible to all through continuous technological innovation and to drive new-quality productive forces for various sectors.

全芯智造

https://www.amedac.com/

Advanced Manufacturing EDA Co., Ltd. (AMEGADAC) was founded in September 2019 with a registered capital of RMB 231 million. Headquartered in Hefei, the company has established wholly-owned subsidiaries in Shanghai, Beijing, Guangzhou, Jinan, Shenzhen, Wuhan, Hong Kong, and Hangzhou.

AMEGADAC is a high-tech enterprise specializing in R&D and delivery of professional software and services for integrated smart manufacturing solutions. With industrial software as its core driver, we actively build collaborative partnerships across the entire industrial chain, facilitating the deep integration of fragmented segments into a fully connected ecosystem. By leveraging cutting-edge technologies such as intelligent systems, we have established a distinctive and comprehensive portfolio covering the full lifecycle of industrial manufacturing software, delivering pivotal breakthroughs in the field of smart manufacturing.

SYNOPSYS® 新思

https://www.synopsys.com/zh-cn.html

Synopsys, Inc. (Nasdaq: SNPS) is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP, simulation and analysis solutions, and design services. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

立芯

https://ledatech.cn/

Founded in 2020, LEDA develops Electronic Design Automation (EDA) tools for digital design. It provides solutions for RTL synthesis, physical implementation, power integrity analysis, physical verification, and 3DIC/chiplet system design.

Witmem 知存科技

https://www.witmem.com/

Witmem (Zhicun) Technology is a global leader in CIM(computing-in-memory) chips, pioneering AI-driven solutions for cutting-edge industrial applications. By leveraging groundbreaking innovations, Witmem has revolutionized traditional computing architectures, significantly reducing data movement through in-memory computation. This approach enhances AI efficiency by two orders of magnitude, addressing the exponential demand for computational power in rapidly evolving AI models. Since its establishment in 2017, Witmem has earned support from top-tier investors and industry leaders. Moving forward, the company remains committed to advancing CIM technology. For more information, please visit www.witmem.com

Empyrean 华大九天

https://www.empyrean-tech.com/

Empyrean Technology, founded in 2009, is an EDA and services provider to the global semiconductor industry. The company strives to be the world's leading EDA provider, delivering a comprehensive front-to-back design flow across all industries.

In the EDA domain, Empyrean Technology offers EDA solution for full custom design, digital SoC design solutions, foundry EDA solutions, advanced packaging design solutions and 3DIC design solutions. Additionally, EDA solution for full custom design includes complete solutions for analog design, complete solutions for memory lC design, complete solutions for RF IC design, and complete solutions for flat panel display design. The company provides EDA-related services, including foundation IP and foundry design enablement services. EDA and services find applications mainly in the fields of lC design, foundry, and packaging.

MEDIATEK

https://www.mediatek.com/

MediaTek Incorporated is the world's fifth largest global fabless semiconductor company. We are market leaders in developing innovative systems-on-chip (SoC) for mobile device, home entertainment, connectivity and IoT (Internet of Things) products. Ultimately, we power more than 2 billion devices a year – supporting productivity in 20 percent of homes and nearly 1 of every 3 mobile phones globally.

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SIEMENS

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概伦电子
PRIMARIUS

https://www.primarius-tech.com/en.php

Primarius is a global competitive EDA company, committed to delivering Innovative DTCO EDA solutions.

We strive to accelerate time-to-market and enhance the YPPA of circuit designs and manufacturing, by providing innovative Design Technology Co-Optimization (DTCO) EDA solutions and unique data-driven approaches.

Our industry-leading design enablement technologies cover semiconductor parametric testing, advanced SPICE modeling, PDK and standard cell library development.

We leverage cutting-edge SPICE/FastSPICE simulation technologies and a flexible custom design platform to establish a complete DTCO-enabled custom design flow for complex Memory, Analog, and Mixed-signal designs.

Monday, January 19, 2026

T1 **Tutorial-1: On-Device AI to Better Mobile and Implantable Devices in Healthcare**
Time: 09:00-12:00, Monday, January 19, 2026
Location: Sleeping Beauty 1/2

Speaker: Yiyu Shi (University of Notre Dame)

T2 **Tutorial-2: Design Methodologies and Toolchains for Compute-in-Memory: From Architectures to Systems**
Time: 09:00-12:00, Monday, January 19, 2026
Location: Sleeping Beauty 3

Speakers: Xiaoming Chen (Institute of Computing Technology, Chinese Academy of Sciences), Jianlei Yang (Beihang University), Zhenhua Zhu (Tsinghua University, The Hong Kong University of Science and Technology)

T3 **Tutorial-3: Design Automation for the Early Fault Tolerant Quantum Computing**
Time: 09:00-12:00, Monday, January 19, 2026
Location: Sleeping Beauty 5

Speakers: Shigeru Yamashita (Ritsumeikan University), He Li (Southeast University), Zhiding Liang (CUHK), Robert Wille (Technical University of Munich)

T4 **Tutorial-4: Bi-Directional Synergy: A Tutorial on Hardware Design for Agentic AI and Agentic AI for Hardware Design**
Time: 14:00-17:00, Monday, January 19, 2026
Location: Sleeping Beauty 1/2

Speakers: Chaojian Li (The Hong Kong University of Science and Technology), Zhongzhi Yu (NVIDIA Research), Zhiyao Xie (The Hong Kong University of Science and Technology)

T5 **Tutorial-5: APS: An MLIR-Based Hardware-Software Co-design Framework for Agile Processor Specialization**
Time: 14:00-17:00, Monday, January 19, 2026
Location: Sleeping Beauty 3

Speakers: Yun (Eric) Liang (Peking University), Youwei Xiao (Peking University), Yuyang Zou (Peking University)

T6 **Tutorial-6: Post-Silicon Validation & Hardware Security in Modern Processors**
Time: 14:00-17:00, Monday, January 19, 2026
Location: Sleeping Beauty 5

Speaker: Ravi Monani (Senior System Design Engineer, AMD; former Intel)

Tuesday, January 20, 2026

Opening and Keynote Session I

Time: 08:05-09:50, Tuesday, January 20, 2026
Location: Cinderella Ballroom 1/6/7/8
Chair(s): Tsung-Yi Ho (The Chinese University of Hong Kong)

ASP-DAC 2026 Opening

Opening Address from General Chair Tsung-Yi Ho (The Chinese University of Hong Kong)
TPC Report from Technical Program Chair Takashi Sato (Kyoto University)

Keynote Address I: FinFET - from Lab to Foundry to EDA/Fabless
Chenming Hu (University of California, Berkeley)

Keynote Address II: Edge AI: Everything, Everywhere, All at Once
Yiran Chen (Duke University)

1A (T4-C) AI Applications for Edge and Domain-Specific Systems

Time: 10:20-12:00, Tuesday, January 20, 2026
Location: Snow White 1
Chair(s): Sunmean Kim (Kyungpook National University); Jeongwoo Park (Sungkyunkwan University)

1A-1 (Time: 10:20-10:45)

1A-2 (Time: 10:45-11:10)

1A-3 (Time: 11:10-11:35)

1A-4 (Time: 11:35-12:00)

Tuesday, January 20, 2026

1B **(SS-4) Toward Fully Automated DTCO: ML Frameworks across Technology, Cell, and Library Layers**

Time: 10:20-11:35, Tuesday, January 20, 2026

Location: Snow White 2

Chair(s): Taewhan Kim (Seoul National University)

1B-1 (Time: 10:20-10:45)

1B-2 (Time: 10:45-11:10)

1B-3 (Time: 11:10-11:35)

1C **(T12-D) Physical Attacks and Countermeasures**

Time: 10:20-12:00, Tuesday, January 20, 2026

Location: Snow White 3

Chair(s): Qiang Liu (Tianjin University); Jiaji He (Tianjin University)

1C-1 (Time: 10:20-10:45)

1C-2 (Time: 10:45-11:10)

1C-3 (Time: 11:10-11:35)

1C-4 (Time: 11:35-12:00)

Tuesday, January 20, 2026

1D (SS-2) Design Automation for Quantum Error Correction: From Algorithms to Architectures

Time: 10:20-12:00, Tuesday, January 20, 2026
Location: Sleeping Beauty 1/2
Chair(s): Zhiyao Xie (The Hong Kong University of Science and Technology)

1D-1 (Time: 10:20-10:45)

Fault-tolerant State Preparation for Quantum Error Correction Codes: Leveraging Design Automation
*Robert Wille (TUM) with contributions from Lucas Berent (TUM), Markus Müller (Forschungszentrum Jülich), Tom Peham (TUM), Ludwig Schmid (TUM), Erik Weilandt (TUM)

1D-2 (Time: 10:45-11:10)

1D-3 (Time: 11:10-11:35)

1D-4 (Time: 11:35-12:00)

1E (T11-A) Ensuring High Quality Designs through Simulation and Verification Advances

Time: 10:20-11:35, Tuesday, January 20, 2026
Location: Sleeping Beauty 3
Chair(s): Yutaka Masuda (Nagoya University); Senling Wang (Ehime University)

1E-1 (Time: 10:20-10:45)

1E-2 (Time: 10:45-11:10)

1E-3 (Time: 11:10-11:35)

1F (T7-A) Efficient Design of Spiking Neural Network Accelerators

Time: 10:20-12:00, Tuesday, January 20, 2026
Location: Sleeping Beauty 5
Chair(s): Can Li (Hong Kong University); Tingting Zhang (McGill University)

Tuesday, January 20, 2026

1F-1 (Time: 10:20-10:45)

1F-2 (Time: 10:45-11:10)

1F-3 (Time: 11:10-11:35)

1F-4 (Time: 11:35-12:00)

Luncheon Talk

Time: 12:30-13:15, Tuesday, January 20, 2026
Location: Cinderella Ballroom 1/6/7/8
Chair(s): Iris Hui-Ru Jiang, National Taiwan University

Luncheon Talk: When Moore Surpasses Mind: The Impact of 6 decades of Relentless Design Automation

Patrick Groeneveld (AMD)

2A (T5-B) Vision and Transformer Acceleration Architectures

Time: 13:30-15:35, Tuesday, January 20, 2026
Location: Snow White 1
Chair(s): Caiwen Ding (University of Minnesota - Twin Cities); Sungju Ryu (Sogang University)

2A-1 (Time: 13:30-13:55)

2A-2 (Time: 13:55-14:20)

2A-3 (Time: 14:20-14:45)

2A-4 (Time: 14:45-15:10)

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2A-5 (Time: 15:10-15:35)

JaneEye: A 12-nm 2K-FPS 18.9-μJ/Frame Event-based Eye Tracking Accelerator····· 170

*Tao Han, Ang Li (Delft University of Technology), Qinyu Chen (Leiden University), Chang Gao (Delft University of Technology)

2B **(CEDA-EDS Special Session: 100 Years of the FET: From Technology Foundations to the EDA Ecosystem)**

Time: 13:30-15:35, Tuesday, January 20, 2026

Location: Snow White 2

Chair(s): Yu [Kevin] Cao (University of Minnesota)

2B-1 (13:30-13:55)

(Special Session) FET100: Celebrating the Past and Inspiring the Future

*Bin Zhao (Jr. Past President, IEEE Electron Devices Society)

2B-2 (13:55-14:20)

(Special Session) The FET at 100: Old and Needing Assistance

*Greg Yeric

2B-3 (14:20-14:45)

(Special Session) CMOS 2.0: UnFETtering the Scaling of CMOS

*Julien Ryckaert (IMEC)

2B-4 (14:45-15:10)

(Special Session) Compact Modeling - A Bridge between Foundry and Circuit Design

*Yogesh Singh Chauhan (IIT, Kanpur)

2B-5 (15:10-15:35)

(Special Session) Nanoelectronic Modeling (NEMO): From Esoteric Quantum Theory to Software that Helps Design Tomorrow's Atomic-scaled Transistors and Global Impact in nanoHUB

*Gerhard Klimeck (Purdue University)

2C **(T13-B) From HDL to Hardware: Scalable Design Automation for Quantum Computing**

Time: 13:30-15:35, Tuesday, January 20, 2026

Location: Snow White 3

Chair(s): Zhiding Liang (The Chinese University of Hong Kong); Johannes Geier (Technical University of Munich)

2C-1 (Time: 13:30-13:55)

Scalable Optimization with GIS-PIM: A Generalized Integer-State Probabilistic Ising Machine····· 177

*Chirag Garg, Sayeef Salahuddin (University of California, Berkeley)

2C-2 (Time: 13:55-14:20)

A Scalable and High-Quality Qubit Mapping and Shuttling Framework for Neutral Atom Quantum Devices····· 184

*Sung-Ying Hsieh, Wai-Kei Mak (National Tsing Hua University)

Tuesday, January 20, 2026

2C-3 (Time: 14:20-14:45)

2C-4 (Time: 14:45-15:10)

2C-5 (Time: 15:10-15:35)

2D University Design Contest

Time: 13:30-15:35, Tuesday, January 20, 2026
Location: Sleeping Beauty 1/2
Chair(s): Fengbin Tu (The Hong Kong University of Science and Technology)

2D-1

2D-2

2D-3

2D-4

2D-5

Tuesday, January 20, 2026

2D-6

2D-7

2E (T10-A) Reliability-Driven and Low-Power Design

Time: 13:30-15:35, Tuesday, January 20, 2026
Location: Sleeping Beauty 3
Chair(s): Bei Yu (The Chinese University of Hong Kong); Yu-Guang Chen (National Central University)

2E-1 (Time: 13:30-13:55)

2E-2 (Time: 13:55-14:20)

2E-3 (Time: 14:20-14:45)

2E-4 (Time: 14:45-15:10)

2E-5 (Time: 15:10-15:35)

Tuesday, January 20, 2026

2F (T8-C) Application of Generative and Predictive Methods to Design Optimization

Time: 13:30-15:35, Tuesday, January 20, 2026
Location: Sleeping Beauty 5
Chair(s): Victor Kravets (IBM Inc.); Xinyu Chen (The Hong Kong University of Science and Technology (Guangzhou))

3A (T5-A) Advanced Accelerators for Emerging AI Workloads

Time: 15:55-18:00, Tuesday, January 20, 2026
Location: Snow White 1
Chair(s): Guohao Dai (Shanghai Jiao Tong University); Zhenhua Zhu (Tsinghua University, The Hong Kong University of Science and Technology)

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3A-2 (Time: 16:20-16:45)

3A-3 (Time: 16:45-17:10)

3A-4 (Time: 17:10-17:35)

3A-5 (Time: 17:35-18:00)

3B (T1-C) Advances in Agile Design Acceleration

Time: 15:55-18:00, Tuesday, January 20, 2026
Location: Snow White 2
Chair(s): Hiroki Nishikawa (The University of Osaka); Shih-Hao Hung (National Taiwan University)

3B-1 (Time: 15:55-16:20)

3B-2 (Time: 16:20-16:45)

3B-3 (Time: 16:45-17:10)

Tuesday, January 20, 2026

3B-4 (Time: 17:10-17:35)

3B-5 (Time: 17:35-18:00)

3C **(T13-A) Beyond Silicon: Emerging Paradigms in EDA for Atomic Scale Computing, Photonics, and Microfluidics**
Time: 15:55-18:00, Tuesday, January 20, 2026
Location: Snow White 3
Chair(s): Xunzhao Yin (Zhejiang University); Andy Yu-Guang Chen (National Central University)

3C-1 (Time: 15:55-16:20)

3C-2 (Time: 16:20-16:45)

3C-3 (Time: 16:45-17:10)

3C-4 (Time: 17:10-17:35)

3C-5 (Time: 17:35-18:00)

Tuesday, January 20, 2026

3D (SS-3) Advances in AI-Driven Circuit Verification and Reliability Analysis

Time: 15:55-17:35, Tuesday, January 20, 2026
Location: Sleeping Beauty 1/2
Chair(s): Zhiyao Xie (The Hong Kong University of Science and Technology)

3D-1 (Time: 15:55-16:20)

3D-2 (Time: 16:20-16:45)

3D-3 (Time: 16:45-17:10)

3D-4 (Time: 17:10-17:35)

3E (T9-E) Timing Analysis and Timing-Aware Physical Synthesis

Time: 15:55-18:00, Tuesday, January 20, 2026
Location: Sleeping Beauty 3
Chair(s): Jeong-Tyng Li (National Tsing Hua University); Yi-Yu Liu (National Taiwan University of Science and Technology)

3E-1 (Time: 15:55-16:20)

3E-2 (Time: 16:20-16:45)

3E-3 (Time: 16:45-17:10)

Tuesday, January 20, 2026

3E-4 (Time: 17:10-17:35)

3E-5 (Time: 17:35-18:00)

3F (T8-B) Adanced Performance Optimization for High-level Synthesis and Scheduling

Time: 15:55-18:00, Tuesday, January 20, 2026
Location: Sleeping Beauty 5
Chair(s): Wei Zhang (The Hong Kong University of Science and Technology); Zeke Wang (Zhejiang University)

3F-1 (Time: 15:55-16:20)

3F-2 (Time: 16:20-16:45)

3F-3 (Time: 16:45-17:10)

3F-4 (Time: 17:10-17:35)

3F-5 (Time: 17:35-18:00)

Wednesday, January 21, 2026

Keynote Session II

Time: 08:20-09:50, Wednesday, January 21, 2026
Location: Cinderella Ballroom 1/6/7/8
Chair(s): Tsung-Yi Ho (The Chinese University of Hong Kong)

Keynote Address III: Déjà Vu: From 3D to Chiplet and PIM/NDP — A Historical Perspective
Yuan Xie (The Hong Kong University of Science and Technology)

Keynote Address IV: Déjà Vu: From 3D to Chiplet and PIM/NDP — A Historical Perspective
Charles Alpert (Cadence)

4A (T4-B) AI for Hardware, Systems, and Verification

Time: 10:20-12:00, Wednesday, January 21, 2026
Location: Snow White 1
Chair(s): Lin Ting-Jung (Ningbo Institute of Digital Twin, EIT); Heechun Park (Ulsan National Institute of Science and Technology)

4A-1 (Time: 10:20-10:45)

*Zechao Lin, Xingbin Wang, Yiming Xie, Dan Meng, Rui Hou (Institute of Information Engineering, Chinese Academy of Sciences)

4A-2 (Time: 10:45-11:10)

*Yan Tan (The Hong Kong University of Science and Technology (Guangzhou)), Xiangchen Meng, Zijun Jiang, Yangdi Lyu (The Hong Kong University of Science and Technology (Guangzhou))

4A-3 (Time: 11:10-11:35)

*Pingqing Zheng, Jiayin Qin, Fuqi Zhang, Niraj Chitla (University of Minnesota, Twin Cities), Zishen Wan (Georgia Institute of Technology), Shang Wu (Northwestern University), Yu Cao, Caiwen Ding, Yang Zhao (University of Minnesota, Twin Cities)

4A-4 (Time: 11:35-12:00)

*Zhantong Zhu, Kangbo Bai, Tianyu Jia (Peking University)

4B (T3-D) Accelerating LLMs with Near- and In-Memory Computing

Time: 10:20-12:00, Wednesday, January 21, 2026
Location: Snow White 2
Chair(s): Shanshi Huang (The Hong Kong University of Science and Technology (Guangzhou)); Shanlin Xiao (Sun Yat-sen University)

Wednesday, January 21, 2026

4B-1 (Time: 10:20-10:45)

4B-2 (Time: 10:45-11:10)

4B-3 (Time: 11:10-11:35)

4B-4 (Time: 11:35-12:00)

4C (T11-C) Tackling Reliability Issues across the Layers

Time: 10:20-11:35, Wednesday, January 21, 2026
Location: Snow White 3
Chair(s): Michihiro Shintani (Kyoto Institute of Technology); Yutaka Masuda (Nagoya University)

4C-1 (Time: 10:20-10:45)

4C-2 (Time: 10:45-11:10)

4C-3 (Time: 11:10-11:35)

Wednesday, January 21, 2026

4D (SS-1a) Mixed-precision: Silicon-to-Model Turbo Knob

Time: 10:20-11:35, Wednesday, January 21, 2026
Location: Sleeping Beauty 1/2
Chair(s): Li Jiang (Shanghai Jiao Tong University & Shanghai Qi Zhi Institute)

4D-1 (Time: 10:20-10:45)

4D-2 (Time: 10:45-11:10)

4D-3 (Time: 11:10-11:35)

4E (T10-B) Explainable and Generative AI for Lithography and Yield Optimization

Time: 10:20-12:00, Wednesday, January 21, 2026
Location: Sleeping Beauty 3
Chair(s): Yuzhe Ma (The Hong Kong University of Science and Technology (Guangzhou)); Binwu Zhu (Southeast University)

4E-1 (Time: 10:20-10:45)

4E-2 (Time: 10:45-11:10)

4E-3 (Time: 11:10-11:35)

4E-4 (Time: 11:35-12:00)

Wednesday, January 21, 2026

4F (T6-B) Smart Techniques for Analog & Mixed-Signal Design

Time: 10:20-11:35, Wednesday, January 21, 2026
Location: Sleeping Beauty 5
Chair(s): Fan Yang (Fudan University); Pingqiang Zhou (ShanghaiTech University)

5A (T3-B) Emerging Memory Architectures and Their Applications

Time: 13:30-15:35, Wednesday, January 21, 2026
Location: Snow White 1
Chair(s): Yuhong Liang (Great Bay University (GBU)); Chun-Yi Lee(National Taiwan University)

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5A-5 (Time: 15:10-15:35)

5B (SS-1b) From Uniform to Adaptive: The Precision-Scalable Computing Era for Edge Intelligence

Time: 13:30-14:45, Wednesday, January 21, 2026
Location: Snow White 2
Chair(s): Fangxin Liu (Shanghai Jiao Tong University)

5B-1 (Time: 13:30-13:55)

5B-2 (Time: 13:55-14:20)

5B-3 (Time: 14:20-14:45)

5C (T12-C) System-Level Security and Secure Communication

Time: 13:30-15:35, Wednesday, January 21, 2026
Location: Snow White 3
Chair(s): Song Bian (Beihang University); Danella Zhao (The University of Arizona)

5C-1 (Time: 13:30-13:55)

5C-2 (Time: 13:55-14:20)

5C-3 (Time: 14:20-14:45)

Wednesday, January 21, 2026

5C-4 (Time: 14:45-15:10)

ANIMo: Accelerating Nested Isolation with Monitor-free Domain Transition……744

*Yibin Xu, Han Wang, Yue Jin, Tianyi Huang, Tianyue Lu, Mingyu Chen (SKLP, Institute of Computing Technology, CAS; University of Chinese Academy of Sciences)

5C-5 (Time: 15:10-15:35)

Reinforced Logic-Based Distributed Routing within Isolated Secure Zones……751

*Yogesh Verma, Mattis Hasler (barkhausen institut), Sebastian Haas, Friedrich Pauls (Barkhausen institut)

5D (Designer Forum 1) Toward Autonomous Chip Design: From Foundation Models to Agentic EDA

Time: 13:30-15:35, Wednesday, January 21, 2026
Location: Sleeping Beauty 1/2
Chair(s): Zhiyao Xie (The Hong Kong University of Science and Technology)

5D-1 (13:30-13:55)

(Designer Forum) Intelligent Chip Design with Agentic AI EDA

*James Gu (Cadence)

5D-2 (13:55-14:20)

(Designer Forum) The Al Transformation of Semiconductor EDA

*Muming Tang (Synopsys)

5D-3 (14:20-14:45)

(Designer Forum) From Algorithmic Optimization to Autonomous Agents: Redefining EDA Workflows with AI

*Peng Zou (Shanghai LEDA Technology)

5D-4 (14:45-15:10)

(Designer Forum) From Generation to Verified Synthesis: Bridging Industrial Reality via C-Guided Agents

*Min Li (Southeast Univeristy)

5D-5 (15:10-15:35)

(Designer Forum) SLEG: A LLM-based SVA Evaluation and Generation System

*Tao Lin (Xepic. Inc.)

5E (T9-D) Performance-Driven Floorplanning and Global Placement

Time: 13:30-15:35, Wednesday, January 21, 2026
Location: Sleeping Beauty 3
Chair(s): Wai Kei Mak (National Tsing Hua University); Yi-Yu Liu (National Taiwan University of Science and Technology)

5E-1 (Time: 13:30-13:55)

MdpoPlanner: Mask-Driven Floorplan via Reinforcement Learning-Based Placement Order…… 758

Yue Wu, *Caiyu Chen, Xiaoyan Yang (Hangzhou Dianzi University)

Wednesday, January 21, 2026

5E-2 (Time: 13:55-14:20)

5E-3 (Time: 14:20-14:45)

5E-4 (Time: 14:45-15:10)

5E-5 (Time: 15:10-15:35)

5F (T8-A) Advances in Logic Optimization and Technology Mapping

Time: 13:30-15:35, Wednesday, January 21, 2026
Location: Sleeping Beauty 5
Chair(s): Hongce Zhang (The Hong Kong University of Science and Technology (Guangzhou)); Yuanqing Cheng (Beihang University)

5F-1 (Time: 13:30-13:55)

5F-2 (Time: 13:55-14:20)

5F-3 (Time: 14:20-14:45)

5F-4 (Time: 14:45-15:10)

Wednesday, January 21, 2026

5F-5 (Time: 15:10-15:35)

6A (T3-C) Circuit- and Device-Aware Design for CIM

Time: 15:55-18:00, Wednesday, January 21, 2026
Location: Snow White 1
Chair(s): Hiromitsu Awano (Kyoto University); Arindam BASU (City University of Hong Kong)

6A-1 (Time: 15:55-16:20)

6A-2 (Time: 16:20-16:45)

6A-3 (Time: 16:45-17:10)

6A-4 (Time: 17:10-17:35)

6A-5 (Time: 17:35-18:00)

6B (T1-B) Accelerator and mapping innovations for LLMs and Neural Networks

Time: 15:55-18:00, Wednesday, January 21, 2026
Location: Snow White 2
Chair(s): Zhe Lin (Sun Yat-sen University); Jianwang Zhai (Beijing University of Posts and Telecommunications)

6B-1 (Time: 15:55-16:20)

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6B-2 (Time: 16:20-16:45)

6B-3 (Time: 16:45-17:10)

6B-4 (Time: 17:10-17:35)

6B-5 (Time: 17:35-18:00)

6C (T12-B) Logic Locking and Hardware Trojan Detection

Time: 15:55-18:00, Wednesday, January 21, 2026
Location: Snow White 3
Chair(s): Amin Rezaei (California State University, Long Beach); Qiaoyan Yu (University of New Hampshire)

6C-1 (Time: 15:55-16:20)

6C-2 (Time: 16:20-16:45)

6C-3 (Time: 16:45-17:10)

6C-4 (Time: 17:10-17:35)

Wednesday, January 21, 2026

6C-5 (Time: 17:35-18:00)

SAND: A Self-supervised and Adaptive NAS-Driven Framework for Hardware Trojan Detection····· 931
*Zhixin Pan (Florida State University), Ziyu Shu (Stony Brook University), Linh Nguyen, Amberbir Alemayoh (Florida State University)

6D (Designer Forum 2) AI in Production EDA: Digital, Custom, and Manufacturing Use Cases

Time: 15:55-17:35, Wednesday, January 21, 2026
Location: Sleeping Beauty 1/2
Chair(s): Min Li (Southeast University)

6D-1 (15:55-16:20)

(Designer Forum) How AI is Supercharging Digital lmplementation
*Ko-Lung Yuan (Siemens)

6D-2 (16:20-16:45)

(Designer Forum) Shaping a Full-custom Design Ecosystem with industry-Academia-Research Collaboration
*Michael Liu (Empyrean Technology)

6D-3 (16:45-17:10)

(Designer Forum) AI-driven Analog and Custom Design Solution
*Yutao Ma (PRIMARIUS)

6D-4 (17:10-17:35)

(Designer Forum) Exploring the Application of Machine Learning inAccelerating Model and Mask Optimization
*Xiaodong Meng (AMEGADAC)

6E (T9-C) Cell Placement and Generation for Advanced Technologies

Time: 15:55-18:00, Wednesday, January 21, 2026
Location: Sleeping Beauty 3
Chair(s): Pingqiang Zhou (ShanghaiTech University); Yibo Lin (Peking University)

6E-1 (Time: 15:55-16:20)

An Effective Placement Framework for Designs with Half-Row-Extended Cells····· 938
Po-Yi Wu (National Tsing Hua University), *Tzu-Sheng Hung (National Tsing Hua University), Wai-Kei Mak, Ting-Chi Wang (National Tsing Hua University)

6E-2 (Time: 16:20-16:45)

DUALPlace: Reinforcement Learning based Mixed-size Placement with Multi Modal Cross Attention····· 945
Yue Wu, *Hu Liu, Jiayi Ding, Junwei Li, Tieming Han, Xiaoyan Yang (Hangzhou Dianzi University)

6E-3 (Time: 16:45-17:10)

SMT-Based Optimal Transistor Folding and Placement for Standard Cell Layout Generation····· 952
*Junghyun Yoon, Heechun Park (Ulsan National Institute of Science and Technology)

6E-4 (Time: 17:10-17:35)

Synthesis of CFET Standard Cells Utilizing Backside Interconnects Towards Improving Pin Accessibility·····959
*Hyunbum Park, Taewhan Kim (Seoul National University)

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6E-5 (Time: 17:35-18:00)

6F (T5-E) Hardware-Software Co-Design and Optimization Frameworks

Time: 15:55-18:00, Wednesday, January 21, 2026
Location: Sleeping Beauty 5
Chair(s): Zhenhua Zhu (Tsinghua University, HKUST)

6F-1 (Time: 15:55-16:20)

6F-2 (Time: 16:20-16:45)

6F-3 (Time: 16:45-17:10)

6F-4 (Time: 17:10-17:35)

6F-5 (Time: 17:35-18:00)

Thursday, January 22, 2026

Keynote Session III

Time: 08:20-09:50, Thursday, January 22, 2026
Location: Cinderella Ballroom 1/6/7/8
Chair(s): Tsung-Yi Ho (The Chinese University of Hong Kong)

Keynote Address V: Unlocking Hyper-Scale AI: Navigating the Future of 3DIC Design Solutions
Jim Chang (TSMC)

Keynote Address VI: Design and Implementation of Control System for Quantum Computers
Takefumi Miyoshi (e-trees.Japan, Inc. & QuEL & The University of Osaka)

7A (T4-A) Efficient AI Model Design and Training

Time: 10:20-12:00, Thursday, January 22, 2026
Location: Snow White 1
Chair(s): Masanori Hashimoto (Kyoto University); Chen Wu (Ningbo Institute of Digital Twin, Eastern Institute of Technology, Ningbo)

7A-1 (Time: 10:20-10:45)

StabiFreeze: Early Stopping for Training Binary Neural Networks via Internal Dynamics Stabilization……1006
*Jisu Kim, Tae-Hwan Kim (Korea Aerospace University)

7A-2 (Time: 10:45-11:10)

Constrained NAS via Symbolic Expressions in Declarative Hierarchical Search Spaces……1014
*Moritz Reiber, Christoph Gerum, Oliver Bringmann (University of Tübingen)

7A-3 (Time: 11:10-11:35)

HERO: Hardware-Efficient RL-based Optimization Framework for NeRF Quantization……1021
*Yipu Zhang, Chaofang Ma, Jinming Ge (The Hong Kong University of Science and Technology), Lin Jiang (Northeastern University), Jiang Xu (The Hong Kong University of Science and Technology (Guangzhou)), Wei Zhang (The Hong Kong University of Science and Technology)

7A-4 (Time: 11:35-12:00)

Gundam: A Generalized Unified Design and Analysis Model for Matrix Multiplication on Edge……1028
Quan Cheng, Haoyuan Li, Weirong Dong (Kyoto University), Mingqiang Huang, Longyang Lin (Southern University of Science and Technology), *Masanori Hashimoto (Kyoto University)

7B (T2-B) Designing Predictable and Reliable Real-Time Systems

Time: 10:20-12:00, Thursday, January 22, 2026
Location: Snow White 2
Chair(s): Zhenyu Yan (The Chinese University of Hong Kong); Zhiding Liang (The Chinese University of Hong Kong

Thursday, January 22, 2026

7B-1 (Time: 10:20-10:45)

7B-2 (Time: 10:45-11:10)

7B-3 (Time: 11:10-11:35)

7B-4 (Time: 11:35-12:00)

7C (T11-B) Scaling up Physical Design Optimization to Heterogeneous Systems

Time: 10:20-11:35, Thursday, January 22, 2026
Location: Snow White 3
Chair(s): Senling Wang (Ehime University); Michihiro Shintani (Kyoto Institute of Technology)

7C-1 (Time: 10:20-10:45)

7C-2 (Time: 10:45-11:10)

7C-3 (Time: 11:10-11:35)

Thursday, January 22, 2026

7D (SS-5) From Solvers to Layout: Cross-Layer Approaches for Reliable and Scalable IC Design

Time: 10:20-12:00, Thursday, January 22, 2026
Location: Sleeping Beauty 1/2
Chair(s): Tony Geng (Rice University)

7D-1 (Time: 10:20-10:45)

7D-2 (Time: 10:45-11:10)

7D-3 (Time: 11:10-11:35)

7D-4 (Time: 11:35-12:00)

7E (T7-B) Emerging Computing Architectures and Learning Systems

Time: 10:20-12:00, Thursday, January 22, 2026
Location: Sleeping Beauty 3
Chair(s): Ke Chen (Nanjing University of Aeronautics and Astronautics); Hao Geng (ShanghaiTech University)

7E-1 (Time: 10:20-10:45)

7E-2 (Time: 10:45-11:10)

7E-3 (Time: 11:10-11:35)

Thursday, January 22, 2026

7E-4 (Time: 11:35-12:00)

7F (T6-A) RF and Photonic IC

Time: 10:20-12:00, Thursday, January 22, 2026
Location: Sleeping Beauty 5
Chair(s): Yuanqing Cheng (Beihang University); Yibo Lin (Peking University)

7F-1 (Time: 10:20-10:45)

7F-2 (Time: 10:45-11:10)

7F-3 (Time: 11:10-11:35)

7F-4 (Time: 11:35-12:00)

8A (T3-A) Hybrid CIM Architectures and Flexible Dataflows

Time: 13:30-15:35, Thursday, January 22, 2026
Location: Snow White 1
Chair(s): Ren-Shuo Liu (National Tsing Hua University); Atsutake Kosuge (University of Tokyo)

8A-1 (Time: 13:30-13:55)

Thursday, January 22, 2026

8A-2 (Time: 13:55-14:20)

8A-3 (Time: 14:20-14:45)

8A-4 (Time: 14:45-15:10)

8A-5 (Time: 15:10-15:35)

8B (T1-A) Exploring interconnect design, power modeling, and system prototyping

Time: 13:30-15:35, Thursday, January 22, 2026
Location: Snow White 2
Chair(s): Chester Park (Konkuk University); Fitzgerald Sungkyung Park (Pusan National Univeristy)

8B-1 (Time: 13:30-13:55)

8B-2 (Time: 13:55-14:20)

8B-3 (Time: 14:20-14:45)

8B-4 (Time: 14:45-15:10)

Thursday, January 22, 2026

8B-5 (Time: 15:10-15:35)

8C (T12-A) Privacy-Preserving & Secure AI Computation

Time: 13:30-15:35, Thursday, January 22, 2026
Location: Snow White 3
Chair(s): Danella Zhao (The University of Arizona); Song Bian (Beihang University)

8C-1 (Time: 13:30-13:55)

8C-2 (Time: 13:55-14:20)

8C-3 (Time: 14:20-14:45)

8C-4 (Time: 14:45-15:10)

8C-5 (Time: 15:10-15:35)

8D (Designer Forum 3) Chiplets Go Mainstream: Design Automation for 2.5D/3D Systems

Time: 13:30-15:35, Thursday, January 22, 2026
Location: Sleeping Beauty 1/2
Chair(s): Hailong Yao (University of Science and Technology Beijing)

8D-1 (13:30-13:55)

Thursday, January 22, 2026

8D-2 (13:55-14:20)

(Designer Forum) Integrated Full-custom 3DIC Design Methodology and Flow

*Michael Liu (Empyrean Technology)

8D-3 (14:20-14:45)

(Designer Forum) Al for EDA: Chiplets Simulation New Era

*Jimin Wen (Xpeedic)

8D-4 (14:45-15:10)

(Designer Forum) Breakthroughs in Chiplet-Based Electromagnetic Designs: Efficient Simulation and Al-Driven Optimization

*Peng Zhao(Faraday Dynamics)

8D-5 (15:10-15:35)

(Designer Forum) A Shift-Left Design Methodology for Chiplet Architecture: Automation, Multi-Physics Modeling and Converaence

*Chen Wu (BTD Technology/EIT)

8E (T9-B) Advances in Routing for Chips and Advanced Packaging

Time: 13:30-15:35, Thursday, January 22, 2026

Location: Sleeping Beauty 3

Chair(s): Siting Liu (The Chinese University of Hong Kong); Hung-Ming Chen (National Yang Ming Chiao Tung University)

8E-1 (Time: 13:30-13:55)

DPO-3D: Differentiable Power Delivery Network Optimization via Flexible Modeling for Routability and IR-Drop Tradeoff in Face-to-Face 3D ICs……1273

*Zhen Zhuang (The Chinese University of Hong Kong), Zheng Yang (Georgia Institute of Technology), Yuxuan Zhao (The Chinese University of Hong Kong), Jiawei Hu (Georgia Institute of Technology), Bei Yu (The Chinese University of Hong Kong), Sung Kyu Lim (Georgia Institute of Technology), Tsung-Yi Ho (The Chinese University of Hong Kong)

8E-2 (Time: 13:55-14:20)

Enhancing Pin Accessibility Through Pin Pattern Migration and Optimization Across Cell Boundaries……1280

*Hyunbae Seo, Sehyeon Chung, Taewhan Kim (Seoul National University)

8E-3 (Time: 14:20-14:45)

Topological Optimization-Based Layer Assignment Method for Fan-Out Wafer-Level Packaging……1287

Haoying Wu, *Guanxian Zhu (Wuhan University of Technology), Xu He (Hunan University), Mingyu Liu (Huazhong University of Science and Technology)

8E-4 (Time: 14:45-15:10)

Au-MEDAL: Adaptable Grid Router with Metal Edge Detection And Layer Integration……1294

Andrew B. Kahng (University of California, San Diego), Seokhyeong Kang, Sehyeon Kim, *Jakang Lee (Pohang University of Science and Technology), Dooseok Yoon (University of California, San Diego)

Thursday, January 22, 2026

8E-5 (Time: 15:10-15:35)

8F (T5-D) Memory-Centric and Compute-in-Memory Innovations

Time: 13:30-15:35, Thursday, January 22, 2026
Location: Sleeping Beauty 5
Chair(s): Zhengwu LIU (The University of Hong Kong); Hongwu Jiang (The Hong Kong University of Science and Technology (Guangzhou))

8F-1 (Time: 13:30-13:55)

8F-2 (Time: 13:55-14:20)

8F-3 (Time: 14:20-14:45)

8F-4 (Time: 14:45-15:10)

8F-5 (Time: 15:10-15:35)

9A (T2-A) Advanced Embedded System Design and Optimization

Time: 15:55-18:00, Thursday, January 22, 2026
Location: Snow White 1
Chair(s): Xin Chen (University of New Mexico); Caiwen Ding (University of Minnesota - Twin Cities)

9A-1 (Time: 15:55-16:20)

Thursday, January 22, 2026

9A-2 (Time: 16:20-16:45)

9A-3 (Time: 16:45-17:10)

9A-4 (Time: 17:10-17:35)

9A-5 (Time: 17:35-18:00)

9C (T10-C) Advanced Thermal Analysis for Advanced Chips

Time: 15:55-18:00, Thursday, January 22, 2026
Location: Snow White 3
Chair(s): Zhiyao Xie (The Hong Kong University of Science and Technology); Tianshu Hou (The Chinese University of Hong Kong)

9C-1 (Time: 15:55-16:20)

9C-2 (Time: 16:20-16:45)

9C-3 (Time: 16:45-17:10)

9C-4 (Time: 17:10-17:35)

Thursday, January 22, 2026

9C-5 (Time: 17:35-18:00)

9D (Panel) AI Accelerators at a Crossroads: Who Will Power the Next Decade of AI?

Time: 15:55-18:00, Thursday, January 22, 2026
Location: Sleeping Beauty 1/2
Chair(s): Li Jiang (Shanghai Jiao Tong University)

Panelists: Yuan Xie (The Hong Kong University of Science and Technology), Yu Wang (Tsinghua University), Gang Chen (Shanghai Houmo Technology Co.,Ltd.), Shaodi Wang (Hangzhou Zhicun (Witmem) Technology Co., Ltd.), Guangyu Sun (Peking University)

9E (T9-A) Machine Learning and Optimization in Physical Design

Time: 15:55-18:00, Thursday, January 22, 2026
Location: Sleeping Beauty 3
Chair(s): Heechun Park (Ulsan National Institute of Science and Technology); Rupesh Karn (NYU)

9E-1 (Time: 15:55-16:20)

9E-2 (Time: 16:20-16:45)

9E-3 (Time: 16:45-17:10)

9E-4 (Time: 17:10-17:35)

9E-5 (Time: 17:35-18:00)

9F (T5-C) Ultra-Low Precision and Quantization Techniques

Time: 15:55-18:00, Thursday, January 22, 2026
Location: Sleeping Beauty 5
Chair(s): Ngai Wong (The University of Hong Kong); Yuzhe Ma (The Hong Kong University of Science and Technology (Guangzhou))

Thursday, January 22, 2026

9F-1 (Time: 15:55-16:20)

9F-2 (Time: 16:20-16:45)

9F-3 (Time: 16:45-17:10)

9F-4 (Time: 17:10-17:35)

9F-5 (Time: 17:35-18:00)

Information

Proceedings:

ASP-DAC 2026 will be providing an authority to access the download site for the conference proceedings. Conference registration in any of the categories will include it. The site will be open on Jan. 19, 2026. Please note that neither CD-ROM nor USB memory are provided.

Banquet:

Conference in-person registrants are invited to attend a banquet to be held on January 21, 2026. The banquet will be held from 18:30 to 20:30 at the "Cinderella Ballroom 1/6/7/8". Registrants receive a banquet ticket to the banquet when they register at the conference.

Free WiFi:

Free Public WiFi is available.

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The organizer cannot accept responsibility for accidents that might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Hongkong during the period of the Conference ranges between 17 degrees Celsius and 20 degrees Celsius.

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Only Hong Kong Dollars (HKD, HK$) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Hong Kong Dollars at foreign exchange banks and other authorized money exchange offices with your passport.

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Invitation to ASP-DAC 2027

On behalf of the Organizing Committee, it is my great pleasure and honor to invite you to the 32nd ASP-DAC, to be held in the very center of Tokyo, Japan, January 25-28, 2027.

We are planning to hold ASP-DAC 2027 at the Hitotsubashi Hall. This venue not only has very excellent access from Haneda and Narita airports, but also only 15 minutes walk, or you can take 1 station by subway from Tokyo Station.

We are also planning complimentary tours of Tokyo for participants from overseas. In recent years, artificial intelligence has seen rapid progress, accompanied by renewed momentum in the semiconductor industry. As large-scale semiconductor systems continue to increase in scale and complexity, there is a growing academic and technological demand for advanced design automation techniques, AI-assisted semiconductor design methodologies, and novel algorithms for artificial intelligence itself.

ASP-DAC 2027 provides a premier international forum for exploring state-of-the-art research results and future directions in electronic design automation, semiconductor and system design, and embedded systems. The conference offers an exceptional opportunity for in-depth technical discussions and the exchange of ideas among researchers and practitioners from around the world, fostering innovation at the intersection of artificial intelligence and design automation.

We look forward to seeing you in Tokyo during ASP-DAC 2027.

Makoto Ikeda
General Chair, ASP-DAC 2027

池田 誠